IEEE802.3aq Channel model ad-hoc

TP3 - Jitter Tolerance for Receiver Stressed Sensitivity Test

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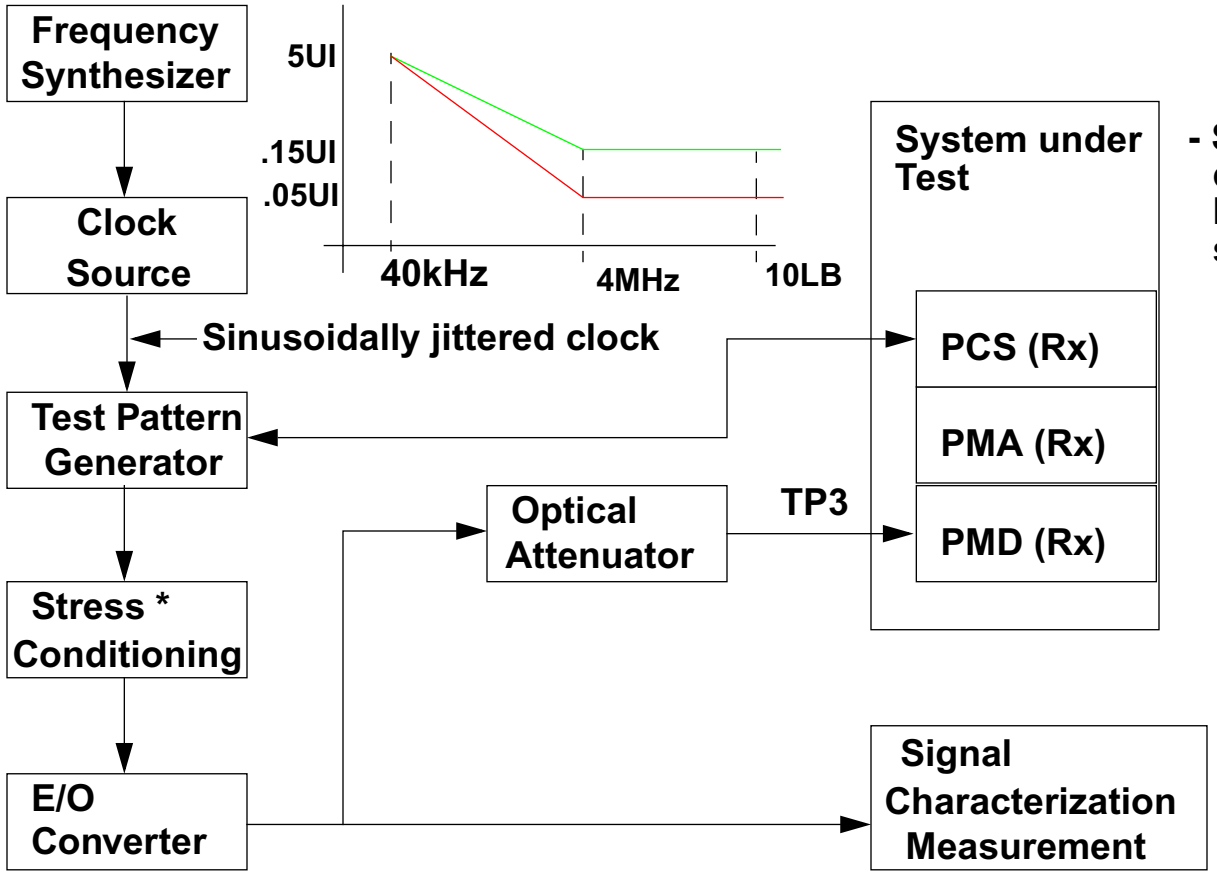
1. Jitter Tolerance for Receiver Stressed Sensitivity Test

802.3ae Clause 52, sinusoidal jitter for stressed receiver conformance test

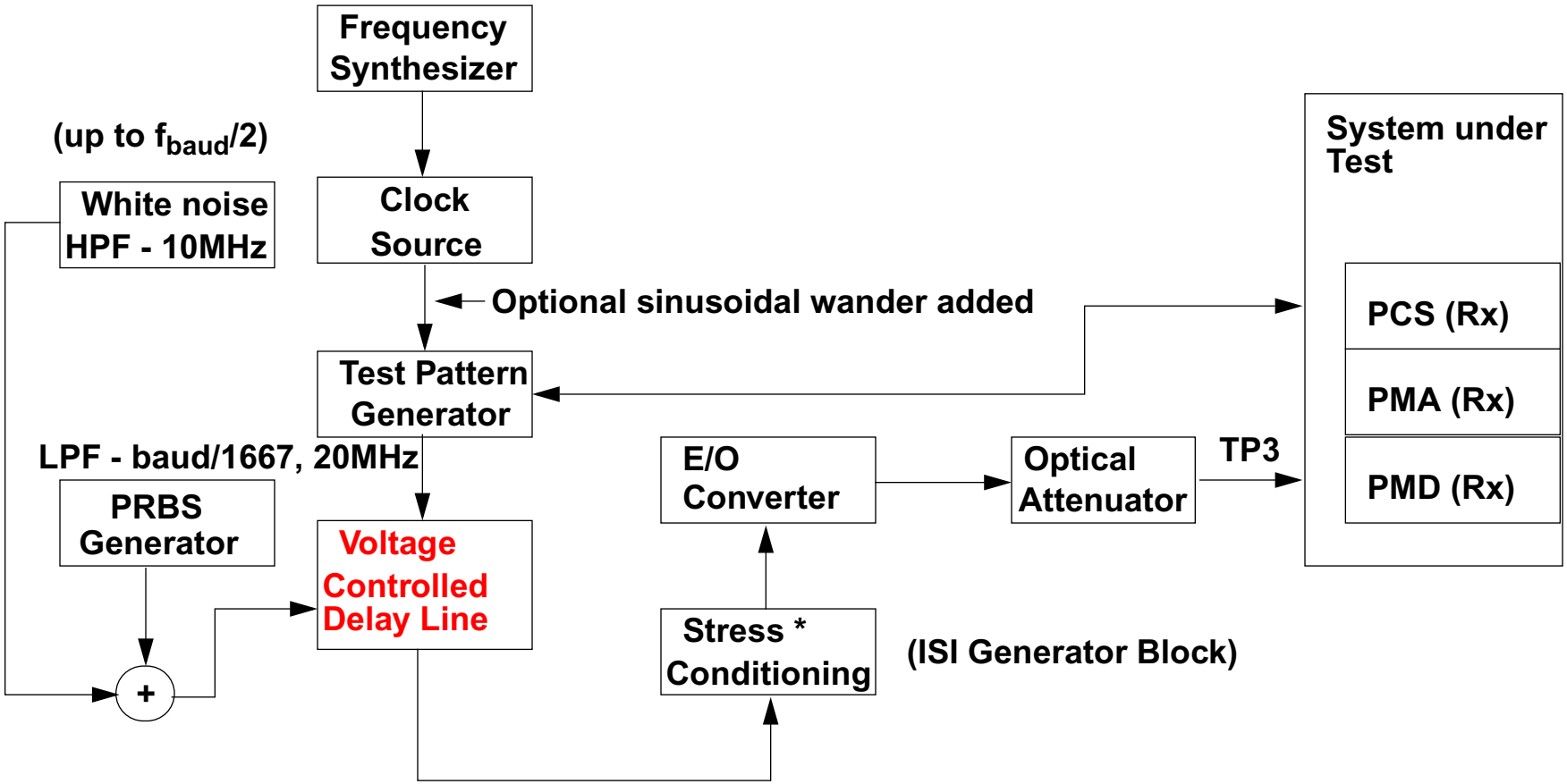


- Stress conditioning consists of a 4th order BT low-pass filter and sinusoidal interferer.

- The conformance test signal is used to validate that the PMD receiver meets BER requirements with near worst case waveforms including pulse width shrinkage, power, simulated channel penalties, and swept sinusoidal jitter contribution applied at TP3.

2. Jitter Tolerance for Receiver Stressed Sensitivity Test

Receiver conformance test, based on the CEI Implementation Agreement



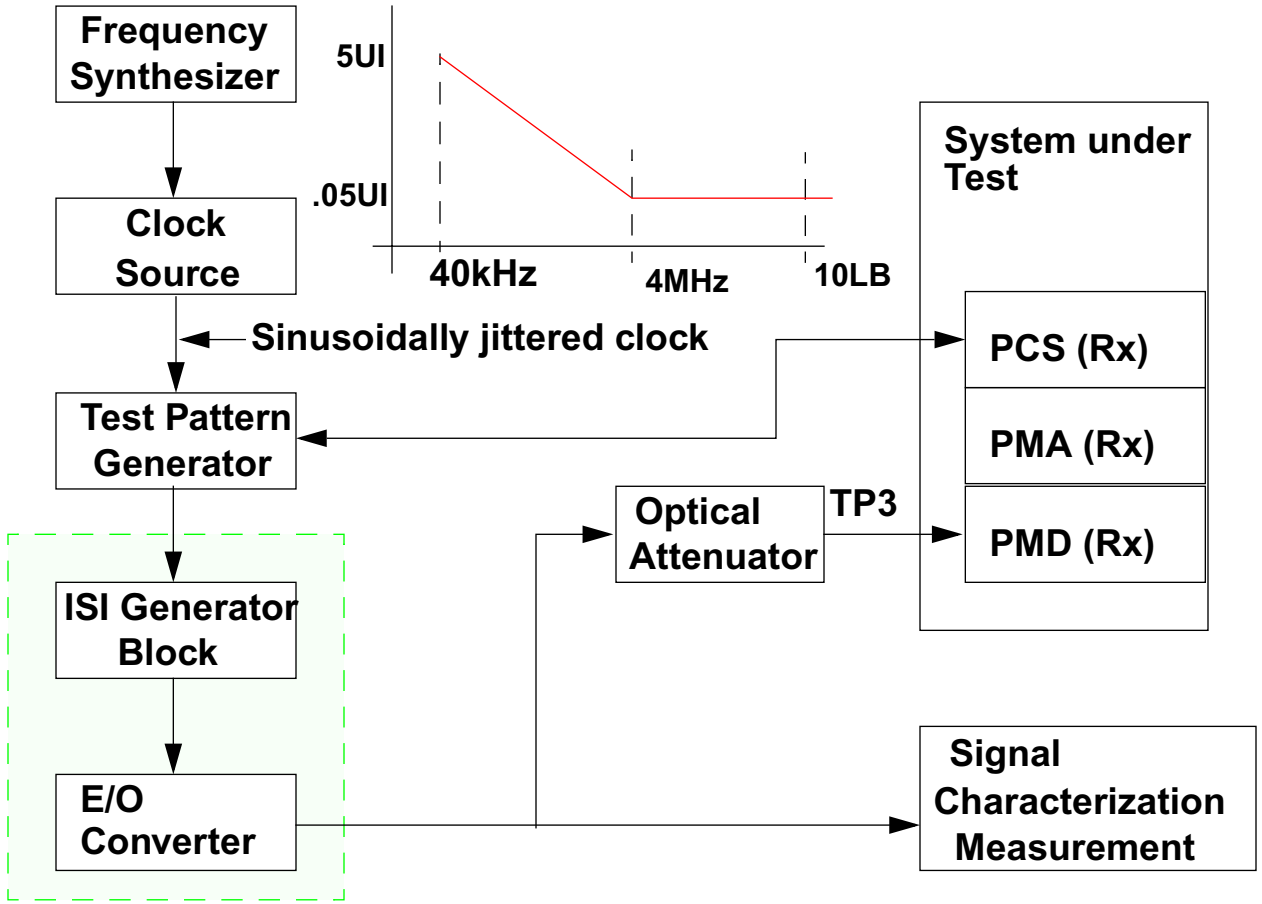
- The conformance test signal is used to validate that the PMD receiver meets BER requirements with any data pattern (data agnostic) and in the presence of crosstalk.
- The actual jitter is added using the voltage controlled delay line. The accuracy of this method, is dependent on the bandwidth, phase linearity and linear dynamic range of this circuit.

3. Jitter Sources and Impact on the Receiver Test

Jitter Source	Jitter Characteristics	Receiver impact	10GBASE-LRM Receiver
Transmitter clock, random jitter	High peak-to-peak amplitudes at low frequencies	The recovered clock will track the incoming jitter	Needed EDC will not correct
Laser random jitter	Small peak-to-peak amplitudes at low frequencies, uniform distribution at high-frequency	The recovered clock will not track the high-frequency incoming jitter	Needed EDC will not correct
Transmitter, pattern (data) dependent jitter (correlated)	Transmitter bandwidth limitation and phase non-linearities (ISI), high frequency components, (above 10 LB*)	The recovered clock will not track the high-frequency incoming jitter	Negligible compared with the channel contribution. Partially reduced by EDC.
Channel jitter contribution	Small for SMF, not generated in the “stress conditioning”, for 10GBASE-L.	Equalizer required for MMF.	Not needed. Jitter generation is included in the “non-quasi-symmetrical stressed signal generator”.

*LB - PLL loop bandwidth.

4. Jitter Tolerance for 10GBASE-LRM Receiver Stressed Sensitivity Test



- The conformance test signal is used to validate that the PMD receiver meets BER requirements with near worst case waveforms (including pre-cursor heavy and post-cursor heavy), power, simulated channel penalties, and swept sinusoidal jitter contribution applied at TP3.
- Noise contributions can be included in the ISI Generator Block.
- The test pattern generator as recommended for 10GBASE-R (802.3ae, clause 52).