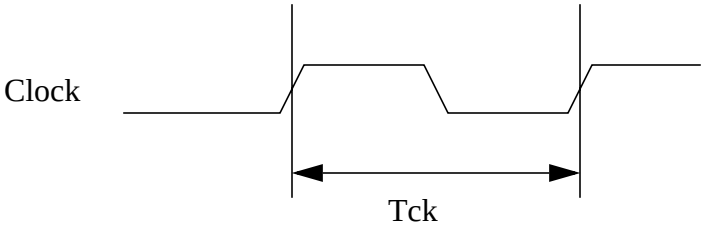
DDR Timing

The following timing specification is recommended for all DDR interfaces. The clock signal referred to below is the clock generated by the source device along with the data. All timing measurements are performed at the Vref crossing or at the differential crosspoint when a differential clock is used. For outputs, all timing measurements are performed driving into a 10 pF load.

Table 1: Timing Requirements

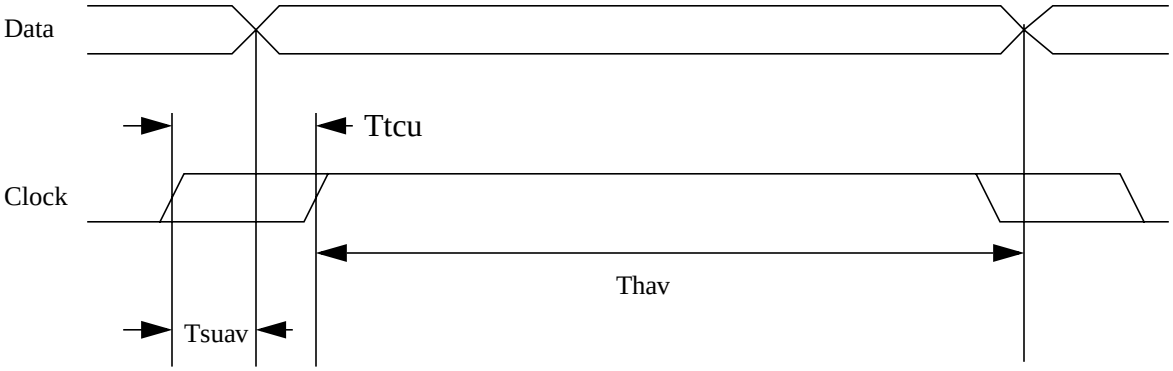
Parameter	Description	min.	max.	Units
Tck	Clock Period			
Tsuav	Data valid to clock transition Available setup time at the output of the source device			
Thav	Clock transition to data invalid Available hold time at the output of the source device			
Ttcu	Total clock uncertainty at the output of the source device			
Tsuav+Thav	Data valid window	0.3		Tck
Tsu	Input setup time			
Th	Input hold time			
Tsu+Th	Required data window at input		0.15	Tck

Clock Timing

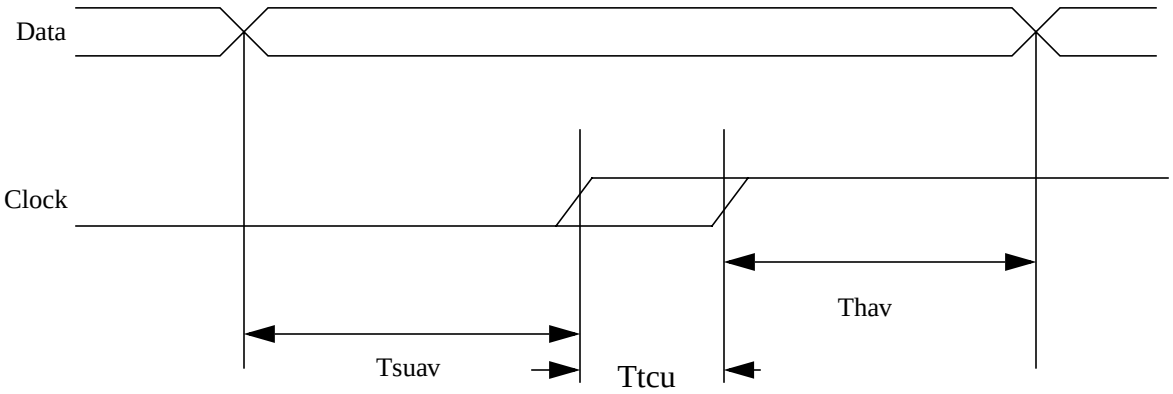


Output Timing

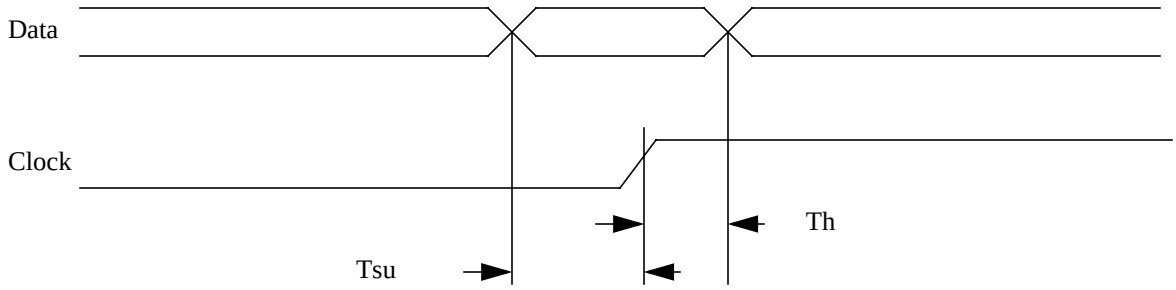
Edge aligned clock timing



Center aligned clock timing



Input Timing



Notes:

1. All timing parameters specified are at the pins/balls.

2. The data valid window calculation at the transmit device should include the effects of Simultaneous Switching Noise (SSN). In other words, SSN is part of the 0.2Tck (0.5Tck total - 0.3Tck for data valid window = 0.2 Tck) transmit device timing allocation.The other transmit device uncertainties that should be included into this allocation are (i) duty cycle deviations of the internal clock, (ii) internal clock jitter, (iii) output data to output clock routing skew on the chip, (iv) internal clock tree skew.

3. Board trace skew will be included in the 0.15Tck board timing allocation (0.3Tck output data valid available - 0.15Tck input data valid required = 0.15 Tck).

4. Inter-Symbol Interference (ISI) or pattern dependent delay will be included in the board timing allocation.

5. Crosstalk induced delay will be included in the board timing allocation.

6. Input timing allocation of 0.15Tck will include the input flip-flop setup and hold times and the on-chip routing skew between the data and clock signals.