Annex 48A

(normative)

Jitter test patterns

Editors' Notes: *To be removed prior to final publication.*

References:
NCITS-TR-25:1999 - Fibre Channel Methodologies for Jitter Specification

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 2.1, February 2001	Initial draft for IEEE P802.3ae Task Force recirculation ballot

This annex defines test patterns which allows the 10GBASE-X PHY described in Clause 48 to test its attached PMD for compliance while in a system environment. The patterns may be implemented at a bit, code-group or frame level and may be used for transmitter testing. The receiver may not have the capability to accept these diagnostic sequences, however, system debug can be improved if a receiver is able to test for one or more of these patterns and report bit errors (e.g. 8B/10B decoder errors) back to the user.

Editors' Note: *To be removed prior to final publication. These jitter patterns are applicable to the 10GBASE-LX4 PHY and possibly XAUI. XAUI applicability needs to be assessed by the XAUI jitter working group. XAUI applicability unanimously validated during 1/24/01 XAUI Jitter Conference call.*

48A.1 High frequency test pattern

The intent of this test pattern is to test random jitter (RJ) at a BER of 10^{-12}, and also to test the asymmetry of transition times. This high frequency test pattern generates a one, or light on, for a duration of 1 bit time, followed by a zero, or light off, for a duration of 1 bit time. This pattern repeats continuously for the duration of the test. For example: 10101010101010101010101010101010101010...

NOTE—This pattern can be generated by the repeated transmission of the D21.5 code-group. Disparity rules are followed.

48A.2 Low frequency test pattern

The intent of this test pattern is to test low frequency RJ and also to test PLL tracking error. This low frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 5 bit times. This pattern repeats continuously for the duration of the test. For example: 11111000001111100000111110000011111100000...

NOTE—This pattern can be generated by the repeated transmission of the K28.7 code-group. Disparity rules are followed.

48A.3 Mixed frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ). This mixed frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 1 bit times, followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 2 bit times followed by a zero for 5 bit times followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 1 bit time followed by a zero for 2 bit times. This pattern repeats continuously for the duration of the test. For example: 11111010110000010100111110101100000010100...

NOTE—This pattern can be generated by the repeated transmission of the K28.5 code-group. Disparity rules are followed.

48A.4 Continuous random test pattern

The Continuous random test pattern is intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

NOTE—The derivation of this pattern may be found in NCITS TR-25:1999, “Methodology of Jitter Specification”. This Annex uses similar modifications to fit the RPAT test pattern into an 802.3 frame.

The continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters as specified in clause 48 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1488 data octets (124 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE. The Modified RPAT sequence is repeated on each lane:

PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (LOOP 124 TIMES, 31 TIMES ON EACH of 4 LANES)

BE D7 23 47 6B 8F B3 14 5E FB 35 59

CRC

F8 79 05 59

IPG

00 00 00 00 00 00 00 00 00 00 00 00

END

48A.5 Continuous jitter tolerance test pattern

The Continuous jitter tolerance test pattern is intended for receiver jitter tolerance by exposing a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low transition density patterns with repeating high transition density patterns. The repeating code-group durations should be longer than the time constants in the receiver clock recovery circuit. This assures that the clock phase has followed the systematic pattern jitter and the data sampling circuitry is exposed to large systematic phase jumps. This stresses the timing margins in the received eye. The following test bit sequences are proposed for receive jitter tolerance testing.

NOTE—The derivation of this pattern may be found in NCITS TR-25:1999, "Methodology of Jitter Specification". This Annex uses similar modifications to fit the JTPAT test pattern into an 802.3 frame.

The Continuous jitter tolerance test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters as specified in clause 48 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1504 data octets, plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE. The Modified JTPAT sequence is repeated on each lane:

PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED JTPAT SEQUENCE

7E for 528 Bytes - Low Density Transition Pattern;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

AB for 4 Bytes - Phase Shift;

B5 for 160 Bytes - High Density Transition Pattern

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

7E for 528 Bytes - Low Density Transition Pattern;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

AB for 4 Bytes - Phase Shift;

B5 for 160 Bytes - High Density Transition Pattern

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift;

F4 for 4 Bytes - Phase Shift;

EB for 4 Bytes - Phase Shift.

Editors' Note: *To be removed prior to final publication. The number of times that the low/high data values are repeated in the frame may need to be adjusted to account for line rate differences between Fibre Channel and 10GBASE-LX4. For example the low high values above are repeated twice within a maximum length 802.3 frame.*

CRC

D5 7A 06 01

IPG

00 00 00 00 00 00 00 00 00 00 00 00

END