The Deficiencies in Measuring Input Jitter Tolerance (IJT) using Sine wave modulated Jitter

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Introduction

Today IJT is measured by phase modulating the clock of a data pattern generator with a sine wave and analyzing the data errors of the clock and data recovery circuit. This method is effective for measuring a specific part of the jitter template. However, it becomes difficult in practice to measure the high frequency end of the jitter template, which is the most critical part for receivers. In this technical note we want to point out some deficiencies in this type of IJT measurement. We also propose a simpler yet accurate way of testing IJT.

Sonet Jitter Template: Lets consider Sonet OC192 jitter template (Fig 1.0, Ref. 1)

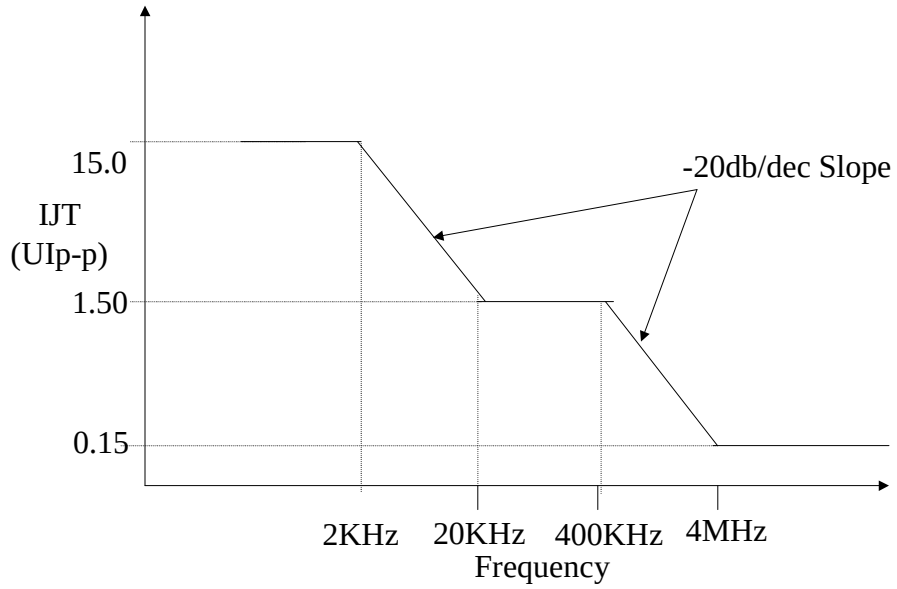


Fig 1.0: OC192 Jitter Template

In fig 1.0 the high frequency limit of the input jitter tolerance is not shown. Since all bandwidth limited jitter or duty cycle induced jitter (DCD), etc., may have jitter contribution up to ½ the data rate clock frequency (Ref 2.0). Thus the high end of the 0.15UI jitter tolerance should stretch up to 5GHz in OC192.

Concerns about the Sinusoidal Jitter Test for the IJT

1. It is hard to find sinusoidal modulation equipment with a 10GHz clock frequency and a modulation frequency above 20MHz, though some of the 10Gb/s receivers may have a phase-locked loop bandwidth over 20MHz. Such a receiver can track input jitter up to 20MHz modulation frequency; therefore any measurement on IJT modulated over 4MHz may not necessarily mean the device under test has sufficient IJT, which an OC192 standard compliant source may generate.

   Consider fig 2.0. It assumes a receiver with 20MHz loop bandwidth, where the IJT test was performed only up to 10MHz, due to the limit of the tester.

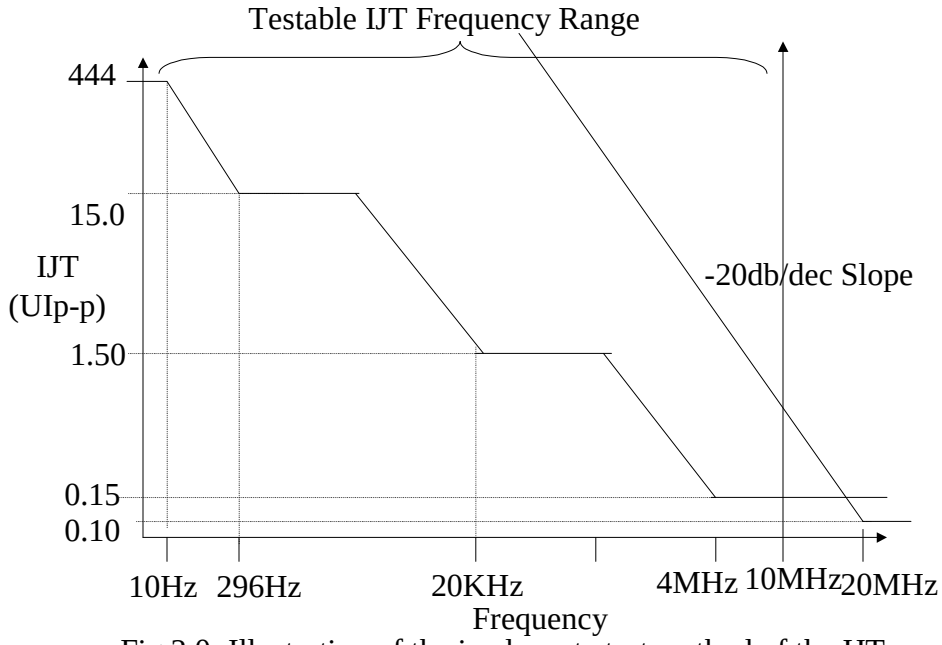
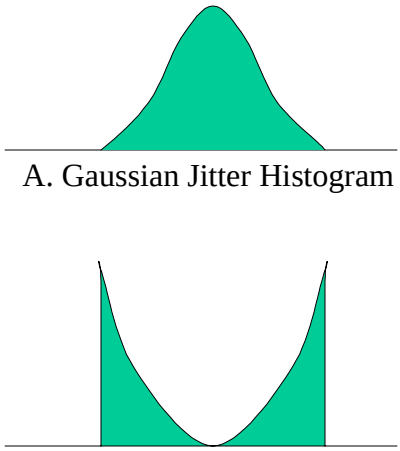


Fig 2.0: Illustration of the inadequate test method of the IJT

2. While this method does not adequately test the device for high frequency components of the input jitter, it over stresses the device with the high density of jitter at the extremes of the jitter histogram. Fig 3.0 compares the histogram for white noise (Gaussian) jitter to the histogram for sinusoidal phase jitter. (Note: Authors can be contacted for the explanation how these two jitter histograms are achieved.)



A. Gaussian Jitter Histogram

B. Sinewave Jitter Histogram

Fig 3.0 Gaussian and Sinewave Jitter Histogram

In case of sinusoidal modulation, the extra "energy" of the extremes of the jitter histogram has no effect in testing most of the clock and data recovery circuits as long as the input jitter modulation is under 0.5UIp-p. SONET specifies 0.15UIp-p IJT beyond the loop bandwidth, which is substantially lower than 0.5UIp-p. It has never been an issue. Theoretically, IJT beyond the loop bandwidth could be as much as 1UIp-p, but in practice 0.8UIp-p or more has been demonstrated. In 10G Ethernet, over 0.5UIp-p of IJT has been proposed. When IJT is over 0.5UIp-p, and the sinusoidal modulation frequency is higher than the loop bandwidth, there is a danger of PLL not locking or false locking. This can be explained in both the time domain and frequency domain.

Frequency Domain Explanation

Consider the frequency domain first. When a clock source (fo) is phase modulated at some frequency (fm), there are peaks in the frequency spectrum (measured by spectrum analyzer) at fo ± fm, fo ± 2fm … and so on. Figure 4.0 shows such spectrum.

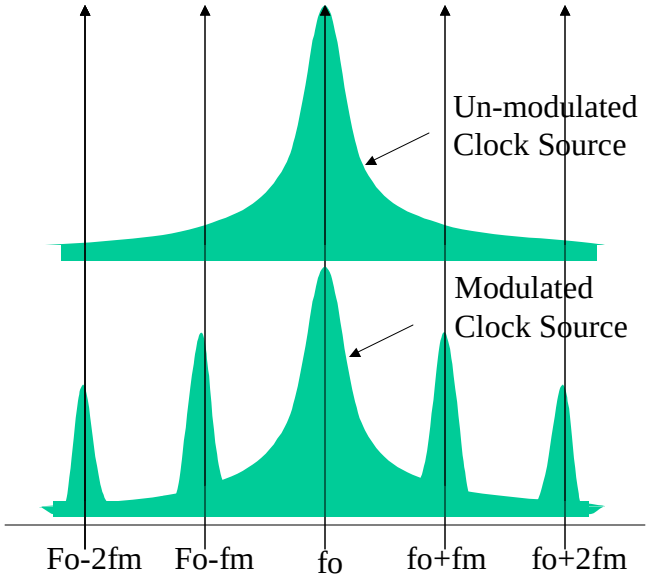
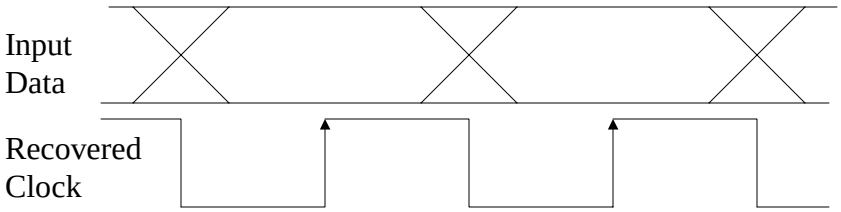


Fig 4.0 Frequency spectrum of un-modulated and phase modulated clock source

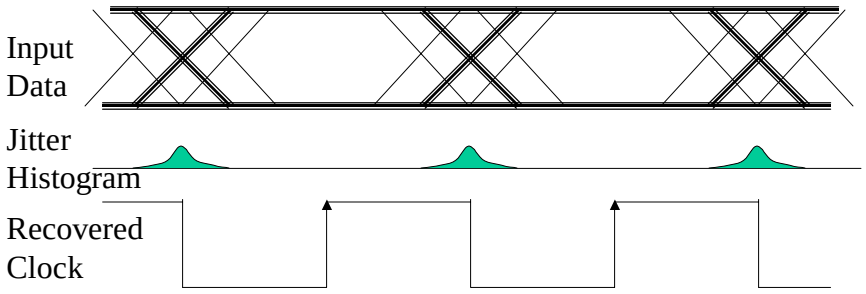
Because of the sharp peaks, the PLL may lock to side peaks and in that case the main peak would look like jitter.

Time Domain Explanation

Consider a Clock and Data recovery circuit where the falling edge of the internal VCO clock aligns to the data transition points (Fig 5.0). The incoming data may have jitter, thus the clock is aligned to the highest data transition density of the incoming data. In the case of Gaussian jitter, even if the IJT is more than 0.5 UI the highest data transition density position is well defined in the center of the distribution (Fig 6.0). However in the case of sinusoidal phase jitter, the highest data transition density position could be very confusing (Fig 7.0). There could be two different positions where the PLL may lock, and in one case it would be false locked.



A. Input Data With No Jitter



B. Input Data With Jitter

Fig 5.0: Clock and Data Recovery

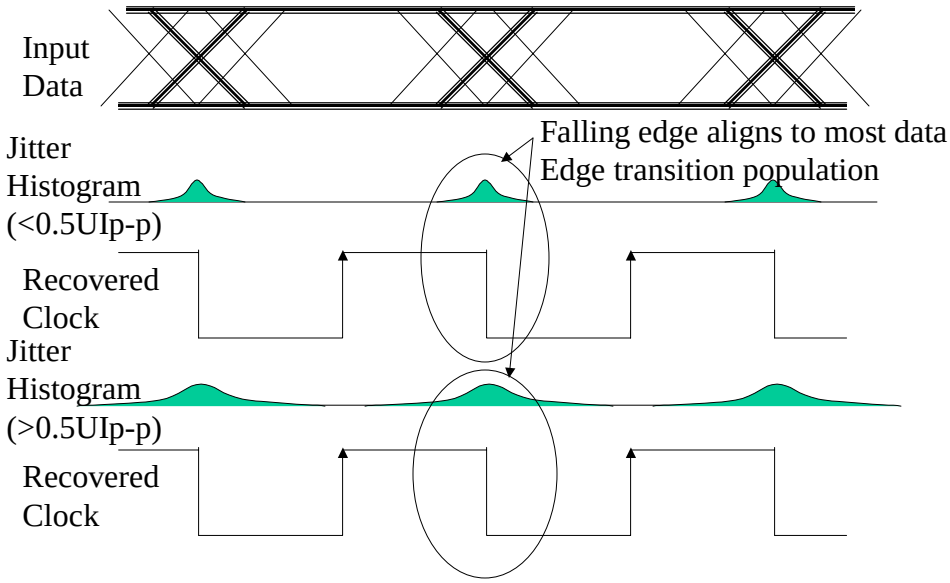


Fig 6.0: Clock and Data Recovery in case of gaussian input jitter

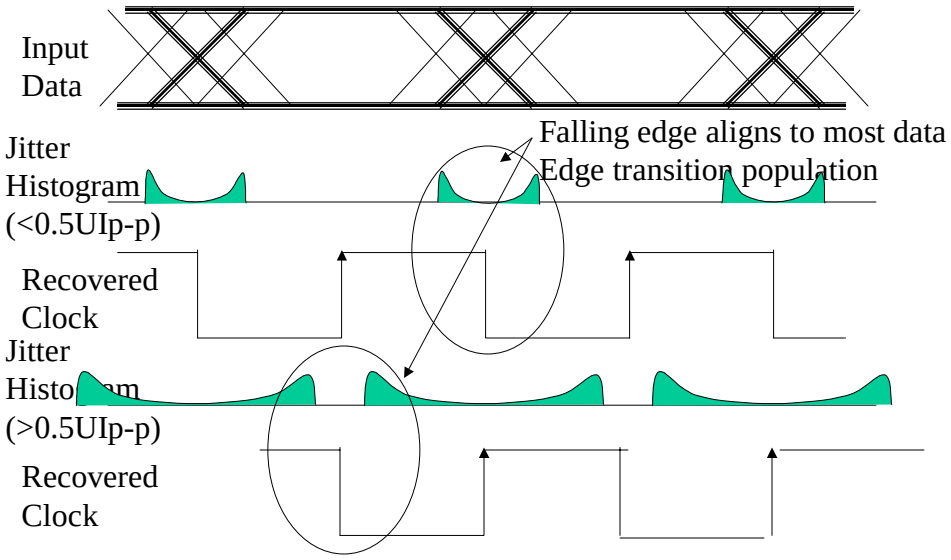


Fig 7.0: Clock and Data Recovery in case of sinwave input jitter

Recommendation

To overcome with the problems with sinusoidal modulation, we propose an alternate way. Fig 8.0 shows a way of generating jitter.

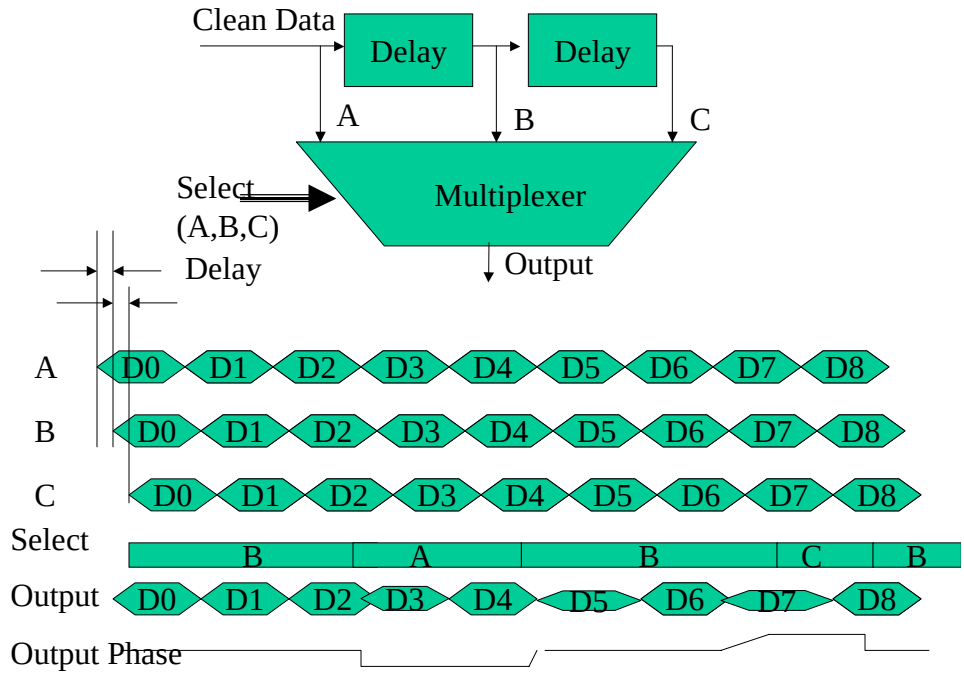


Fig 8.0: Digital Jitter Generation

In this jitter generation method, the delay represents the modulation index. Because phase change happens as a step, the jitter contains all the frequency contents up to a very high frequency, which is limited by the switching time of the multiplexer, which could be

as low as one symbol. In this way, a very high frequency IJT could be measured. The histogram of the digital jitter generation is compared to sinusoidal and Gaussian jitter histograms in Fig 9.0. It is also shown in figure 9.0 C, that the digital jitter generation approximates the Gaussian jitter and it does not have a null at the place where the highest data transition is expected, as was the case with sinusoidal jitter.

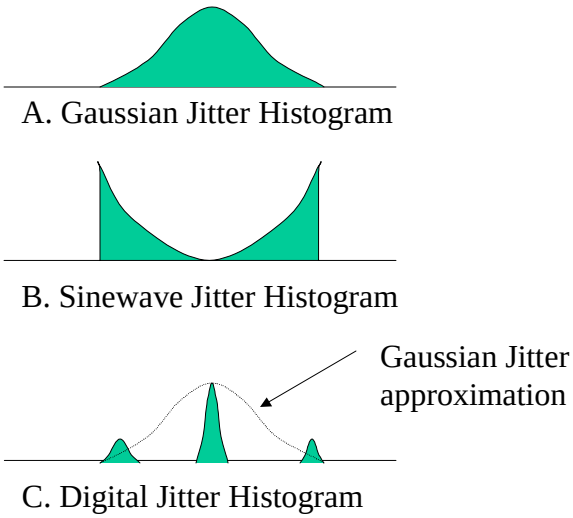


Fig 9.0 Gaussian and Sinewave Jitter Histogram

Conclusion

In this technical note, an alternate method of IJT testing is recommended which solves some of the deficiencies in the traditional method of IJT testing using sinusoidal phase jitter. The proposed jitter modulation could test very high frequency IJT, without overstressing the device under test with more energy at the sidebands. The proposed method would not confuse IJT with the phase locking characteristics of the clock and data recovery circuit.

References:

1. Yuriy M. Greshishchev et al, “A Fully Integrated SiGe Receiver IC for 10-Gb/s Data Rate”, IEEE Journal of Solid State Circuits, Vol 35, pp. 1949-1956, No. 12, Dec 2000.
2. Atul K.Gupta et al, “Loop Bandwidth Optimization and Jitter Measurement Techniques for Serial HDTV systems”, SMPTE Journal, pp. 703-712, Sep 2000.