bered bits are received before higher-numbered bits), and the data-groups must be presented in the sequence in which they were received. The PMA sublayer is not required to align the data being presented to the WIS on any boundary.

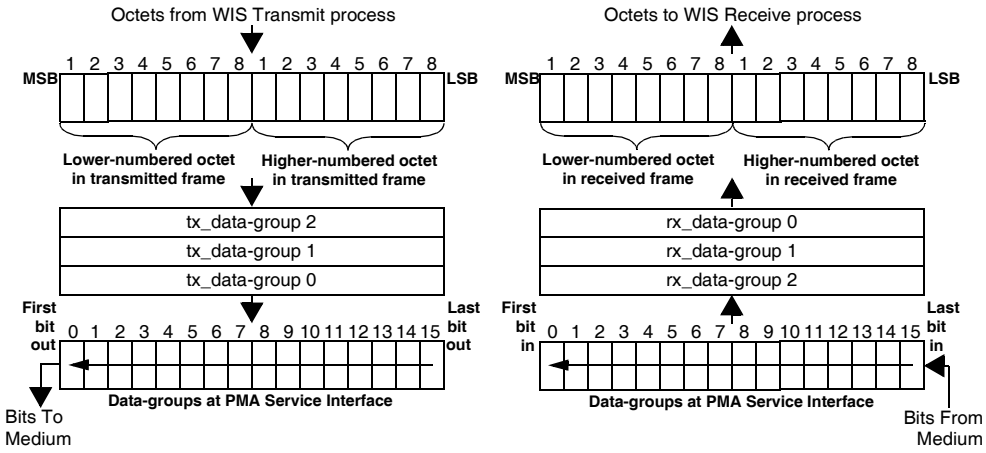

Figure 50–11—Transmission order

The WIS also utilizes the signal detect primitive received from the PMA sublayer to determine when the PMA is unable to provide valid data to the WIS via its service interface. This primitive is used to unlock the state machine implemented in the Synchronization process and force it to re-synchronize, as described in 50.4.

NOTE—The signal detect primitive received from the PMA differs from the Loss of Signal (LOS) defect described in 50.3.2.5. LOS is a status condition that is reported to Layer Management for error monitoring purposes (50.3.9.1.5), but otherwise does not affect the internal functioning of the Receive Process or the Synchronization Process. The PMA signal detect primitive, however, acts as a control signal that directly affects all parts of the WIS receive functionality.

50.3.7 WIS data delay constraints

The sum of the transmit and receive data delays for any implementation of the WIS shall not exceed 14000 BT. Transmit data delay is measured from the input of a given unit of data by the PCS at the WIS service interface to the presentation of the same unit of data by the WIS to the PMA at the PMA service interface. Receive data delay is measured from the input of a given unit of data by the PMA at the PMA service interface to the presentation of the same unit of data by the WIS to the PCS at the WIS service interface. The time required to insert or process any necessary overhead or stuff octets must be included as part of the data delay incurred by the WIS. No constraint is placed on the individual values of the transmit and receive data delays for a given implementation, provided their sum falls within the above limit.

50.3.8 WIS jitter pattern generator and checker

The WIS shall incorporate a jitter pattern generator and a jitter pattern checker to permit in-circuit testing using jitter test patterns. Jitter test mode can be activated separately for the transmit and receive portions of the WIS, according to the WIS Transmit jitter test enable and WIS Receive jitter test enable control bits supported within its management registers (see 45.2.2.6). In addition, two different types of test patterns (square-wave and pseudo-random) may be selected by means of the Jitter test pattern control bit. The specific test pattern to be output or received may further be selected by means of the 10G WIS Jitter Test Seed register (45.2.2.18). Errors detected during jitter pattern testing are recorded and provided to the Station Management entity via the 10G WIS Jitter Test Error Count register (45.2.2.19). The WIS Service Interface is inoperative when either the WIS Transmit process or WIS Receive process is placed in jitter test mode.

When the WIS transmit function is operating in jitter test mode, the jitter pattern generator shall produce a continuous jitter test pattern which is sent 16 bits at a time to the underlying PMA sublayer via PMA_UNITDATA.request primitives. When the WIS receive function is operating in jitter test mode, and the pseudo-random test pattern has been selected, 16-bit data-groups received from the underlying PMA sublayer by means of PMA_UNITDATA.indicate primitives shall be accepted and processed by the jitter pattern checker, which shall verify that the received data corresponds to the expected jitter test pattern.

In the square-wave jitter test mode, the WIS Transmit, Receive and Synchronization processes shall be disabled or otherwise prevented from processing data, and the contents of the 16-bit 10G WIS Jitter Test Seed register are continuously transferred to the PMA via the PMA Service Interface. The most significant bit of the 10G WIS Jitter Test Seed register shall form the most-significant bit of the 16-bit data-group sent to the PMA, and the least-significant bit shall form the least-significant bit of the data-group. The Station Management entity is responsible for placing an appropriate pattern of bits into the 10G WIS Jitter Test Seed register so as to produce a square-wave pattern at the output of the PMA. The default bit pattern to be loaded into the 10G WIS Jitter Test Seed register shall be 00-FF hexadecimal. No checking is performed on the 16-bit data-groups received from the PMA sublayer in this mode.

In the pseudo-random jitter test mode, the WIS Transmit process is utilized to generate a transmitted jitter test pattern (if activated by the WIS Transmit jitter test enable control bit) and the WIS Synchronization and Receive processes are utilized to check a received jitter test pattern (if separately activated by the WIS Receive jitter test enable control bit). Figure 50–12 provides a functional diagram of the WIS when operating in this mode.

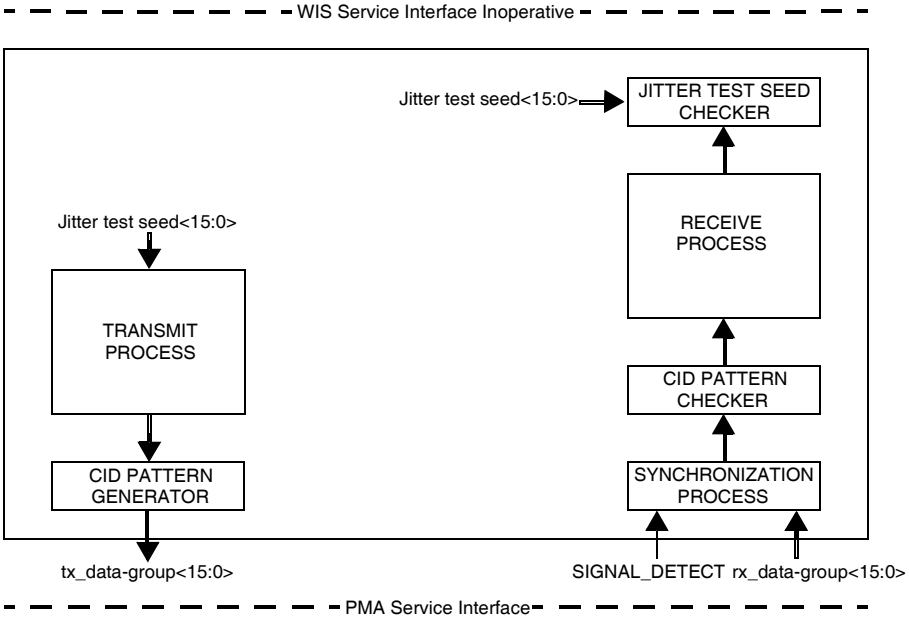

Figure 50–12—Pseudo-random jitter test mode operation

When placed in pseudo-random jitter test mode, the input to the payload mapping function of the WIS Transmit process (see 50.3.1.1) shall be obtained directly from the 10G WIS Jitter Test Seed register, such that the contents of this register are used in place of the tx_data-unit<15:0> parameter of the WIS Service Interface. Bit 0 of the 10G WIS Jitter Test Seed register shall correspond to tx_data-unit<0> and bit 15 of the register shall correspond to tx_data-unit<15>. All of the Path, Line and Section Overhead bytes shall be set to their normal values as defined elsewhere in this clause. The default value of 00000001 shall be used for the transmitted J0 octet.

The output of the WIS Transmit process is modified by a Consecutive Identical Digit (CID) pattern generator before finally being transferred to the PMA via the PMA Service Interface. The CID pattern generator locates the J0 and Z0 octets in the Section Overhead portion of the transmitted WIS frames (see 50.3.2.3) and replaces them with a pattern of 1536 bits constructed as follows:

a) Approximately 72 consecutive logic zero bits, followed by:
b) a pseudo-random sequence having a 50% ones-density and a run length limited to between 4 and 11 bits, followed by:
c) approximately 72 consecutive logic one bits.

The length of the pseudo-random sequence shall be selected such that the total length of the CID pattern is exactly 1536 bits, but the exact value chosen is implementation specific.

When the WIS receive function is placed in pseudo-random jitter test mode, as shown in Figure 50–12, the WIS Receive and Synchronization processes operate normally, with the exception that the J0 and Z0 bytes in the WIS frames received from the PMA shall be interpreted as carrying a CID pattern. The output of the Synchronization process is passed to a CID pattern checker that first verifies the contents of the received CID pattern present in the J0 and Z0 octet positions, and then replaces the 1536-bit CID pattern space with the default values for J0 and Z0 before transferring the data to the WIS Receive process. Errors detected by the CID pattern checker shall be counted and reported via the 10G WIS Jitter Test Error Count register. The output of the WIS Receive process shall be passed to a jitter test seed checker, which verifies that the expected 16-bit jitter test seed pattern (as defined by the 10G WIS Jitter Test Seed register) is present throughout the payload capacity of the received WIS frames. Errors detected by the jitter test seed checker shall also be counted and reported via the 10G WIS Jitter Test Error Count register.

The Station Management entity is also responsible for monitoring parity errors detected and reported by the WIS Receive process, via the 10G WIS Line BIP Errors register (45.2.2.15), the 10G WIS Path Block Error Count register (45.2.2.16), and the 10G WIS Section Section BIP Error Count register (45.2.2.17), to detect additional bit errors during the jitter test process.

NOTE—The implied re-use of the WIS Transmit, Receive and Synchronization processes to implement the pseudo-random jitter test functions is not a required attribute; implementations may select any physical means of realizing the jitter transmit and receive functionality, provided that the external behavior of the WIS conforms to that described herein.

50.3.9 Loopback

The WIS shall be placed in loopback mode when the Loopback bit in the WIS Control 1 register (45.2.2.1.2) is set to a logic one. In this mode, the WIS shall accept data on the transmit path from the 10GBASE-R PCS and return it on the receive path to the 10GBASE-R PCS. In addition, the WIS shall transmit a continuous sequence of eight logic one bits followed by eight logic zero bits to the PMA sublayer, in the pattern 00-FF hexadecimal. No SONET overhead or fixed stuff shall be output to the PMA at this time. The WIS shall ignore all data presented to it by the PMA sublayer during loopback.

NOTE—The signal path through the WIS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that this signal path encompass as much of the WIS circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data, while ensuring that remote entities do not interpret this test data as valid information. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

50.3.10 Management interface

The WIS shall support a set of required and optional management objects to permit it to be controlled by the Station Management entity (STA). Access to management objects within the WIS is accomplished by means of a set of registers within the MDIO register space as defined in 45.2.2, which are implemented by the Link Management function depicted in Figure 50–2.