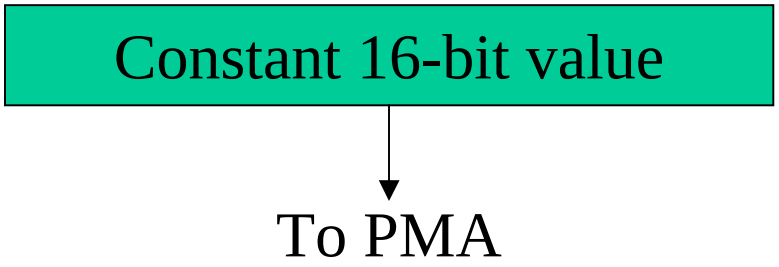
WIS Jitter Patterns

Patterns selected

1. Square-wave pattern (transmit only)
   - Output constant 16-bit value to PMA from MDIO register
   - PMA will convert this 16-bit value to an output waveform
   - The 16-bit value selected should produce a square wave
   - The default value selected is 0x00FF (8 ones, 8 zeros)
2. Pseudo-random pattern (generated & checked)
   - Input 16-bit seed to normal WIS transmit process
   - WIS produces a SONET frame with a pseudo-random payload set to the product of the seed and the SONET scrambler
   - Overwrite the J0/Z0 field (192 bytes) with a CID pattern
     - CID = 72 ‘0’s, 1392 pseudorandom bits, 72 ‘1’s
   - Output the result to the PMA for serialization/transmission
   - Check same pattern as received from PMA using WIS receive process

Square-wave pattern



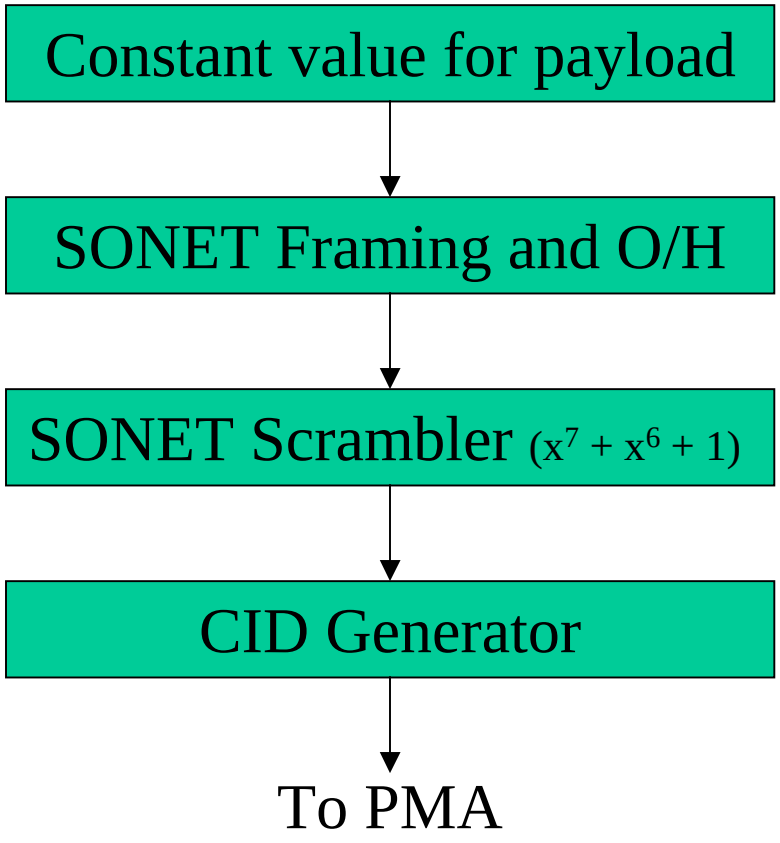
Replaces WIS Transmit process output

- Taken from MDIO register

Default transmit value = 0x00FF; square wave of 8 zeros followed by 8 ones

Transmit only; WIS Receive process is disabled

Pseudo-random pattern (TX)



Replaces payload from PCS
- Taken from MDIO register

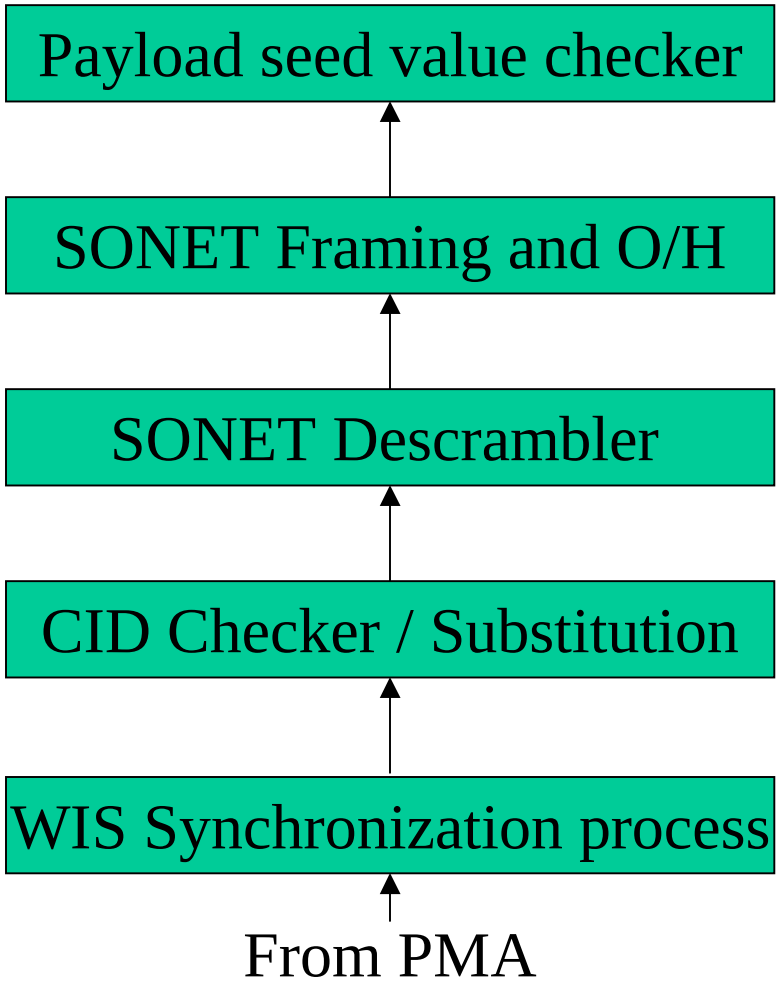
Standard SONET Framing
J0 = 0x01

Standard SONET Scrambler

CID = Consecutive Identical Digits
- 72 consecutive '1's and 72 consecutive '0's placed in J0/Z0 byte locations
- Overwrites output of WIS Transmit process

Total pattern length = 155520 bytes (1,244,160 bits); repeat rate = 8000/sec

Pseudo-random pattern (RX)



Checks contents of frame payload

- Compares to seed in MDIO register

Standard SONET framing

Standard SONET descrambler

Checks CID value against expected

Replaces CID field with original J0/Z0 for use by the WIS Receive process (J0 = 0x01)

Standard SONET frame sync

Detection of bit errors

1. Normal WIS parity checking
   - Section BIP
   - Line BIP
   - Path Block Errors
2. Jitter test hardware checking
   - Compare CID to expected value, record number of bit differences
   - Compare payload extracted from WIS frames to expected value, record number of bit differences
3. Reporting
   - MDIO registers indicating BIP and Block errors
   - MDIO register indicating CID and payload bit errors (total)

Open issues

1. Suitability of pseudo-random pattern
   - Adequate test coverage?
   - Adequate representation of expected worst-case pattern?
   - Is a constant seed value OK for use as the payload (i.e., can the SONET scrambler be relied on to generate a good enough PRBS pattern), or is a separate PRBS generator for the payload needed?
   - Note that the 10GE jitter spectrum is not bandlimited to 80 MHz, unlike SONET
2. Implementability
   - Is the structure outlined implementable? What about the processing of the CID field on receive?
   - Will it unduly tax existing implementations of WIS/SONET framers?
3. Interoperability
   - CID has some unspecified features – precise length of ‘0’ and ‘1’ sequences, contents of pseudo-random bit string separating ‘0’s & ‘1’s; is this likely to give rise to interoperation issues? Should this be specified exactly? (And, if so, what should the spec be?)