25Gb/s Single Lane SMF 10km PMDs Technical Feasibility

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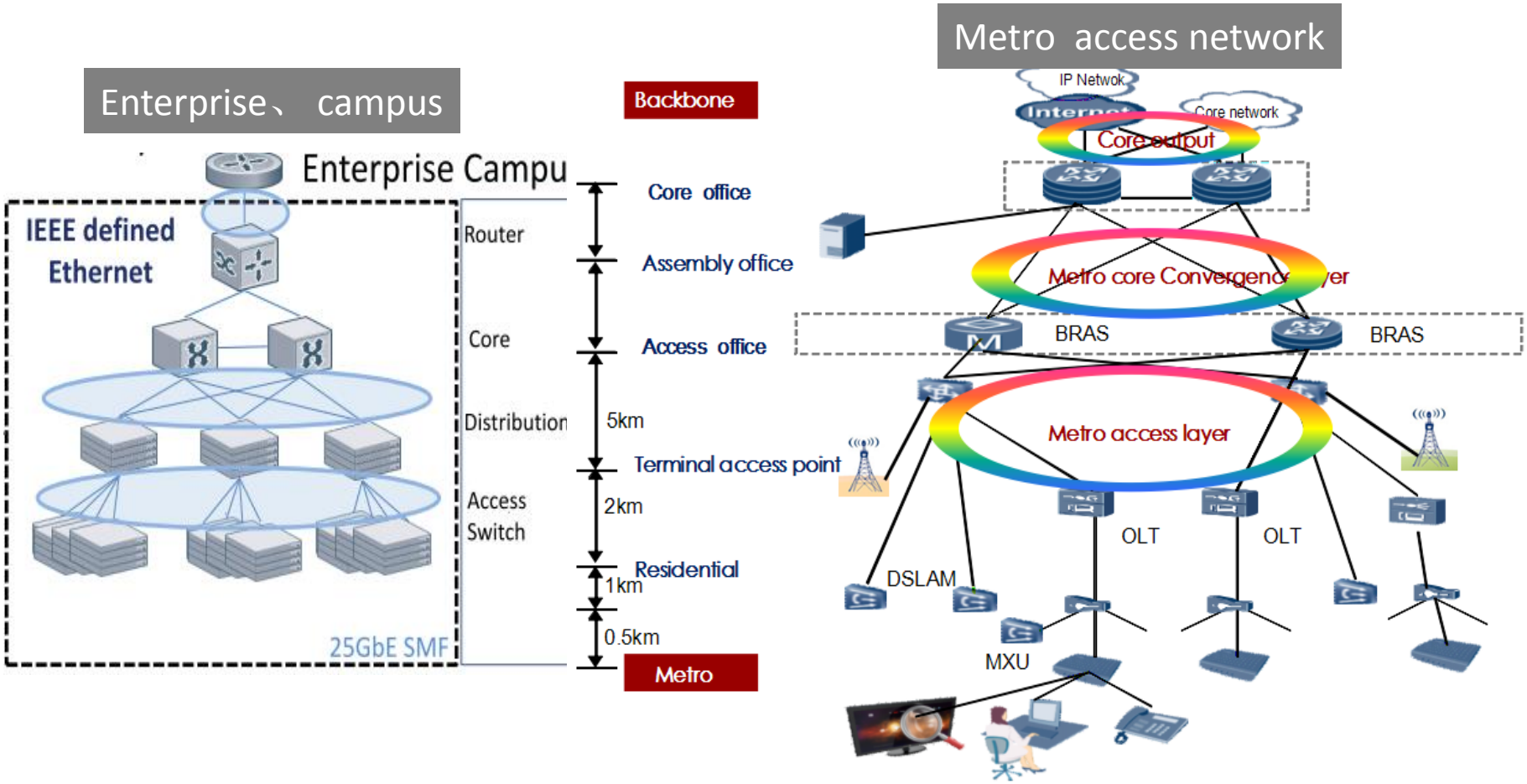
Outline

- 10km standard is needed
- Technical feasibility of 10km
- Test result
- Cost
- Potential of 25Gb/s

10km standard is needed

- Initial applications of 25G SMF PMDs



In Enterprise, Campus and Metro/Access area,

- More than 50% distance is <10km.

◆ 2km standard is needed?

No.

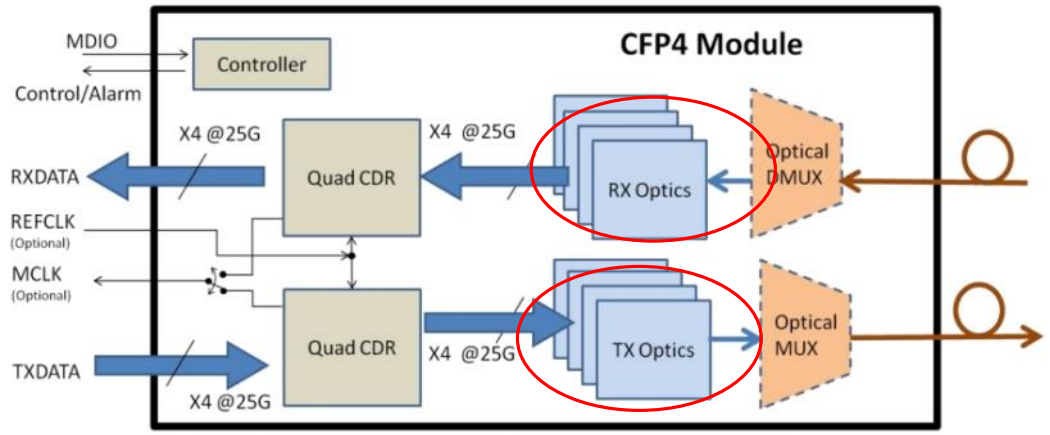
1）The main application of 25G SMF PMDs is not in datacenter but Enterprise, Campus and Metro/Access networks.
2km is not a typical distance.

2）Technically the solutions of 2km and 10km are almost the same. The cost of 2km is only <10% lower than that of 10km.

Technical Feasibility of 10km

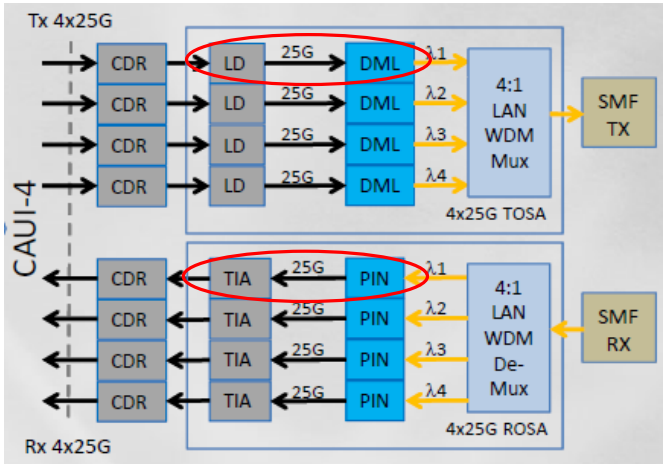
- Reuse the technology of 100GBASE-LR4

CFP: EML TOSA+ PIN-TIA ROSA



CFP: 4x28Gbps per channel

QSFP: DML TOSA+PIN-TIA ROSA



QSFP: 4x25.8Gbps per channel

The internal structure of the 100GBASE-LR4 is made up of 4 x25G.

◆ The best solution for implementation

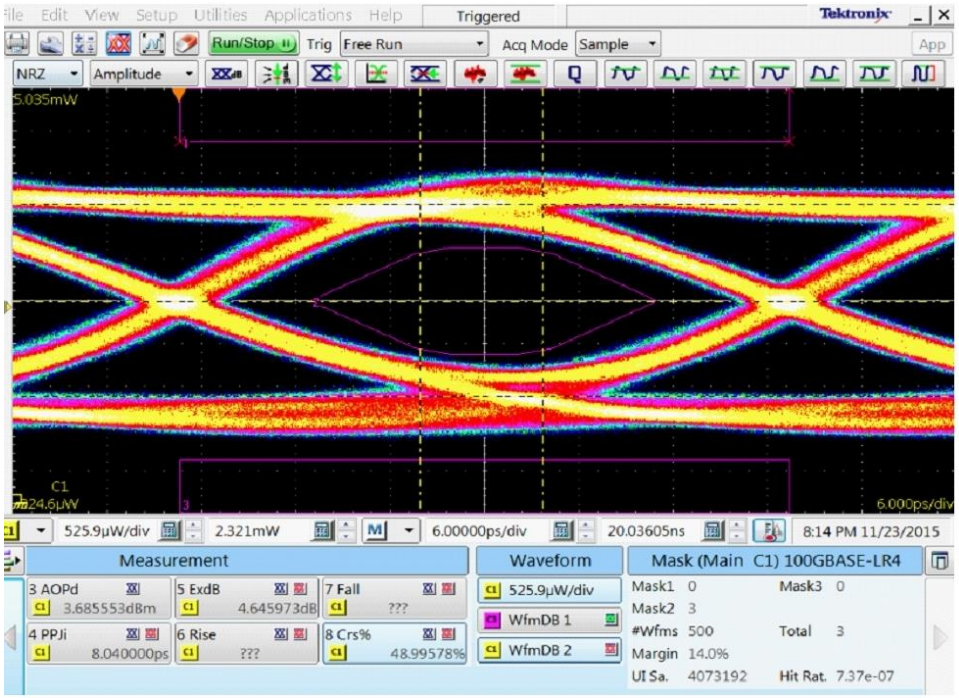
	Cost	Power consumption	Maturity
EML+PIN	high	high	yes
DML+PIN	low	low	yes
SIP (silicon photonics)			no

- ✓ EML have to use TEC but DML is uncooled,
- ✓ the power consumption of EML is much higher than DML.
- ✓ The cost of EML is twice higher than DML.
- ✓ SIP is an attractive technology, but now it's not the time to use it in 25G single lane PMDs. It's not mature enough.

Test result

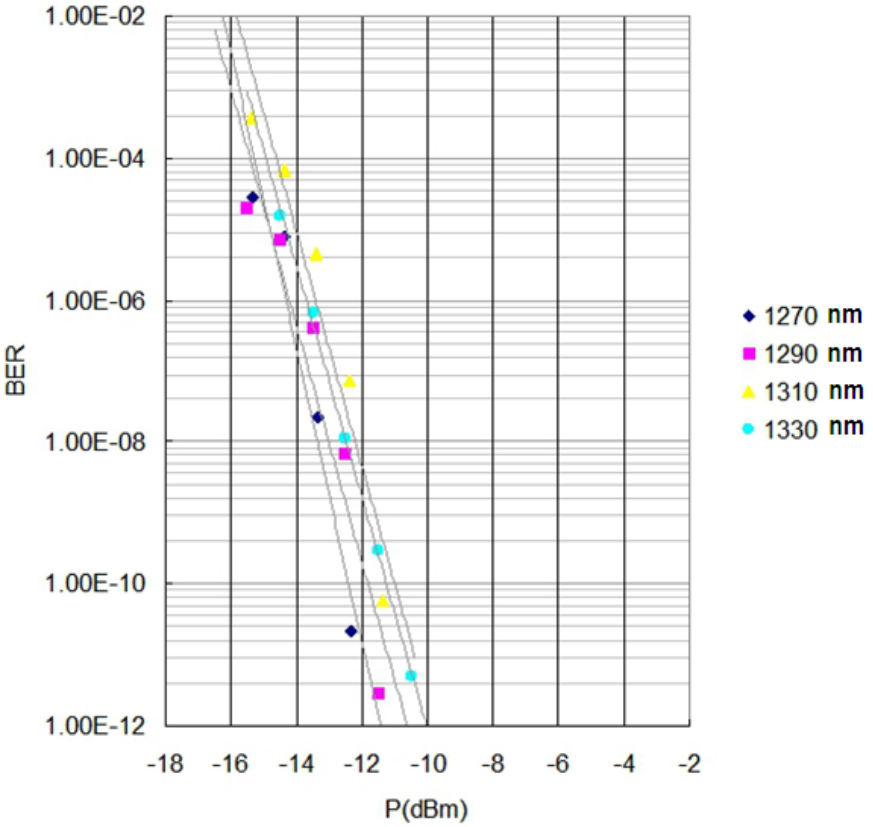
◆ Test results of DML+PIN scheme

DML Transmitter Eye Diagram(70℃)



OMA: 3.68dBm
ER: 4.64dB
Mask margin>14%

PIN Receiver Sensitivity (70℃)



sensitivity is about -10dBm

◆ Power Budget 10km, 8.5dB

Table 88–9—100GBASE–LR4 and 100GBASE–ER4 illustrative link power budgets

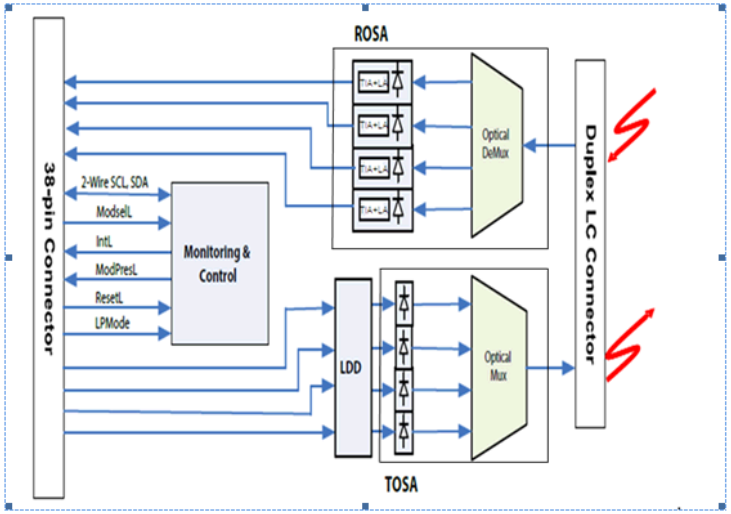
Parameter	100GBASE-LR4	Unit
Power budget (for maximum TDP)	8.5	dB
Power budget	—	dB
Operating distance	10	km
Channel insertion loss	6.3[b]	dB
Maximum discrete reflectance	–26	dB
Allocation for penalties[c] (for maximum TDP)	2.2	dB
Allocation for penalties[c]	—	
Additional insertion loss allowed	0	dB

- ✓ DML+PIN is good for 10km operation
- ✓ TOSA is compatible with SFP28 Package
- ✓ ROSA is compatible with SFP28 Package

The test results meet the requirements.
DML+PIN can be used to realize 25GBASE-L.

Cost

◆ 25G SFP vs 40G QSFP- BOM Costs



40G QSFP

BOM

	25G single lane PMDs	40G QSFP
BOM	25G LD TOSA	4×10G LD array
	25G PIN BOSA	4×10G PD array
	SFP package	MUX
		DEMUX
		QSFP package

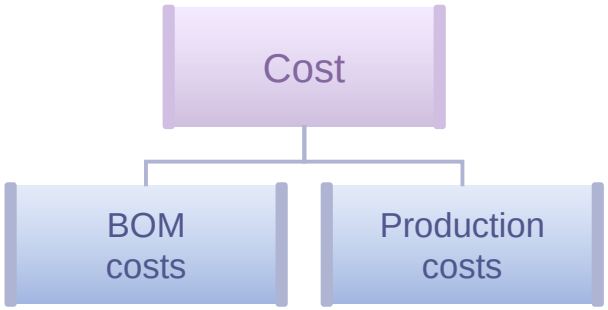
Compare the BOM costs:

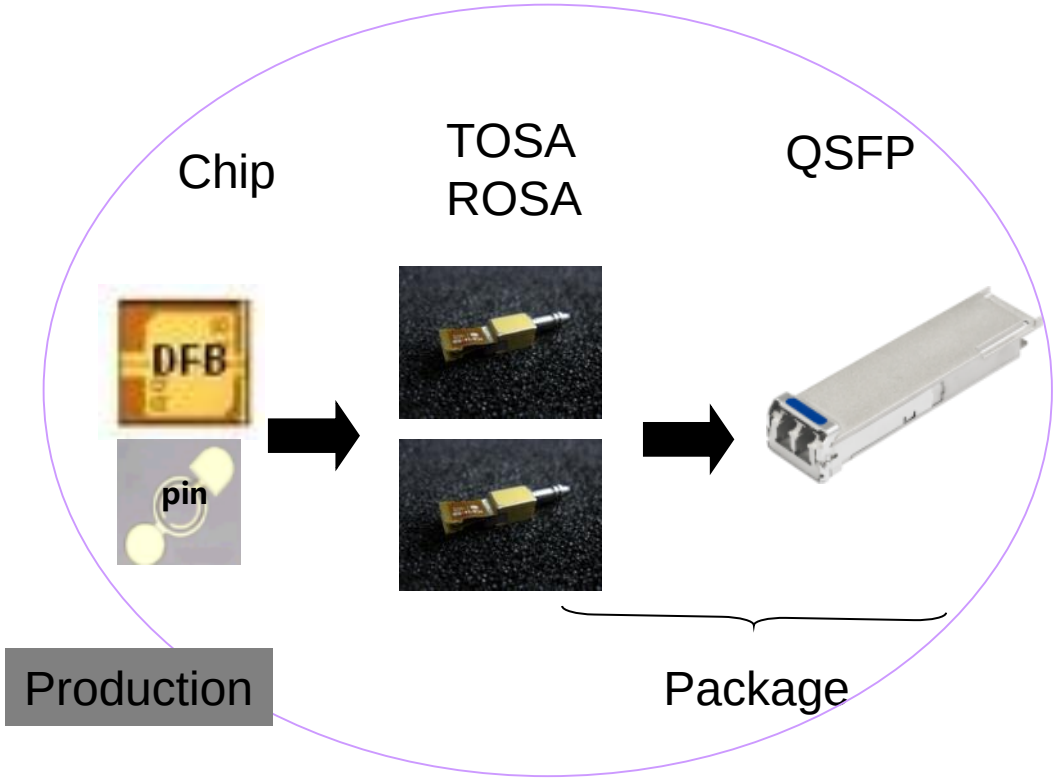
✓ The cost of single lane 25G chip is don't-know yet (can be higher)

✓ The structure of 40G QSFP Is more complex than 25G SFP.

This does not mean that the cost of 25G single lane SFP is lower than that of 40G QSFP. This is a bit pessimistic, and not the final conclusion.

◆ Production Costs





Cost of components = BOM costs + production costs

- ✓ Single channel packaging process is much easier than that of four channels.
- ✓ The Complexity of four channels result in much higher process cost and test cost than Single channel.

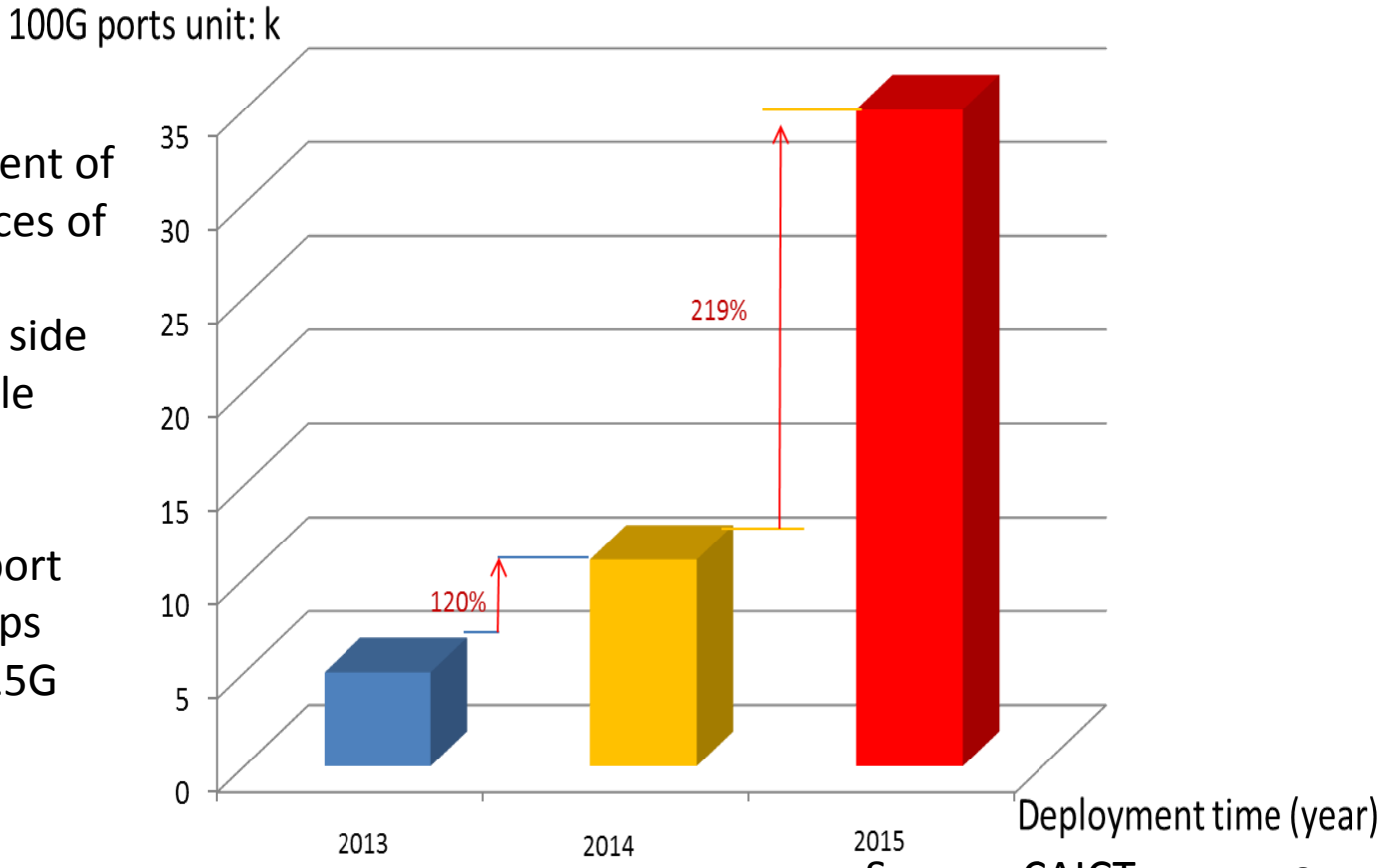
And the chip costs will be reduced as the product increases.

Potential of 25Gb/s

- The vigorous development and deployment of 100G will speed up the cost reduction of the 25G industry chain.

The chart is the deployment of 100Gb/s line side interfaces of China from 2013 to 2015.
The corresponding client side interfaces are mostly single mode 100GE too.

This 100GE single mode port numbers fast growing helps reducing the cost of the 25G industry chain.



Source: CAICT

Summary

- Single lane 25Gb/s 10km PMDs standard is needed.
- The cost of single lane 25Gb/s 10km PMDs is promising.

Thank You !