PI Balance Specifications

End-to-End Pair-to-Pair Ad Hoc

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Overview

- **Part 1: Further analysis of potential PI specifications**
  - **Error trends for PI P2PRunb specifications are presented**
  - **A spreadsheet is provided separately which can be used for further analysis of final worst case model results, which**
    - Allows user entry of
      - final worst case model effective resistances for specification derivations
      - And user entry of PI resistance ranges to test those specifications
    - Derived PI specifications are for:
      - Limits derived from the worst case E2E-P2PRunb Model
        - (Rmax < Rmin * TBDx + TBDy)
      - PI P2PRunb limits
- **Part 2: Proposed text is presented for PSE balance specifications**
  - **Effective resistance limits are bounded by the equation derived from E2E-P2PRunb (Rmax < Rmin * TBDx + TBDy)**
    - See http://www.ieee802.org/3/bt/public/jul14/bennett_01_0714.pdf
  - **Proposed PSE Balance specifications are composed of an effective resistance specification under section 33.1.4 and a current unbalance specification in table 33-11.**
    - The existing 802.3at rules for balance within a pair are likewise composed of a resistance balance specification in section 33.1.4, and a current unbalance specification in Table 33-11.

E2E P2PRunb vs PI P2PRunb

Trends noted from spreadsheet results:

Limits derived from E2E P2PRunb

Variable	Limit	Check	Compare
PSE Rmin	PSE Rmax	E2E P2PRunb	*PSE PI P2PRunb*
0.05	0.0535	0.2404	*0.0342*
0.1	0.1352	0.2404	*0.1496*
0.15	0.2168	0.2404	*0.1822*
0.2	0.2985	0.2404	*0.1976*
0.25	0.3801	0.2404	*0.2065*
0.3	0.4618	0.2404	*0.2124*
0.35	0.5435	0.2404	*0.2165*
0.4	0.6251	0.2404	*0.2196*
0.45	0.7068	0.2404	*0.2220*
0.5	0.7884	0.2404	*0.2238*
0.55	0.8701	0.2404	*0.2254*
0.6	0.9517	0.2404	*0.2267*
0.65	1.0334	0.2404	*0.2277*
0.7	1.1150	0.2404	*0.2287*
0.75	1.1967	0.2404	*0.2295*

PSE Nominal PI P2PRunb of 11.63% (from spreadsheet) is overly restrictive when total PSE PI resistances are higher

Limits based upon PI P2PRunb

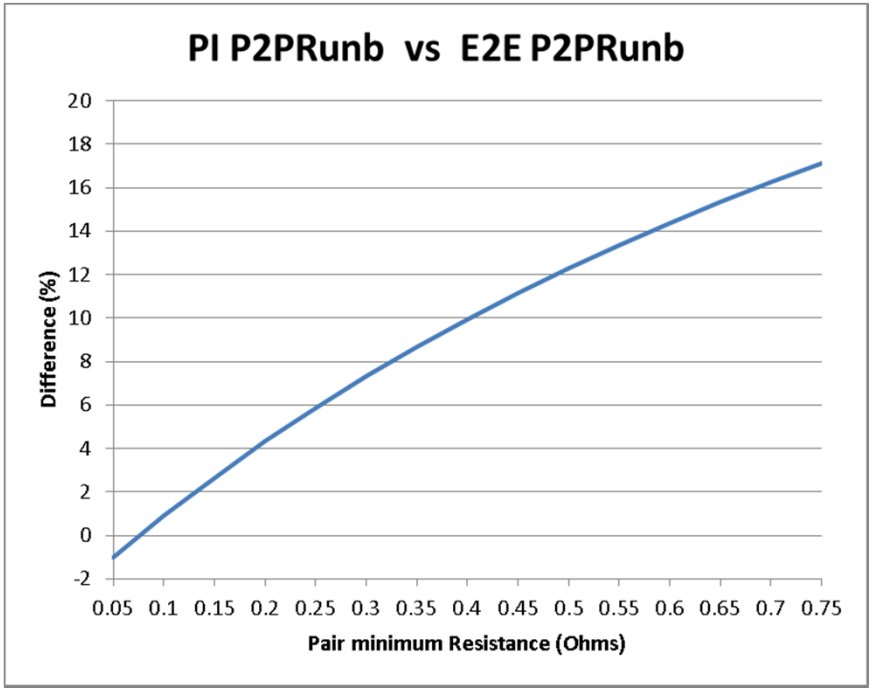
Variable	Limit	Compare	Check
PD Rmin	PD Rmax	E2E P2PRunb	*PD PI P2PRunb*
0.25	0.4384	0.1882	*0.2737*
0.5	0.8768	0.2195	*0.2737*
0.75	1.3151	0.2340	*0.2737*
1	1.7535	0.2424	*0.2737*
1.25	2.1919	0.2478	*0.2737*
1.5	2.6303	0.2517	*0.2737*
1.75	3.0687	0.2545	*0.2737*
2	3.5070	0.2567	*0.2737*
2.25	3.9454	0.2584	*0.2737*
2.5	4.3838	0.2599	*0.2737*
2.75	4.8222	0.2610	*0.2737*
3	5.2606	0.2620	*0.2737*
3.25	5.6989	0.2629	*0.2737*
3.5	6.1373	0.2636	*0.2737*
3.75	6.5757	0.2642	*0.2737*

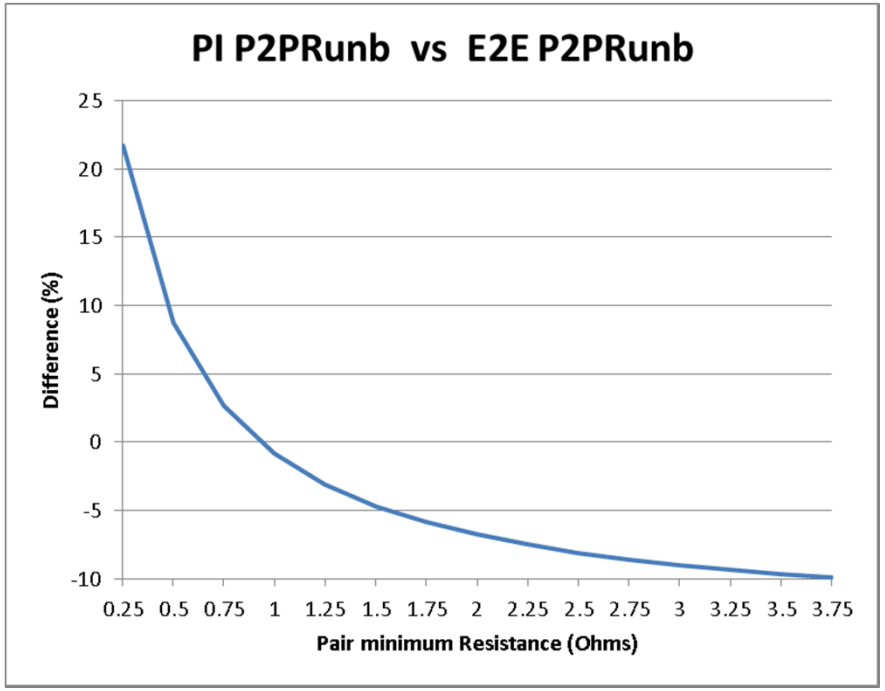
PDs meeting PI P2PRunb can FAIL worst case current unbalance when total PD PI resistances are higher

PI P2PRunb Specification effect on system balance

Positive percentages are more *restrictive* than necessary

Negative percentages can result in current unbalance *exceeding* target worst case





PSE and PD graphs resulting from the example provided in the spreadsheet

(Spreadsheet content is based upon ranges on a scale commensurate with worst case models)

Specification comparison

- **If the PI P2PRunb limit is *lower* than worst case (WC) E2E P2PRunb, which is likely to occur in the PSE PI:**
  - Low PI resistances may pass PI P2PRunb and exceed WC E2E P2PRunb
  - High PI resistances may fail PI P2PRunb and meet WC E2E P2PRunb
- **If the PI P2PRunb limit is *higher* than worst case E2E P2PRunb, which is likely to occur in the PD PI:**
  - Low PI resistances may fail PI P2PRunb and meet WC E2E P2PRunb
  - High PI resistances may pass PI P2PRunb and exceed WC E2E P2PRunb
- **If the specification is derived from worst case E2E P2PRunb:**

  (Rmax < Rmin * TBDx + TBDy)
  - Worst case E2E P2PRunb is not exceeded for any PI resistance range
  - The specification is implementation independent and least restrictive
- **Effective resistances (*Reff = V/I*) taken near maximum capacity are composed of active, passive resistances and voltage offsets**
  - No additional resistance or voltage balance specifications are necessary
  - One simple specification – No confusion about "Resistance Unbalance" conveying passive resistance (as precedence in standards suggest)

Proposed Balance Specification Baseline Text

Proposed base-line text (PSE Section):

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33.1.4.xx Type 3 and Type 4 PSE PI Requirement for Pair to Pair balance

4-pair operation requires that the effective resistances between twisted wire pairs of the same polarity conform to equation 33-1.XX:

$$Rpse\_max < Rpse\_min * TBDx + TBDy \qquad 33\text{-}1.XX$$

where Rpse_max and Rpse_min are maximum and minimum effective resistances determined at >85% of maximum port capacity. Each of the Rpse parameters is the common mode effective resistance in the path of a twisted wire pair, including all PSE elements that are exclusively in the path of that wire pair.

Optional, if deemed necessary to meet a desired current balance:
Additionally, Rpse_min shall be no less than TBD Ohms.

Pair to pair balance in a PI shall not change when powering other PIs in any mode within the PSE. In order to meet this requirement, it is recommended that twisted wire pairs of the same polarity be powered through paths from a common node which does not pass current to any other PI.

Any active current balancing method within the PSE which provides current balance meeting or exceeding the current unbalance specification (Iunb_ptp) in table 33-11 shall not be required to meet this specification.

Table 33.11 Parameter:

Table 33.11 Type 3 and Type 4 PSE PI Current Unbalance

Item #:	TBD
Parameter:	Pair-to-pair current unbalance
Symbol:	Iunb_ptp
Unit:	%
Min:	- -
Max:	TBD% *(From Worst Case E2E P2PRunb Models)*
Type:	3, 4
Additional Info:	See 33.2.x.x *(next slide)*

Table 33-11 Referenced Content:

33.2.x.x Pair-to-Pair Current Unbalance

Pair-to-Pair current unbalance is specified for 4-pair power by equation 33.x.x.x

$$I_{unb\_ptp} = (I_{max} - I_{min}) / (I_{max} + I_{min}) \qquad 33.x.x.x$$

Where I_{unb_ptp} is the current unbalance between pairs of the same polarity when 4-pair power is provided at >85% of maximum PSE port capacity. Imax, Imin is the maximum and minimum total current in each pair. I_{unb_ptp} is specified for unbalanced resistive loads defined in 33.x.x.y

$$R_{pair\_max} = TBD, \quad R_{pair\_min} = TBD \qquad 33.x.x.y$$

Where the pair resistances are common mode resistances in the wire pairs of the same polarity and are connected as shown in figure 33.x.x.z. The specification must be met with the unbalanced loads applied in either combination to wire pairs of the same polarity.

Table 33-11 Reference (Continued):

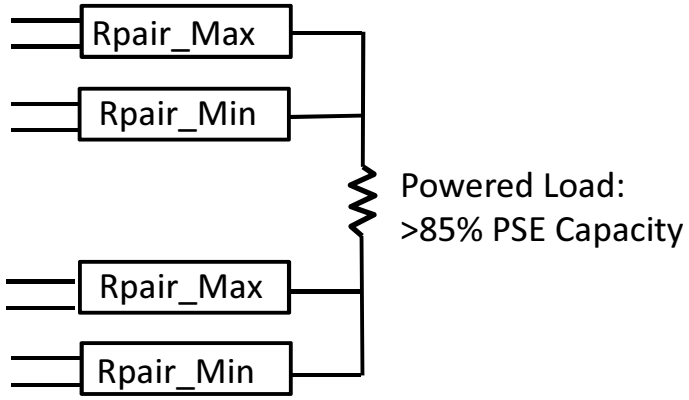

FIG. 33.x.x.z Unbalanced load configuration

Section 33.1.4.xx specifies effective PSE PI effective resistances that may alternatively be used to meet Pair-to-Pair current unbalance requirements when active current balancing is not implemented.

(Rpair_max and Rpair_min correspond to the effective resistances of the channel + PD from the worst case model, under >85% load conditions)