Add the text "See Annex 33-F for more details**" to:**

- after CC_DET_SEQ constant description in section 33.2.5.8, page 65, line 40
- into section 33.2.7.1 PSE 1-Event Physical Layer classification, page 97, line 30
- into section 33.2.7.2 PSE Multiple Event Physical Layer classification, page 97, line 51

Replace sentence "See Annex 33C for more information on Autoclass**" on page 101, line 8 to "**See Annex 33-C for more information on Autoclass operation and Annex 33-F for more information on Autoclass timing**"**

Annex 33-F

(Informative)

Sample Timing Diagrams

The following timing diagrams are provided for informative purposes only.

33F.1 Type 3 and Type 4 CC_DET_SEQ timing diagrams

Each of following sample timing diagrams show a PSE performing a sequence of connection check, detection, classification, power up and power on events. A PSE implements one or more of the four defined CC_DET_SEQ sequences based on the results of detection, connection check and 4PID.

33F.1.1 CC_DET_SEQ=0 timing diagrams

CC_DET_SEQ = 0 is the first of four possible connection check and detection sequences.

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=0 when the connection check result is single.

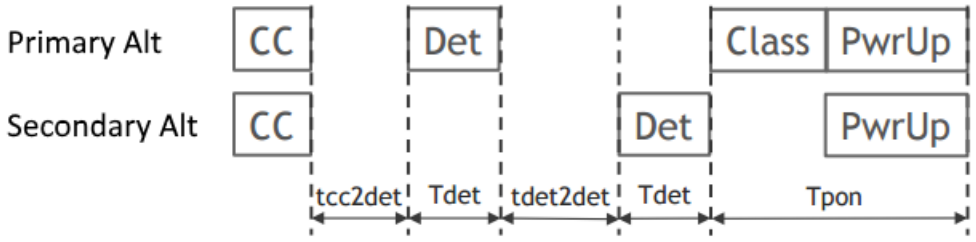

Figure 33F-1 – PSE implementing CC_DET_SEQ=0, do_cxn_chk result is single

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=0 when the connection check result is dual and Class_4PID_mult_events_sec is TRUE.

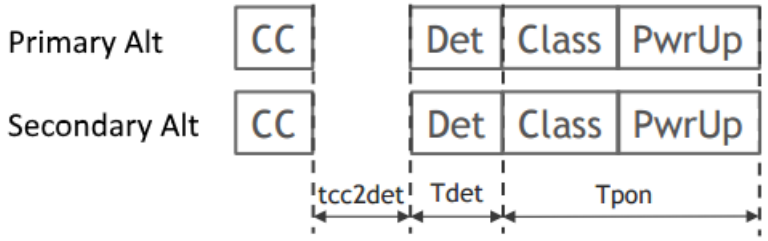

Figure 33F-2 – PSE implementing CC_DET_SEQ=0, do_cxn_chk result is dual, simultaneous power on

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=0 when the connection check result is dual and Class_4PID_mult_events_sec is FALSE.

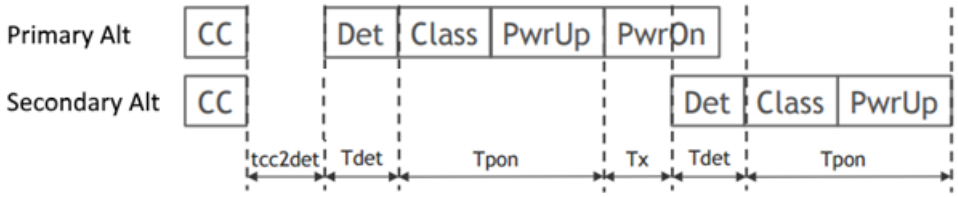

Figure 33F-3 – PSE implementing CC_DET_SEQ=0, do_cxn_chk result is dual, staggered power on

33F.1.2 CC_DET_SEQ=1 timing diagrams

CC_DET_SEQ = 1 is the second of four possible connection check and detection sequences.

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=1 when the connection check result is single.

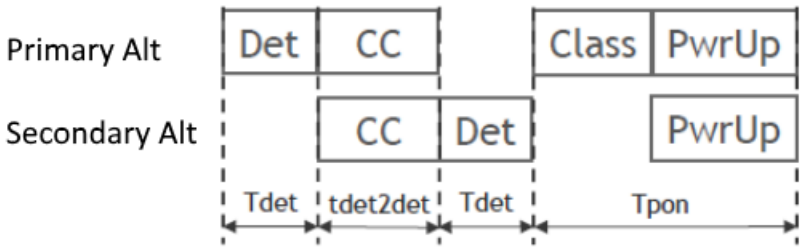

Figure 33F-4 – PSE implementing CC_DET_SEQ=1, do_cxn_chk result is single

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=1 when the connection check result is dual and Class_4PID_mult_events_sec is TRUE.

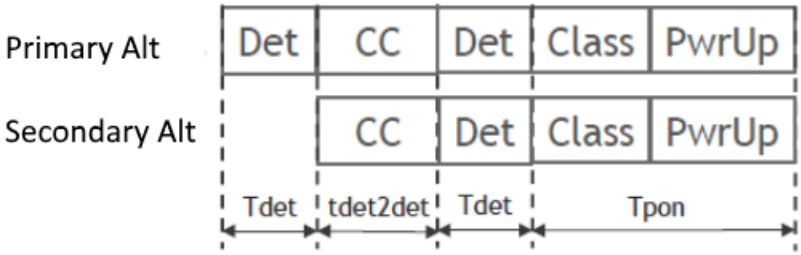

Figure 33F-5 – PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, simultaneous power on

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=1 when the connection check result is dual and Class_4PID_mult_events_sec is FALSE.

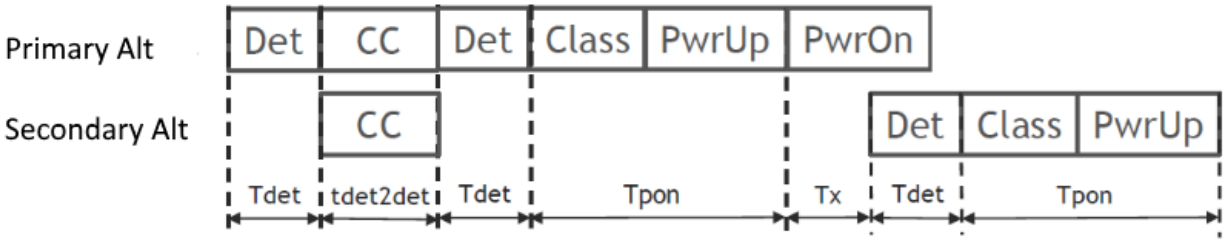

Figure 33F-6 – PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered power on

33F.1.3 CC_DET_SEQ=2 timing diagrams

CC_DET_SEQ = 2 is the third of four possible connection check and detection sequences.

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=2 when the connection check result is single.

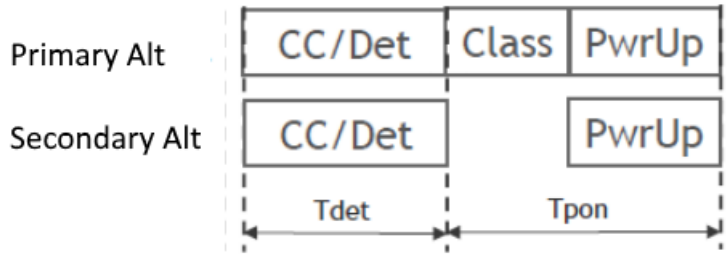

Figure 33F-7 – PSE implementing CC_DET_SEQ=2, do_cxn_chk result is single

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=2 when the connection check result is dual and PD_4pair_cand is initially TRUE.

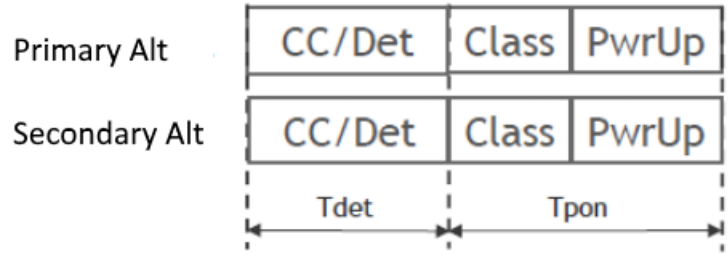

Figure 33F-8 – PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, simultaneous power on

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=2 when the connection check result is dual and PD_4pair_cand is initially FALSE.

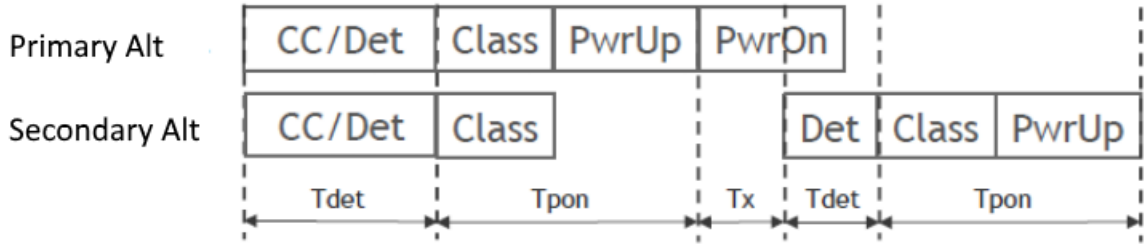

Figure 33F-9 – PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, staggered power on

33F.1.4 CC_DET_SEQ=3 timing diagrams

CC_DET_SEQ = 3 is the fourth of four possible connection check and detection sequences.

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=3 when the connection check result is single.

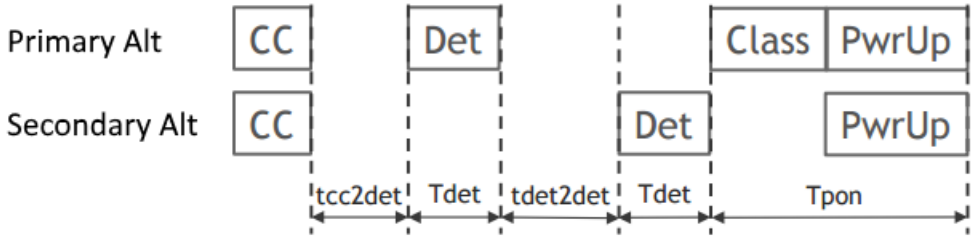

Figure 33F-10 – PSE implementing CC_DET_SEQ=3, do_cxn_chk result is single

The following timing diagram illustrates a PSE implementing CC_DET_SEQ=3 when the connection check result is dual.

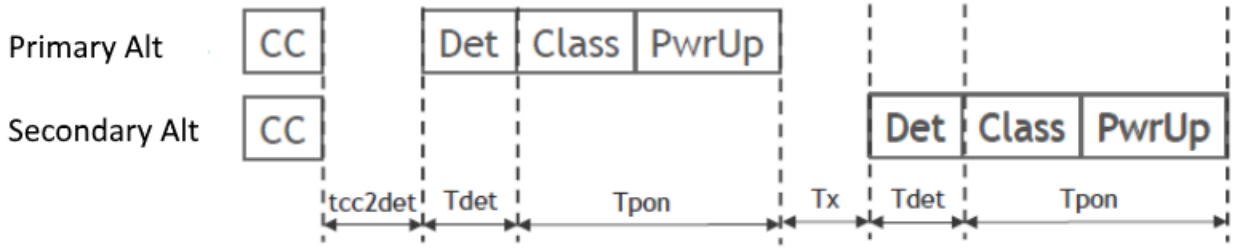

Figure 33F-11 – PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual

33F.2 PSE Single-Event Physical Layer classification timing diagram

The following sample timing diagram shows a PSE performing a Single-Event Physical Layer classification. No timing relationship between the first class event and the subsequent power on is shown or implied. After T_{CLE1} the PSE may transition directly to the power on voltage.

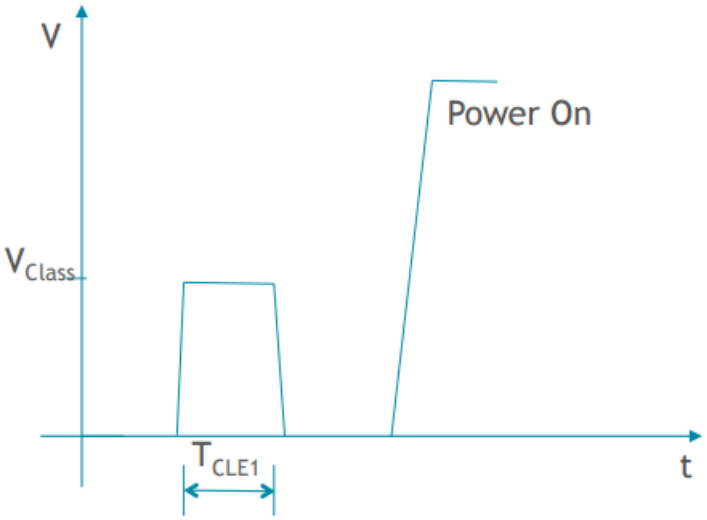

Figure 33F-12 - PSE Single-Event Physical Layer classification

33F.3 PSE Multiple-Event Physical Layer classification timing diagram

The following sample timing diagram shows a Type 2 PSE performing a Multiple-Event Physical Layer classification with a Class 4 PD.

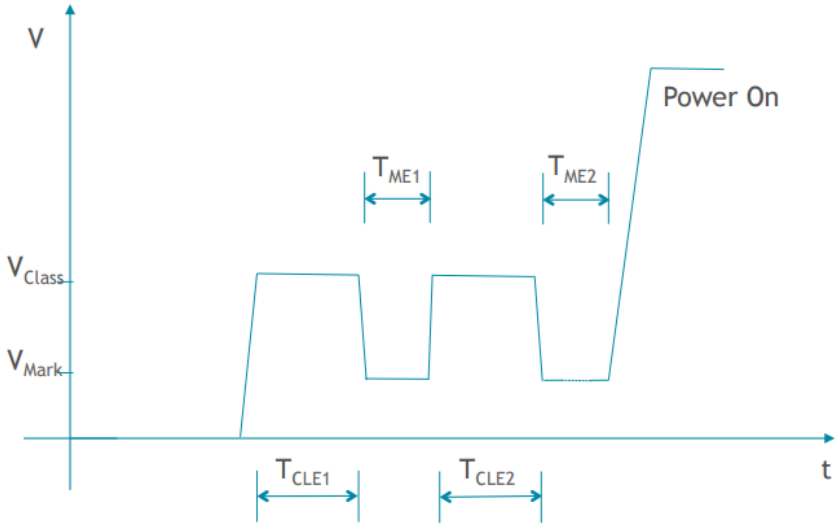

Figure 33F-13 - Type 2 PSE – Class 4 PD

The following sample timing diagram shows a Type 4 PSE performing a Multiple-Event Physical Layer classification with a Class 8 PD. Autoclass is not shown in the following timing diagram.

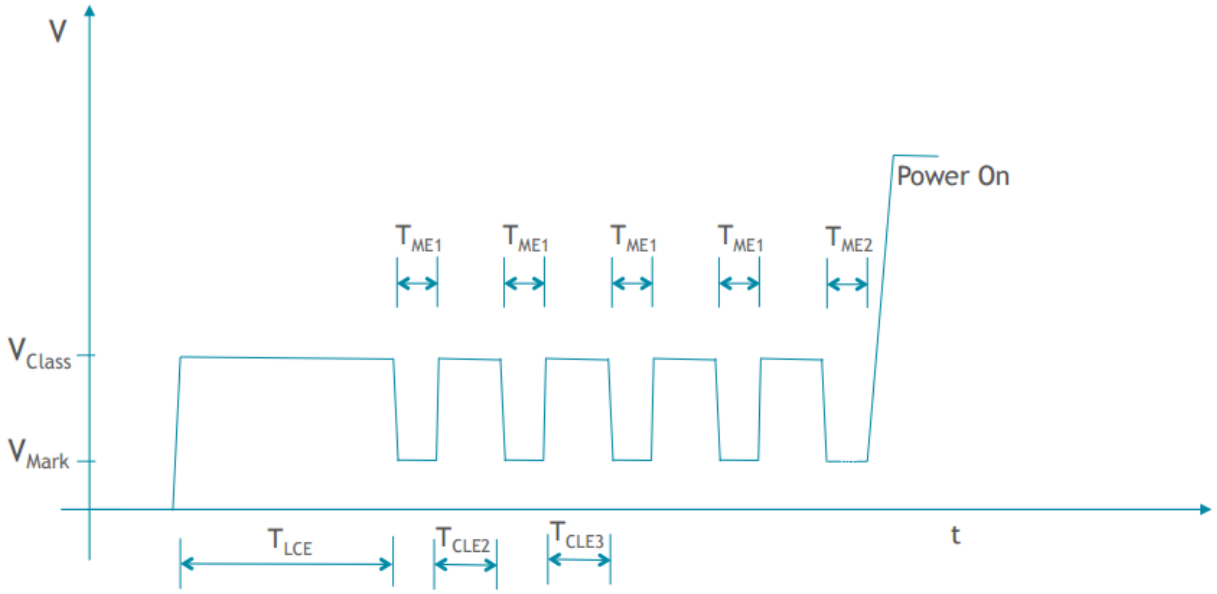

Figure 33F-14 - Type 4 PSE – Class 8 PD – no autoclass

33F.4 Autoclass timing diagram

The following sample timing diagram shows a Type 3 or Type 4 PSE performing Multiple-Event Physical Layer classification with autoclass enabled. The autoclass-enabled PD responds by requesting an autoclass measurement.

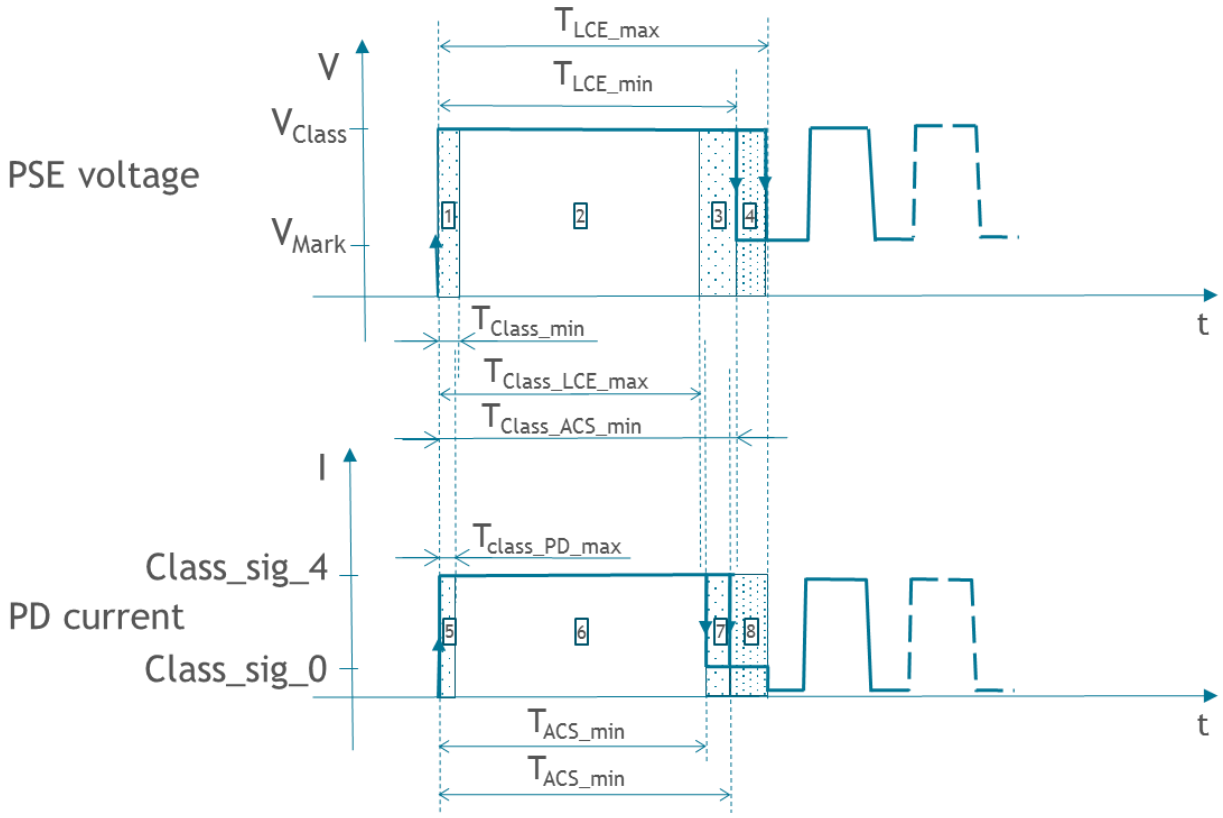

Figure 33F-15 - Type 3 or Type 4 PSE and PD autoclass example