
# Backfeed Adhoc

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# Backfeed voltage

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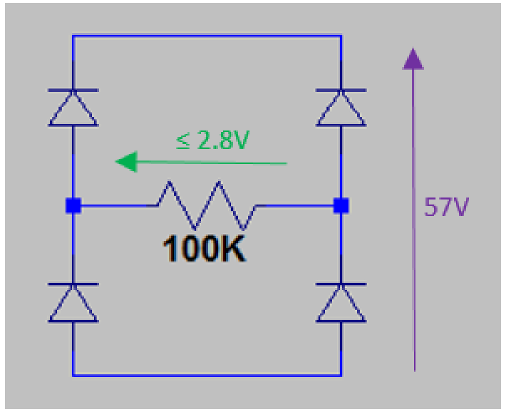
# Backfeed voltage … a closer look (single-signature PD)

## Existing IEEE Std 802.3-2015 :

When $V_{Port\_PD}$ max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected shall not exceed $V_{bfd}$ max as specified in Table 33–18. When $V_{Port\_PD}$ max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected shall not exceed $V_{bfd}$ max.



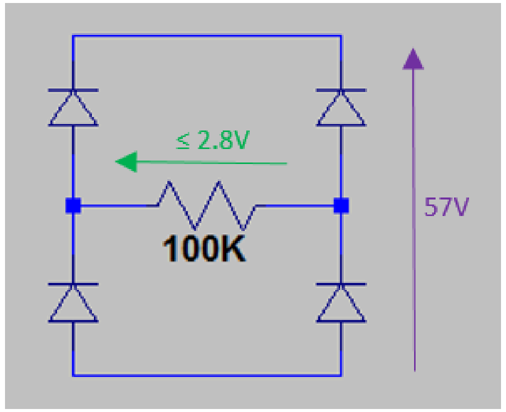

## P802.3bt D3.4 :

When any voltage in the range of 0 V to $V_{Port\_PD-2P}$ max is applied across the PI at either polarity specified on the conductors of either Mode A or Mode B according to Table 145–20, the voltage measured across the PI for the other Mode with a 100 kΩ load resistor connected across that other Mode shall not exceed $V_{bfd}$ as defined in Table 145–29.

# Backfeed voltage … a closer look (single-signature PD)

## Existing IEEE Std 802.3-2015 :

When $V_{Port\_PD}$ max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected shall not exceed $V_{bfd}$ max as specified in Table 33–18. When $V_{Port\_PD}$ max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected shall not exceed $V_{bfd}$ max.




## Yseboodt_01_0518_backfeed_baseline:

For a single-signature PD, when any voltage in the range of 0 V to $V_{Port\_PD-2P}$ max is applied per any of the valid 2-pair configurations, defined in Table 145–20, that have only a single pair connected to positive $V_{PSE}$ (see Figure 145–29a), the voltage on the Mode not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed $V_{refl}$ as defined in Table 145–29.

# Schottky Power Rectifier MBRA160

The temperature of the diode bridge on the unpowered pairset will be close to the lead temperature of the diodes conducting the current on the powered pairset.

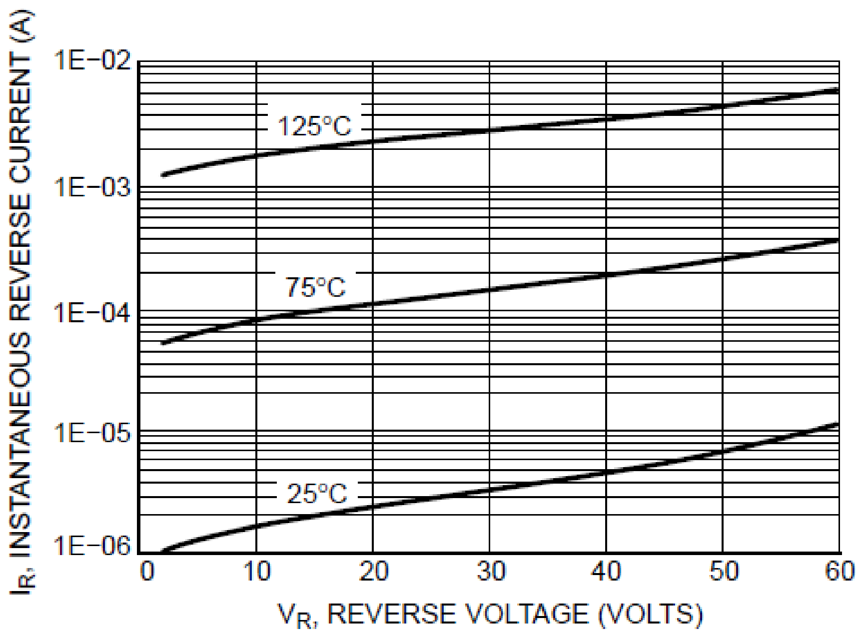
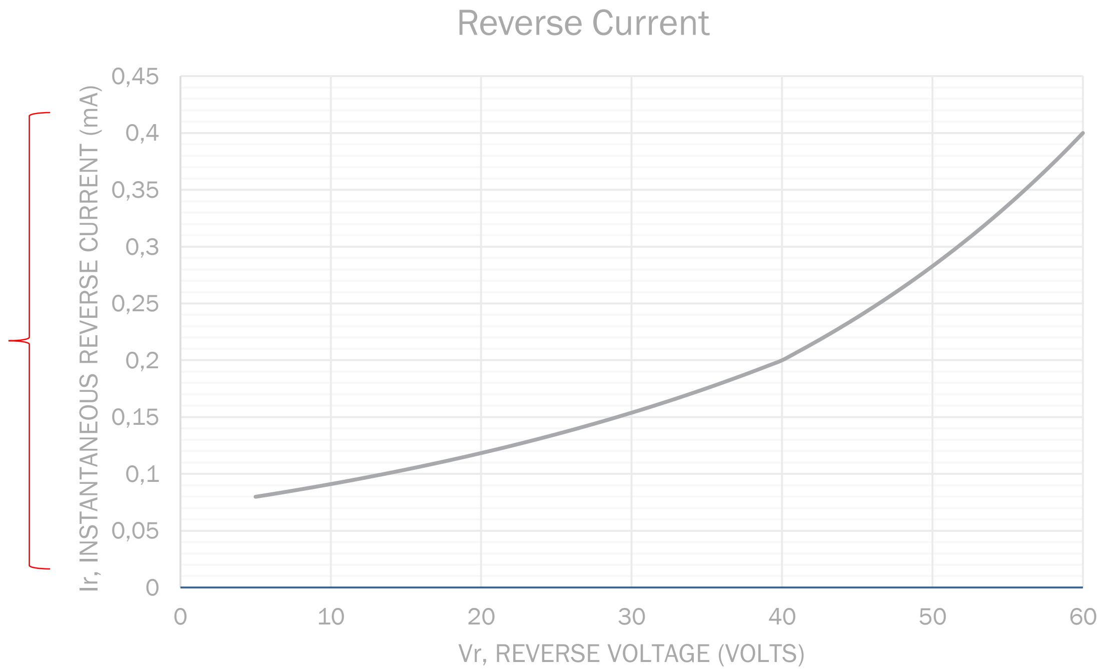


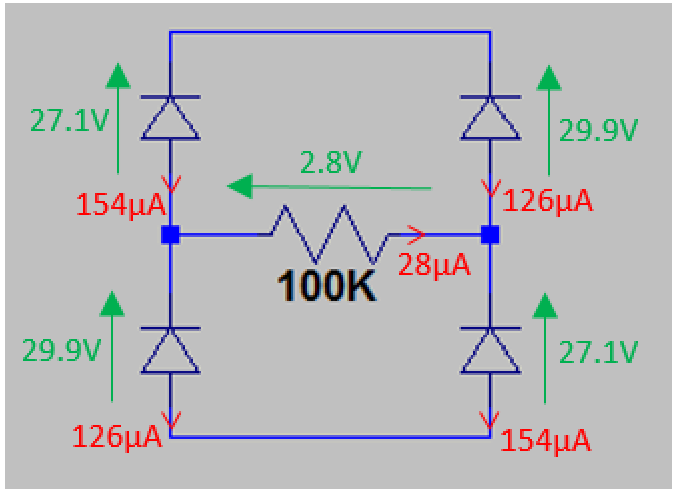

**Figure 3. Typical Reverse Current**

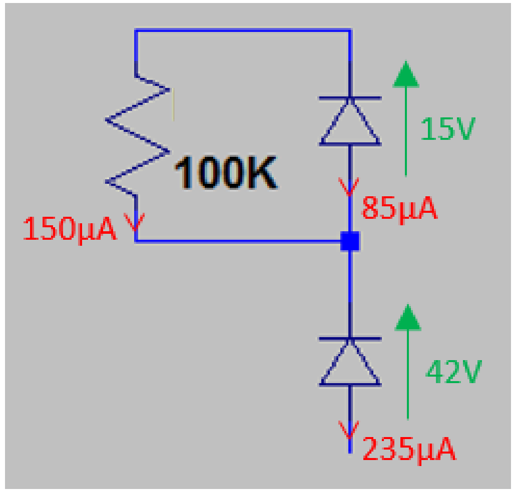



A lead temperature around 65°C corresponds to a common operating condition (the same temperature is used to specify the max cable DCR – see 145C.3)

# Backfeed voltage … a closer look (single-signature PD)

When extending the existing ‘symmetrical’ backfeed voltage specification to an ‘asymmetrical’ 3P reflected voltage specification, a significantly larger reflected voltage value can be expected even with PDs using real diode bridges.




Moreover when introducing a backfeed/reflected current specification and furthermore reducing the 100kΩ down to 0 Ω, much larger backfeed/reflected currents than 28µA (2.8V/100kΩ) can be expected (e.g. 360µA@57V).

# Backfeed voltage

Backfeed Voltage as specified in the past and today (P802.3bt D3.4) seems only to prevent significant power dissipation or damage on a pairset not capable of transferring power.

Extending the backfeed voltage specification from a pairset not capable of transferring power to a pairset capable of transferring power but that’s not powered up (yet) in a 3P configuration, introduces the risk to make even PDs that use real diode bridges non-compliant.


# Reflected voltage

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# Reflected voltage during 3P detection (single-signature PD)

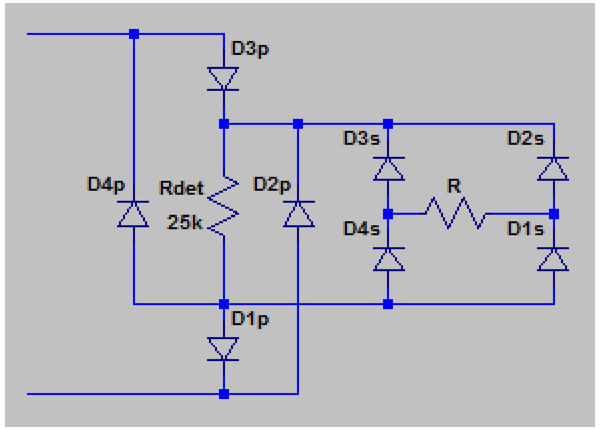
We are on the path to introduce a new requirement for 3P detection (Yseboodt_01_0518_backfeed_baseline):

For a single-signature PD, when any voltage in the range of 0 V to 10.1 V is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive $V_{PSE}$ (see Figure 145–29a and Figure 145–29b), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed $V_{refl}$ as defined in Table 145–29.

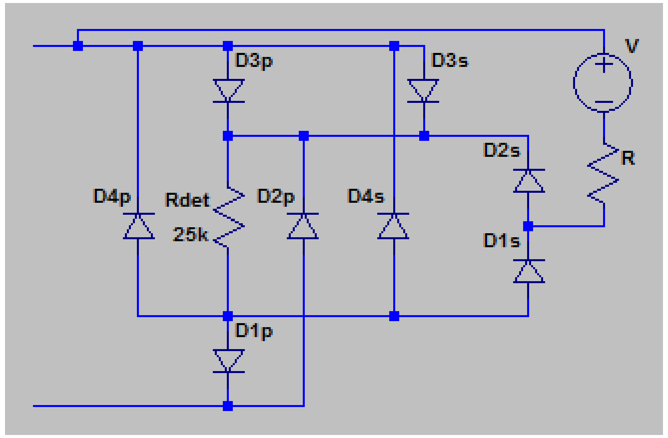
We should be careful not to introduce any new issues or to be too strict and making solutions non-compliant without reason.

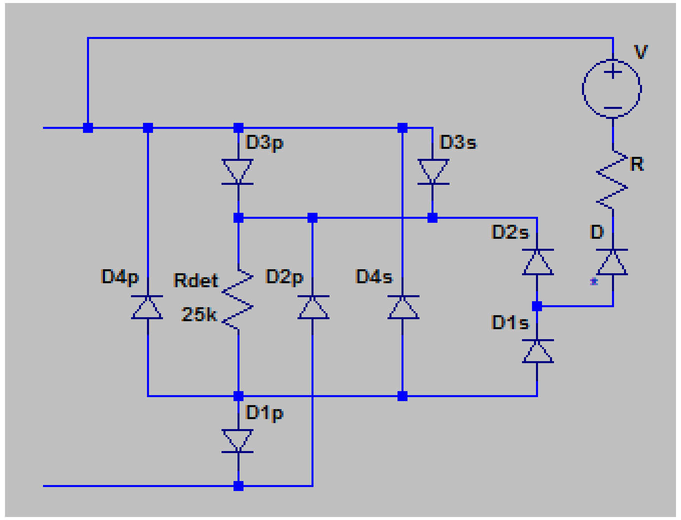
# Reflected voltage during 3P detection (single-signature PD)

When extending the existing 'symmetrical' detection specifications to an 'asymmetrical' 3P detection specification, again things are different:




vs




The 2P overall schematic (on the left) versus the new 3P overall schematic(s) (on the right).

The Schottky diode DC leakage current is usually overlooked !

What should be the V, R and (optional?) D for the other mode of the "3P PSE" ?

(... if any combination is possible anyhow allowing a "3P PSE")

# Reflected voltage during 3P detection (single-signature PD)

Will this new text (in Yseboodt_01_0518_backfeed_baseline) not create unnecessary new issues like making (schottky) diode bridges non-compliant:

For a single-signature PD, when any voltage in the range of 0 V to 10.1 V is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive $V_{PSE}$ (see Figure 145–29a and Figure 145–29b), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed $V_{refl}$ as defined in Table 145–29.

This text would then cover the case V=0, R=100k and no diode.

This text would then basically become a requirement for diode D1s:

its DC leakage current should be below **28uA** for a 7V reverse voltage.

Is this really required to meet 3P detection? (Overall, detection has to do with a current difference for a 1V voltage difference.)

Also, how would this relate to the **1.3mA** Irefl requirement for the PSE ?

# Reflected voltage during 3P detection (single-signature PD)

Rather then including this requirement in the Reflected voltage section,

For a single-signature PD, when any voltage in the range of 0 V to 10.1 V is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive $V_{PSE}$ (see Figure 145–29a and Figure 145–29b), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed $V_{refl}$ as defined in Table 145–29.

shouldn't we rather look at what really matters for 3P detection and include the test requirements for this in the PSE section 145.2.6 (**PSE detection of PDs**) and PD sections 145.3.4 (**PD valid and non-valid detection signatures**) and 145.3.5 (**PD signature configurations**)?

Let's not forget or neglect the Schottky diode DC leakage current !