Insert new subclause 145.5.3.7.0a below 145.5.3.7 as follows:

145.5.3.7.0a Mode designation

Dual-signature PDs are implemented on Mode A and Mode B as defined in 145.3.2. Mode information is obtained by replacing the X in the desired variable or function with the letter of the Mode of interest. Modes are referred to in general as follows:

X

Generic Mode designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.
Values:
A: Mode A
B: Mode B

P

Powered Mode designator. When P is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams. "P" refers to the Mode that is currently powered. It's value is only defined when the PD is powered over 2-pair.
Values:
A: Mode A
B: Mode B

145.5.3.7.2 Variables

Info (not part of baseline)

We are using the shorthands 'twopairmode' and 'fourpairmode' in the PD state diagrams. These are defined below. Note that the $\wedge$ symbol denotes boolean XOR as defined in 21.5.4. Unlike for the PSE there is no easy method to derive if a Mode is powered. The best method is to check that present_mps_mode(X) is set to TRUE to determine if a Mode is powered.

Add the variable / alias to the variable list as follows:

- twopairmode: Alias for the following term: (present_mps_mode(A) $\wedge$ present_mps_mode(B))
- fourpairmode: Alias for the following term: (present_mps_mode(A) * present_mps_mode(B))

Add the PD_REQUESTED_VALUE_mode(X) variable to the variable list as follows:

PD_REQUESTED_VALUE_mode(X)

The value of this variable is used by the dual-signature to indicate the amount of power it requires on Mode A and Mode B, while it is being powered in 2-pair mode.
Values: 1 through 499

Info (not part of baseline)

There are a bunch of statements "When a PD mode is not active, the value is set to zero." and "When a PD mode is not active, the value shall be set to zero." that do not belong in the variable section.

Remove the following statements from 145.5.3.7.2:

- When a PD mode is not active, the value is set to zero.
- When a PD mode is not active, the value shall be set to zero.

145.5.3.7.4 State diagrams

Change Figure 145–44 as follows:

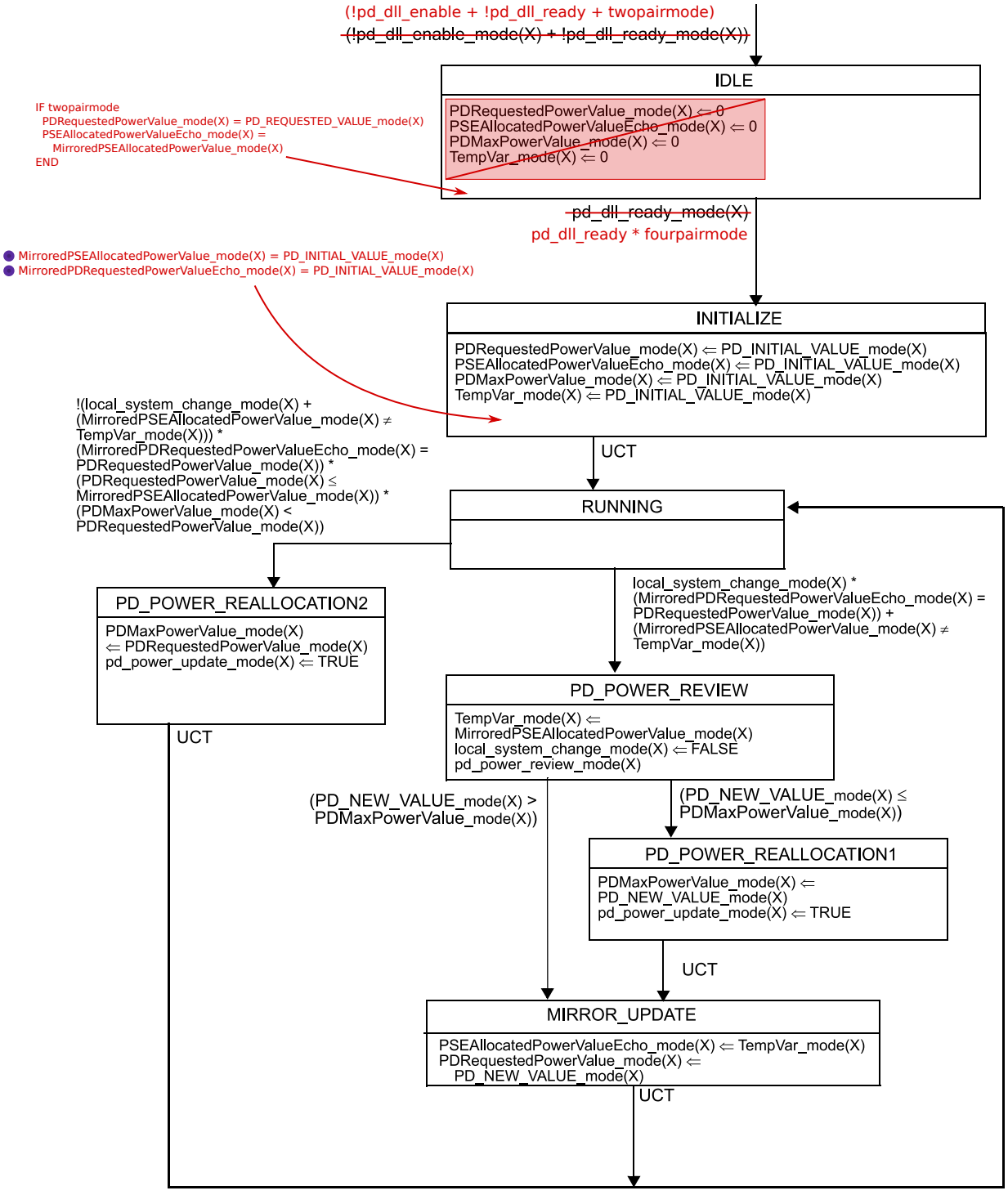

Figure 145–44—Dual-signature PD power control state diagram for 4-pair mode

Insert Figure 145–44a as follows:

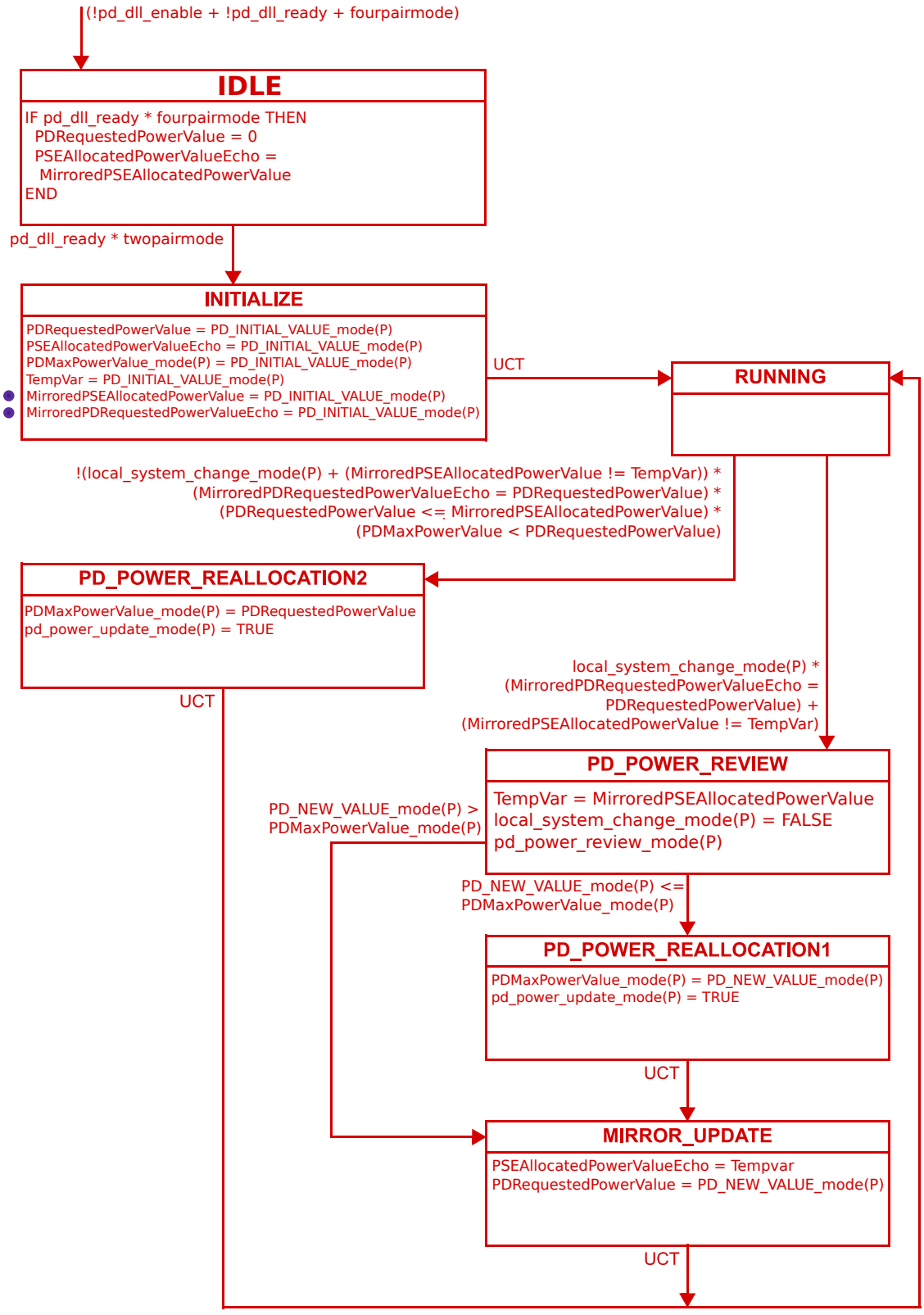

Figure 145-44a --- Dual-signature PD power control state diagram for 2-pair mode

145.5.5 State change procedure across a link (dual-signature)

Add new subclause under 145.5.5 as follows:

145.5.5.1a Transitions between 2-pair and 4-pair mode (dual-signature)

When a PSE, connected to a dual-signature PD, transitions from 4-pair to 2-pair operation, it shall assign the value of PSEAllocatedPowerValue_alt(X), where X is the powered Alternative, to PSEAllocatedPowerValue. The purpose of this is that the PD can continue operating over the remaining powered Mode.
When a PSE, connected to a dual-signature PD, transitions from 2-pair to 4-pair operation, it shall assign the value of PSEAllocatedPowerValue to PSEAllocatedPowerValue_alt(X), where X is the Alternative that was initially powered.
A dual-signature PD that is switched from 4-pair to 2-pair mode requests the amount of power it needs for 2-pair operation in the PDRequestedPowerValue variable. Per Table 145–42 this is the requested power for the active Mode.

79.3.2 Power via MDI TLV

. . .

The Power via MDI TLV shown in Figure 79–3 was originally defined in IEEE Std 802.1AB-2005 Annex G.3. This original TLV only supported the first three fields of Figure 79–3, labeled basic fields, enabling discovery and advertisement of Power via MDI capabilities. The Power via MDI TLV was revised by IEEE Std 802.3at-2009 to add a further three fields, labeled DLL classification extension, to provide Data Link Layer (DLL) classification capabilities. The Power via MDI TLV was revised again by IEEE Std 802.3bt-201x to add a further nine fields, labeled Type 3 and Type 4 extension to support additional capabilities offered by Type 3 and Type 4 PSEs and PDs.

~~Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension.~~

. . .

Append to the following paragraph as follows:

If a Type 1 or Type 2 power entity implements Data Link Layer classification, it shall support the Power Via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered. If a Type 3 or Type 4 power entity implements Data Link Layer classification, it shall support both the DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Type 1 and Type 2 devices shall not include the Type 3 and Type 4 extension fields in transmitted LLDPDU's.

Info (not part of baseline)

Out of all the fields and bits in the “Type 3 and Type 4 extensions”, there is one bit that is specifically intended for Type 1 and Type 2 PDs. The PD 4PID bit allows such a PD to assert that it is 4-pair capable. By having this bit in the “Type 3 and Type 4 extensions” fields, we open up Pandora’s box of having the define ALL of the fields for Type 1 and Type 2 devices.

The proposed solution is to move this bit into a reserved bit of the existing fields. That way, the “Type 3 and Type 4 extensions” can be restricted to Type 3 and Type 4 devices only.

79.3.2.4.1 Power type

Move the PD 4PID bit from Table 79–6d (System setup field) to bit position 2 in Table 79-4 (Power type/source/priority field) as follows:

Table 79–6d—System setup field

Bit	Function	Value/meaning
7:6	Reserved	Transmit as zero. Ignore on receive.
5:2	Power typex	5 4 3 2 1 1 1 1 = Type 4 dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Type 3 dual-signature PD 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Type 4 single-signature PD 1 0 0 0 = Type 4 PSE 0 1 1 1 = Type 3 single-signature PD 0 1 1 0 = Type 3 PSE 0 1 0 1 = Type 2 PD 0 1 0 0 = Type 2 PSE 0 0 1 1 = Type 1 PD 0 0 1 0 = Type 1 PSE 0 0 0 1 = Reserved/Ignore 0 0 0 0 = Reserved/Ignore
1	PD 4PID	1 = PD supports powering of both Modes simultaneously 0 = PD does not support powering of both Modes simultaneously
0	PD Load	1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated. 0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.

Move PD 4PID

Table 79–4—Power type/source/priority field

Bit	Function	Value/meaning
7:6	power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	power source	Where power type = PD 5 4 1 1 = PSE and local 1 0 = Reserved 0 1 = PSE 0 0 = Unknown Where power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3:2	Reserved	Transmit as zero, ignore on receive
1:0	power priority	1 0 1 1 = low priority PD 1 0 = high priority PD 0 1 = critical priority PD 0 0 = priority unknown (default)

Move 4PID to bit 2

Info (not part of baseline)

Restore sections on PD requested power and PSE allocated power. The new subclause in Clause 145 above will deal with what needs to be filled out in particular circumstances.

79.3.2.5 PD requested power value

Info (not part of baseline)

We have now changed this legacy field to include 0 as a valid value. For Type 1/2 this was an illegal value, which now becomes a legal value, which leads to undefined behavior if used. This would not be a problem, were it not that Clause 33, by mistake, allows the value 0 in the variable that is linked to this field. We will need to file an MR to change the DLL state diagram in Clause 33, to restrict the value PDRequestedPowerValue from 1 through 255. Both changes together do not result in a change in legacy requirements.

Replace content above the dashed line with content below the dashed line as follows:

The PD requested power value field shall contain the PDs requested power value defined in Table 79–5, for Type 1, Type 2, and single-signature Type 3 and Type 4 PDs. The fields for PD requested power value shall be set to the sum of PD requested power value Mode A and PD requested power value Mode B in Table 79–6a, for Type 3 and Type 4 dual-signature PDs.

The PD requested power value field shall contain the PDs requested power value defined in Table 79–5.

Change Table 79–5 as follows:

Table 79–5 — PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~+~~ 0 through ~~255~~ 999.

79.3.2.6 PSE allocated power value

Info (not part of baseline)

We have now changed this legacy field to include 0 as a valid value. For Type 1/2 this was an illegal value, which now becomes a legal value, which leads to undefined behavior if used. This would not be a problem, were it not that Clause 33, by mistake, allows the value 0 in the variable that is linked to this field. We will need to file an MR to change the DLL state diagram in Clause 33, to restrict the value PSEAllocatedPowerValue from 1 through 255. Both changes together do not result in a change in legacy requirements.

Replace content above the dashed line with content below the dashed line as follows:

The PSE allocated power value field shall contain the PSE's allocated power value defined in Table 79–6 for PSEs connected to single-signature PDs and Type 1 and Type 2 PDs.

The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field, as defined in Table 79–6a, shall be provided in the PSE allocated power value field for Type 3 and Type 4 PSEs connected to a dual-signature PD. The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field may be provided in the PSE allocated power value field for Type 1 and Type 2 PSEs when connected to a dual-signature PD.

The PSE allocated power value field shall contain the PSEs allocated power value defined in Table 79–6.

Change Table 79–6 as follows:

Table 79–6 — PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through ~~255~~ 999.

79.3.2.6a Dual-signature PD requested power value Mode A and Mode B

The "Dual-signature PD requested power value Mode A and Mode B" fields shall contain the PD requested power value defined in Table 79–6a and Table 79–6aa for Mode A and for Mode B of a dual-signature PD.

~~If Mode (X) is non-active while the other mode is active, the inactive PD requested power value Mode (X) field value shall be set to 0.~~

~~Single-signature PDs shall set the PD requested power value Mode A and Mode B fields to 0.~~

"Dual-signature PD requested power value Mode A" and "Dual-signature PD requested power value Mode B" are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

Info (not part of baseline)

Each field has its own Table in Clause 79. Table 79–6a and 79–6b are the only exception where two fields share a Table. I'm splitting them into two Tables to be consistent.

Change Table 79–6a as follows and create new Table 79–6aa:

Table 79–6a — Dual-signature PD requested power value field for Mode A

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through 499.

Table 79–6aa — Dual-signature PD requested power value field for Mode B

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through 499.

79.3.2.6b PSE allocated power value Alternative A and Alternative B

The "PSE allocated power value Alternative A field" and the "PSE allocated power value Alternative B" field shall contain the values in Table 79–6b and Table 79–6ba. ~~for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.~~

Change Table 79–6b as follows and create new Table 79–6ba:

Table 79–6b — PSE allocated power value field for Alternative A

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through 499.

Table 79–6ba — PSE allocated power value field for Alternative B

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal + 0 through 499.

Move the paragraph below (with changes) to above Table 79–6b in this subclause.

The "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives, when the PSE provides power over 4-pair. ~~"PSE allocated power value Alternative A" and "PSE allocated power value Alternative B"~~ These fields are the power levels at the dual-signature PD PI. The PSE uses ~~this value~~ these values to compute $P_{Class\text{-}2P}$ as defined in 145.2.7. ~~A PSE providing power to a Type 1, Type 2, or single-signature Type 3 or Type 4 PD, places 0 in the "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields defined in Table 79–6b.~~

79.3.2.6e PSE maximum available power

The PSE maximum available power field shall contain the highest power the PSE can grant as defined in Table 79–6e. The PSE shall set the value of this field taking available power budget and hardware capabilities into account. For dual-signature PDs this value refers to the total amount of power available at the PI, even though power is allocated separately on a per pairset basis.

79.4.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

Info (not part of baseline)

This addresses comment i-319 against D3.0

Add to Table 79–9 as follows:

TLV name	TLV variable	LLDP Local System Group managed object class attribute
Power via MDI	Dual-signature power Classx Mode A	aLldpXdot3LocPowerClassxA
	Dual-signature power Classx Mode B	aLldpXdot3LocPowerClassxB

Add to Table 79–10 as follows:

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
Power via MDI	Dual-signature power Classx Mode A	aLldpXdot3RemPowerClassxA
	Dual-signature power Classx Mode B	aLldpXdot3RemPowerClassxB