

# CU4HDD Backplane Channel Analysis

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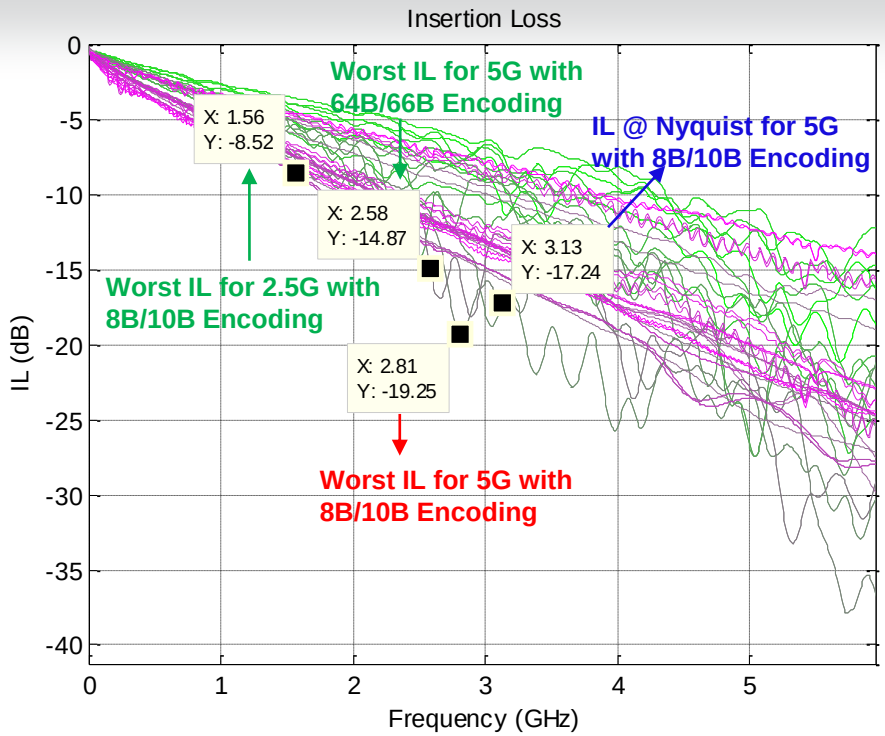
# Outline

- Analysis of 54 SAS backplane channels (www.t10.org)
  - Channels are from connector to connector (TP1 <-> TP4)
  - IL - Insertion loss
  - ICR ( Insertion loss to crosstalk ratio )
- Simulation results using COM model ( Annex 93A 802.3bj with updated configurations)
- Simulation results with Stateye V4.2.3
- Performance analysis for PCS coding and equalizations
  - PCS coding: 8B/10B vs. 64B/66B encoding
  - TX EQ– 3 tap TX FIR

# COM – Channel Operating Margin ( Annex 93A) – Simulation Configurations

- 2.5G-BASE-X – 8B/10B
  - Baud rate: 3.125G.
  - TX EQ: No
  - DFE: No
- 5G BASE-X –8B/10B
  - Baud rate: 6.25G
  - With/Without: TX EQ of 3-Tap FIR
  - DFE: 6-Tap
- 5G BASE-R –64B/66B
  - Baud rate: 5.15625G
  - With/Without: TX EQ of 3-Tap FIR
  - DFE: 6-Tap

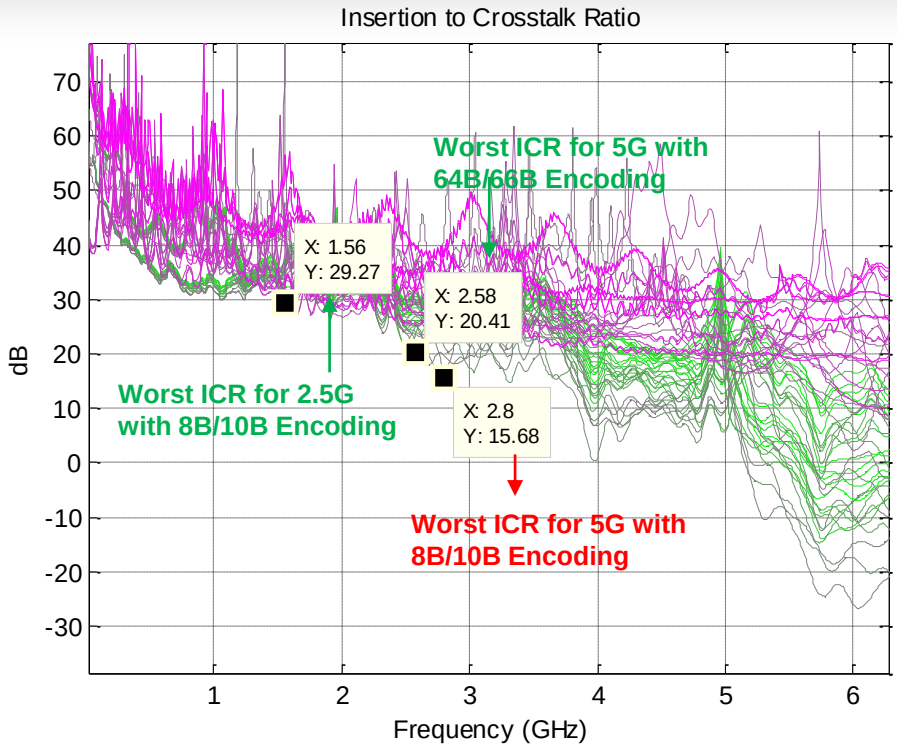
# Channel Analysis of Insertion loss




| Scheme | 2.5G 8B/10B | 5G 64B/66B | 5G 8B/10B |
|---|---|---|---|
| Worst IL (dB) | 8.52 | 14.87 | 19.25 |

- HP24, HP25, HP26 are with worst Insertion loss
  - Large insertion loss deviation @ ~2.8GHz.

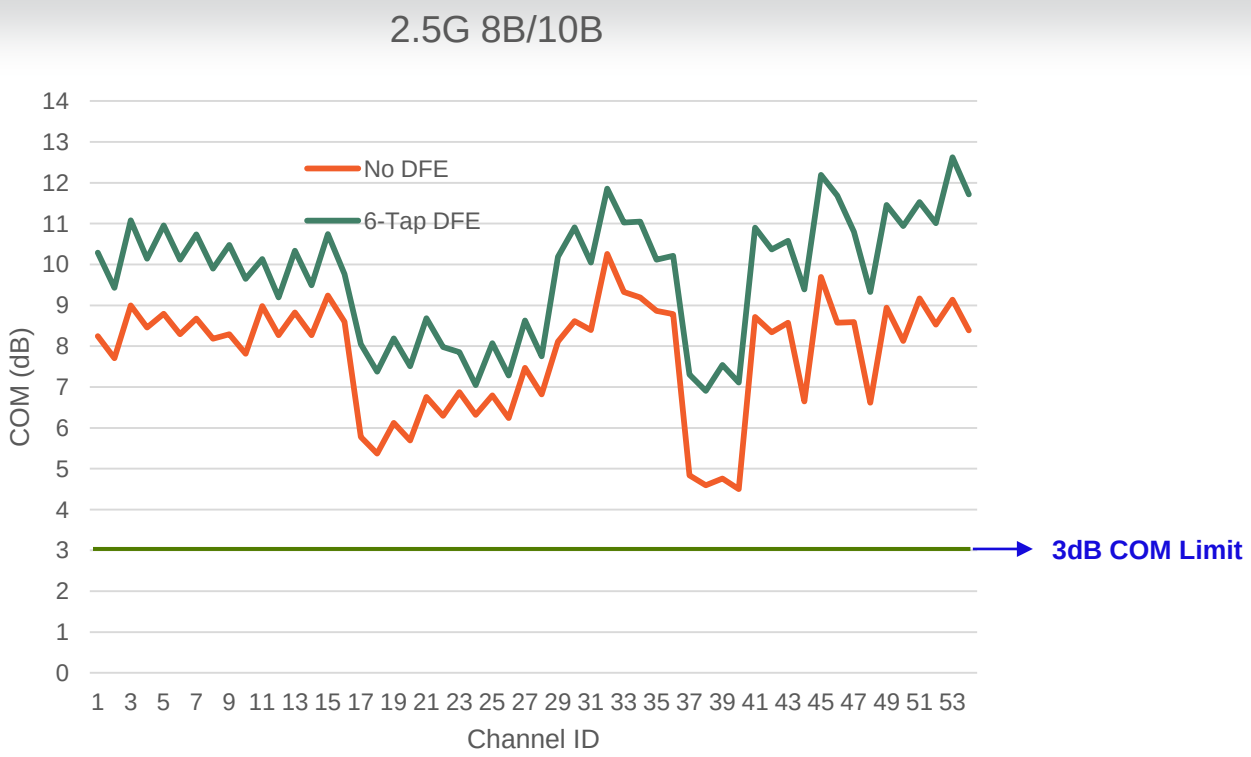
# Channel Analysis of ICR




| Scheme | 2.5G 8B/10B | 5G 64B/66B | 5G 8B/10B |
|---|---|---|---|
| Worst IL (dB) | 29.27 | 20.41 | 15.68 |

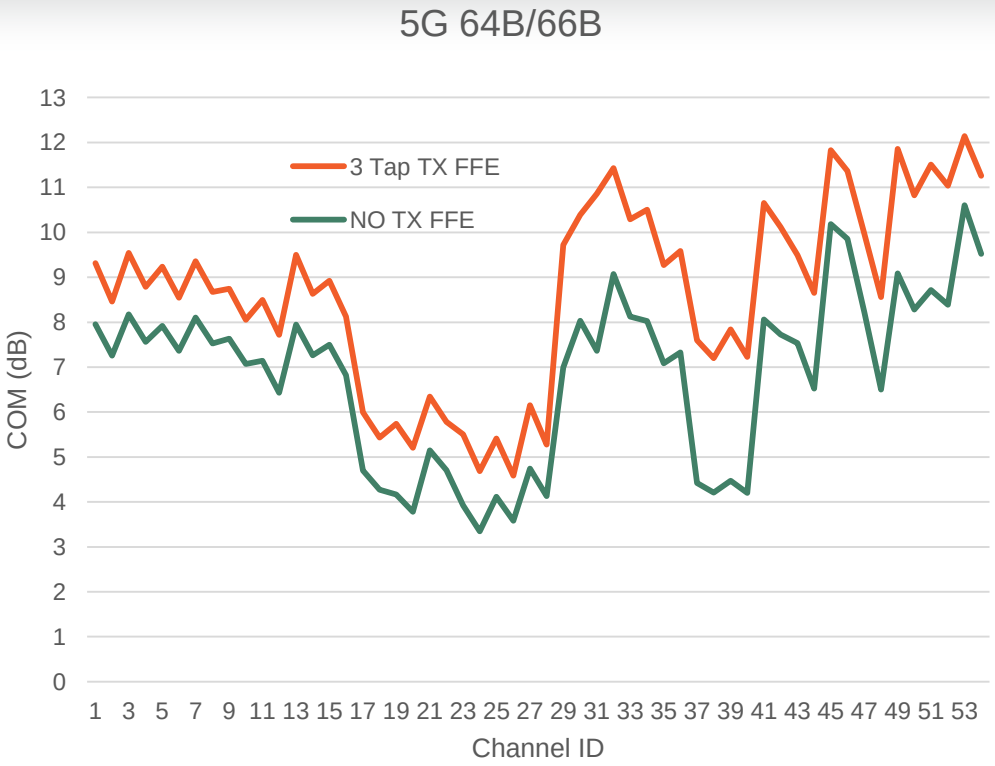
- Some channels have ICR dip @ ~2.8GHz

# Simulation Results with COM - 2.5GBASE-X



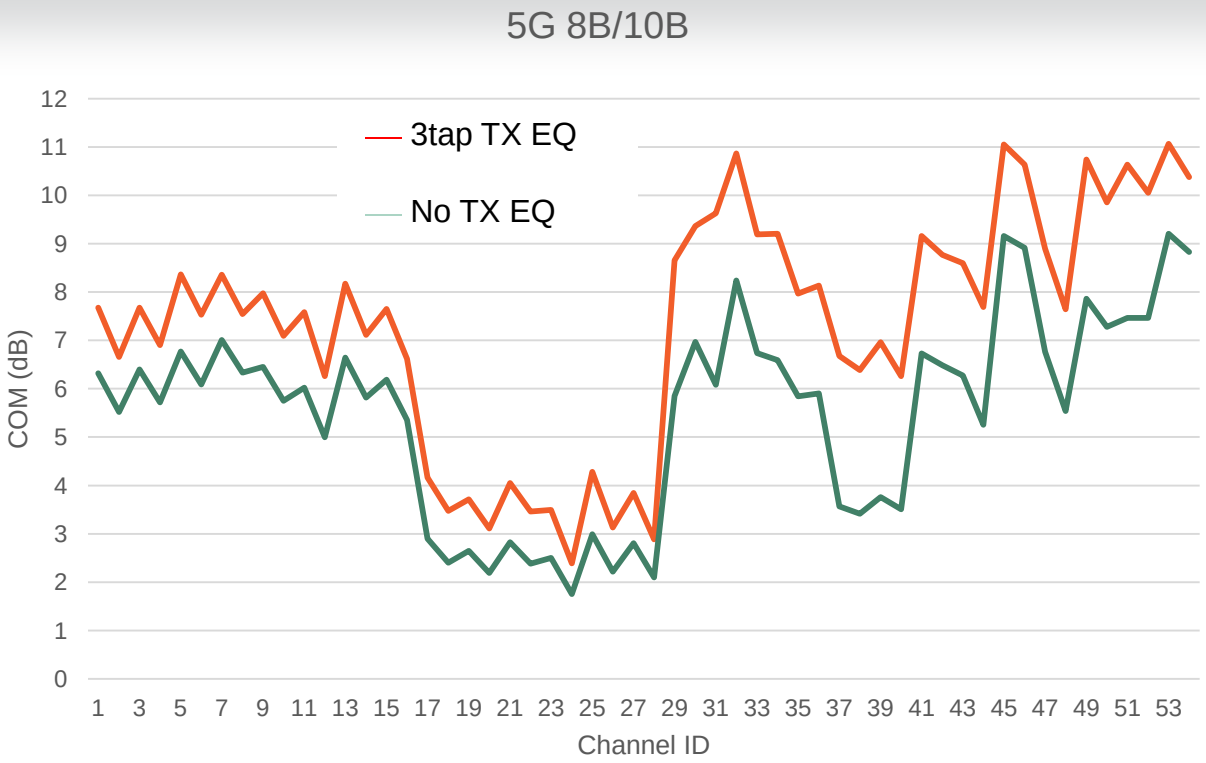

- 2.5Gbps with 8B/10B encoding
  - 3dB COM reserved for loss from implementations
  - All channels pass without DFE or TX EQ

# Simulation Results with COM -5GBASE-R



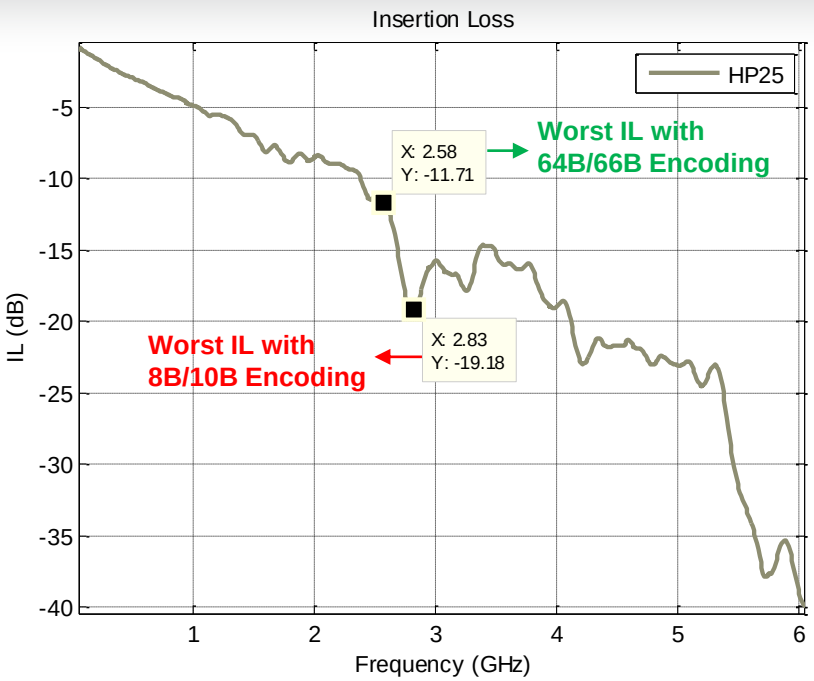

- 5Gbps with 64B/66B encoding
  - All channels pass without TX EQ

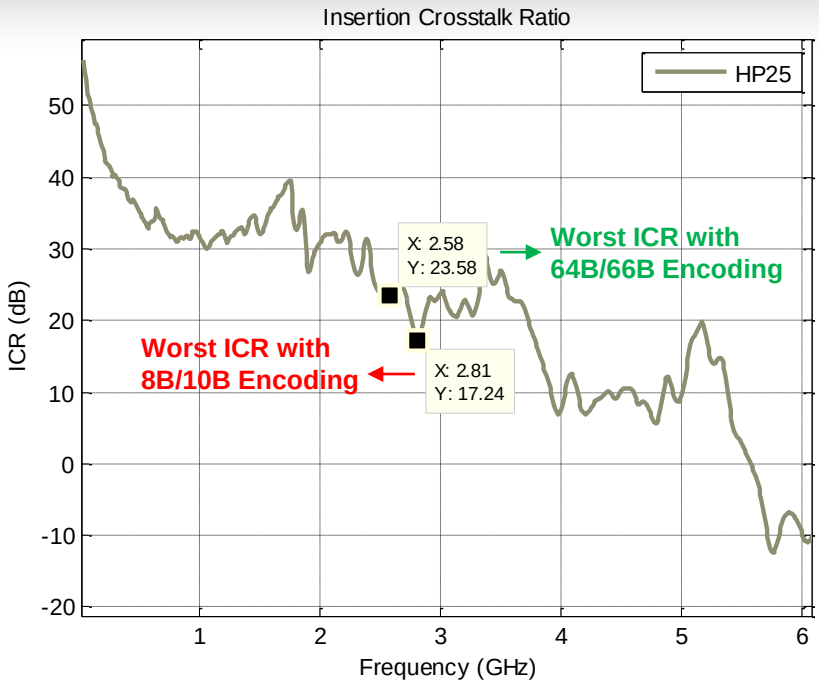
# Simulation Results with COM -5GBASE-X




- 5Gbps with 8B/10B encoding
  - 20% of channels fail even with TX EQ
  - Non-optimal DFE shape due to 8B/10B idle patterns may result in further performance loss ( Lo_802.3CU4HDD_01_0915)

# Performance Analysis with COM – IL dip



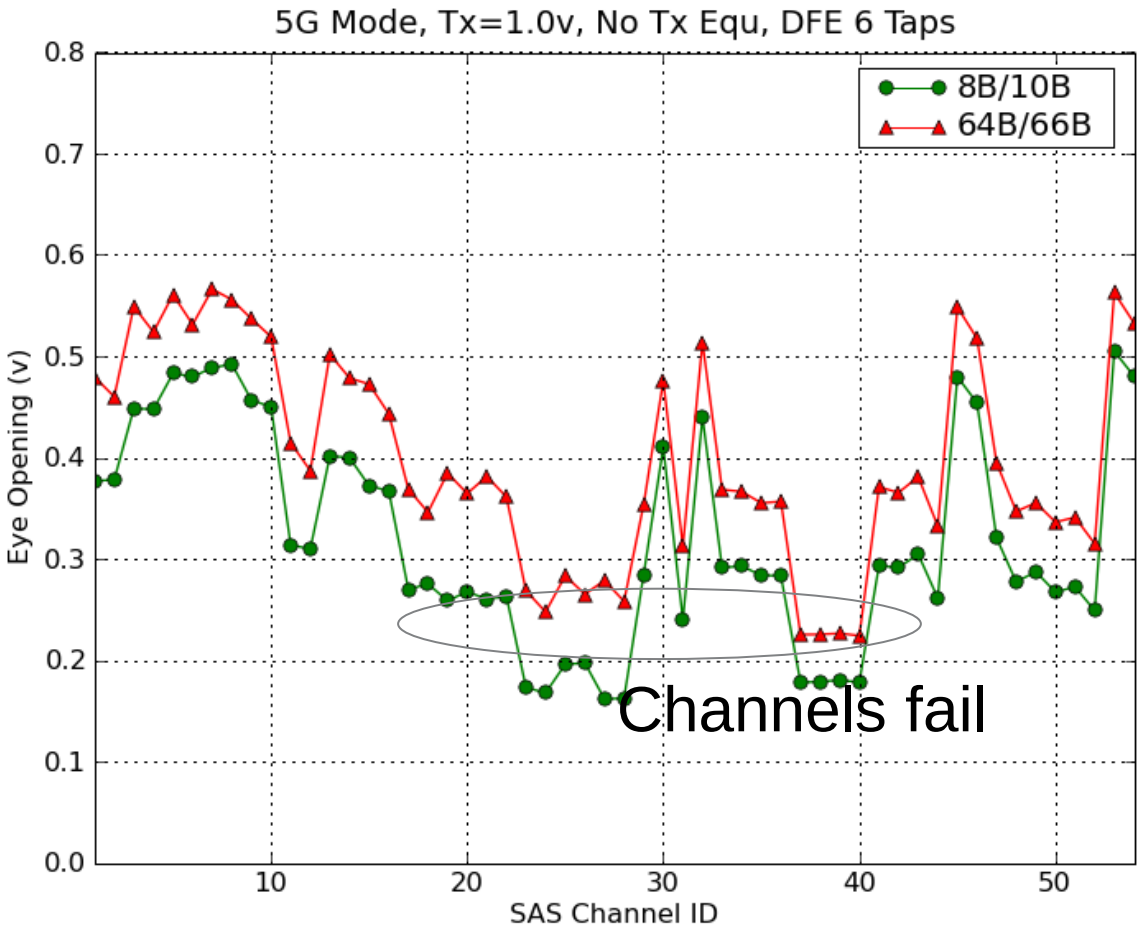




- HP25 has IL dip @ around 2.8GHz and ICR dip @ around 2.8GHz
  - Out of band for 64B/66B scheme (Nyquist at 2.578125GHz)
  - In band for 8B/10B scheme (Nyquist at 3.125GHz)

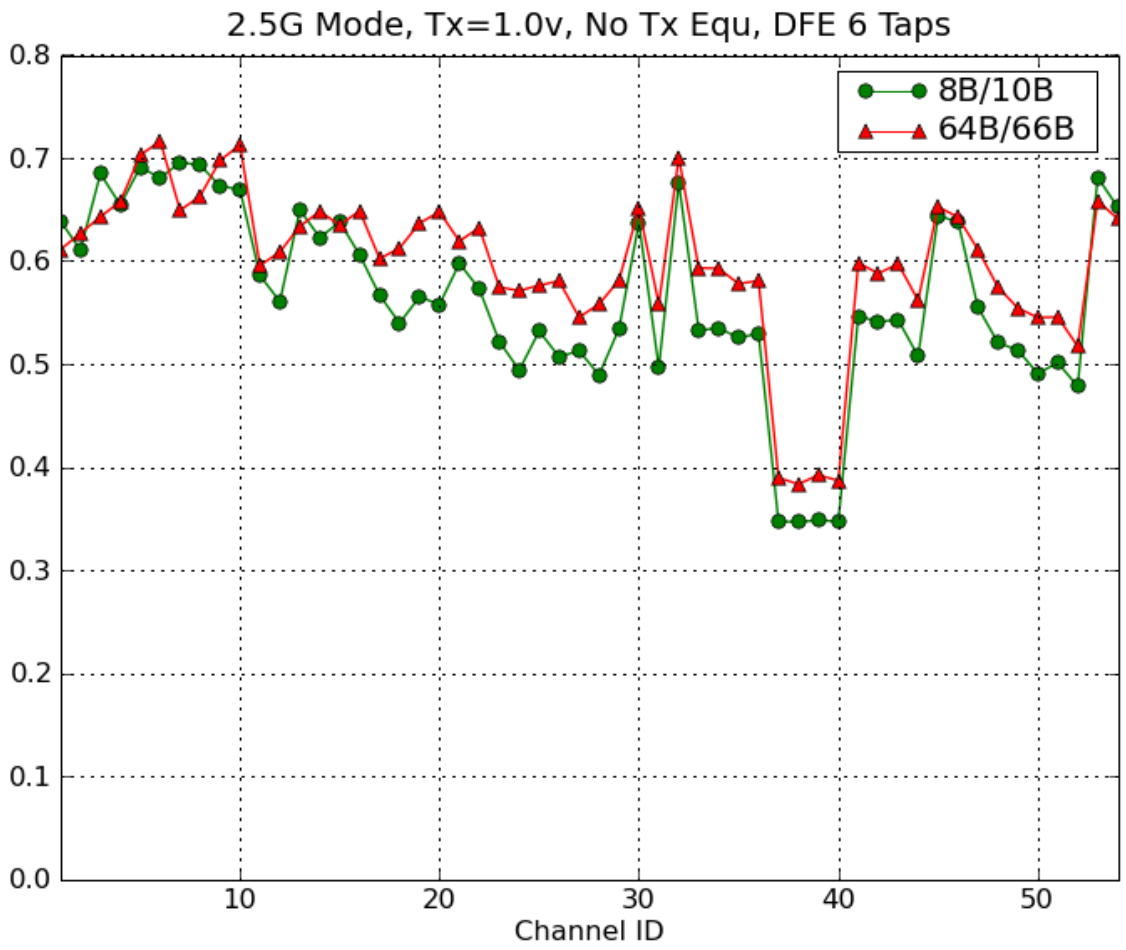
# Simulation Results Using Stateye v4.2.3

- For additional margin - target BER $10^{-15}$
- No TX EQ added
- 6-Tap DFE
- Jitter model added
- Results of eye opening for all 54 channels
- Minimum Required Eye Opening 0.2V
- Observations:
  - 5GBASE-X Mode(8B/10B), 10 channels fail the required eye opening.
  - 5GBASE-R Mode(64/66B) and 2.5GBASE-X(8B/10B) all channels pass
- The results align with that of COM analysis

# Simulation Results Using Stateye – 5G mode



# Simulation Results Using Stateye – 2.5G mode



# Conclusions

- 2.5Gbps
  - ICR  are good for all channels.
  - All channels pass without TX EQ or DFE.
  - 8B/10B is feasible
- 5Gbps
  - All channels pass with 64B/66B encoding and no TX EQ required
  - Some channels fail with 8B/10B encoding
  - 64B/66B is a better choice than 8B/10B for both performance and implementation considerations

# BACKUP SLIDES

# List of Channels : 54 channels

| channel ID | channel | XTALK |
|---|---|---|
| 1 | 'HP01' | 'HP19' |
| 2 | 'HP01' | 'HP15+HP16+2HP17+2HP18' |
| 3 | 'HP02' | 'HP19' |
| 4 | 'HP02' | 'HP15+HP16+2HP17+2HP18' |
| 5 | 'HP03' | 'HP19' |
| 6 | 'HP03' | 'HP15+HP16+2HP17+2HP18' |
| 7 | 'HP04' | 'HP19' |
| 8 | 'HP04' | 'HP15+HP16+2HP17+2HP18' |
| 9 | 'HP05' | 'HP19' |
| 10 | 'HP05' | 'HP15+HP16+2HP17+2HP18' |
| 11 | 'HP06' | 'HP19' |
| 12 | 'HP06' | 'HP15+HP16+2HP17+2HP18' |
| 13 | 'HP07' | 'HP19' |
| 14 | 'HP07' | 'HP15+HP16+2HP17+2HP18' |
| 15 | 'HP08' | 'HP19' |
| 16 | 'HP08' | 'HP15+HP16+2HP17+2HP18' |
| 17 | 'HP09' | 'HP19' |
| 18 | 'HP09' | 'HP15+HP16+2HP17+2HP18' |
| 19 | 'HP10' | 'HP19' |
| 20 | 'HP10' | 'HP15+HP16+2HP17+2HP18' |
| 21 | 'HP11' | 'HP19' |

# List of Channels

| | | |
|---|---|---|
| 22 | 'HP11' | 'HP15+HP16+2HP17+2HP18' |
| 23 | 'HP24' | 'HP19' |
| 24 | 'HP24' | 'HP15+HP16+2HP17+2HP18' |
| 25 | 'HP25' | 'HP19' |
| 26 | 'HP25' | 'HP15+HP16+2HP17+2HP18' |
| 27 | 'HP26' | 'HP19' |
| 28 | 'HP26' | 'HP15+HP16+2HP17+2HP18' |
| 29 | 'long_board_to_drive_oldconn' | 'long_board_to_drive_oldconn_next' |
| 30 | 'short_board_to_drive_oldconn' | 'short_board_to_drive_oldconn_next' |
| 31 | 'long_board_to_board' | 'long_board_to_board_FEXT' |
| 32 | 'short_board_to_board' | 'short_board_to_board_FEXT' |
| 33 | 'b1_thu' | 'b1_next' |
| 34 | 'b2_thu' | 'b2_next' |
| 35 | 'c1_thu' | 'c1_next' |
| 36 | 'c2_thu' | 'c2_next' |
| 37 | 'd1_thu' | 'd1_next' |
| 38 | 'd1_thu' | 'd1_lcc' |
| 39 | 'd2_thu' | 'd2_next_hdd' |
| 40 | 'd2_thu' | 'd2_next_lcc' |
| 41 | 'a2_thu' | 'a2_next' |
| 42 | 'a2_thu' | 'a2_lcc' |
| 43 | 'Intel_HDD_BP_C_MB_03_thru' | 'Intel_HDD_BP_C_MB_03_FEXT' |
| 44 | 'Intel_HDD_BP_C_MB_04_thru' | 'Intel_HDD_BP_C_MB_04_FEXT' |
| 45 | 'Intel_HDD_SC_MB_11' | 'Intel_HDD_SC_MB_11_FEXT' |
| 46 | 'Intel_HDD_SC_MB_12' | 'Intel_HDD_SC_MB_12_FEXT' |
| 47 | 'Intel_MB_C_BP_HDD_01_thru' | 'Intel_MB_C_BP_HDD_01_FEXT' |
| 48 | 'Intel_MB_C_BP_HDD_02_thru' | 'Intel_MB_C_BP_HDD_02_FEXT' |
| 49 | 'Intel_MB_LC_HDD_05' | 'Intel_MB_LC_HDD_05_FEXT' |
| 50 | 'Intel_MB_LC_HDD_06' | 'Intel_MB_LC_HDD_06_FEXT' |
| 51 | 'Intel_MB_LC_HDD_07' | 'Intel_MB_LC_HDD_07_FEXT' |
| 52 | 'Intel_MB_LC_HDD_08' | 'Intel_MB_LC_HDD_08_FEXT' |
| 53 | 'Intel_MB_SC_HDD_09' | 'Intel_MB_SC_HDD_09_FEXT' |
| 54 | 'Intel_MB_SC_HDD_10' | 'Intel_MB_SC_HDD_10_FEXT' |