



On 1uH PoC Inductor

Information to 802.3dm Task Force

July 31, 2025

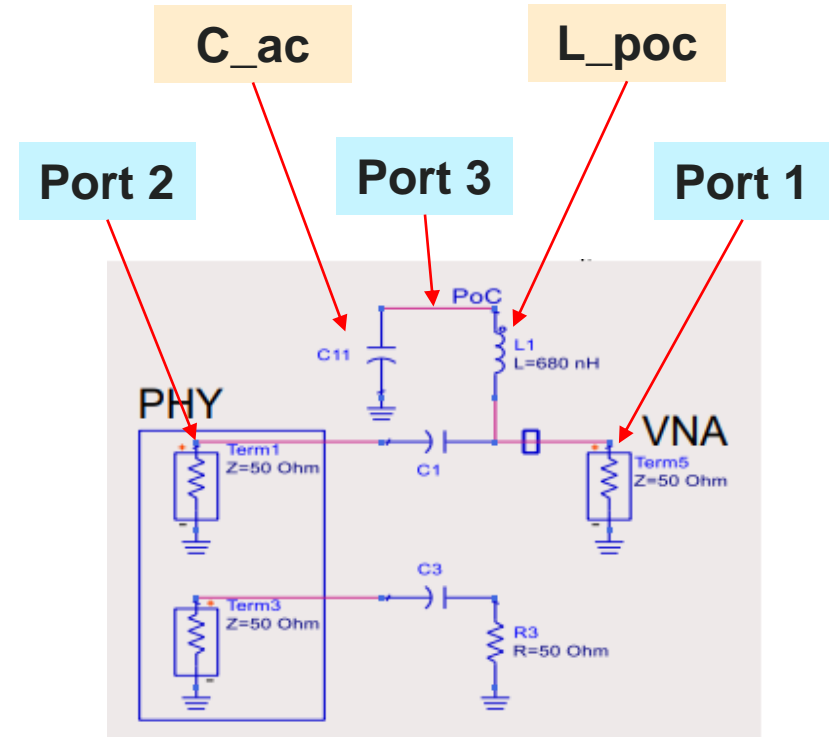
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Introduction

- In the 802.3dm meeting in Madrid Ahmad Chini presented
 - https://www.ieee802.org/3/dm/public/0725/Chini_3dm_01b_07272025.pdf
- In the discussion of this presentation, it was pointed out that the 1uH inductor might not provide sufficient isolation from PMIC noise coupling into MDI (connector) and into the PHY
- This presentation shares a high-level analysis of the signal transfer functions on the PCB board when using single 1uH inductor

PCB Circuit

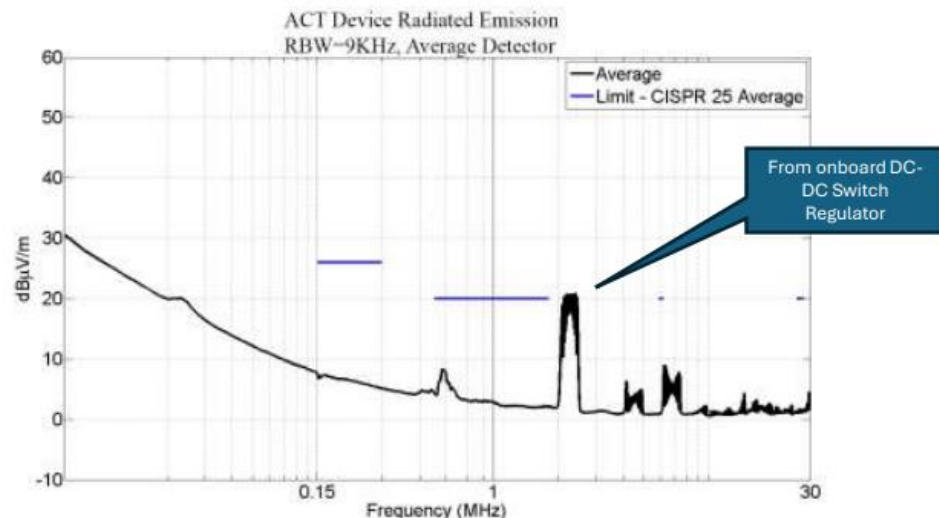
- The circuit diagram on the right is taken from [Chini_3dm_01b_07272025.pdf](https://www.ieee802.org/3/dm/public/0725/Chini_3dm_01b_07272025.pdf)
- The “Port” labels have been added to identify the ports used in the analysis on the following slides
- The PoC inductor L_{poc} and the AC-coupling capacitor C_{ac} are varied in the calculations on the following slides



From https://www.ieee802.org/3/dm/public/0725/Chini_3dm_01b_07272025.pdf

Noise from Power Management IC (PMIC)

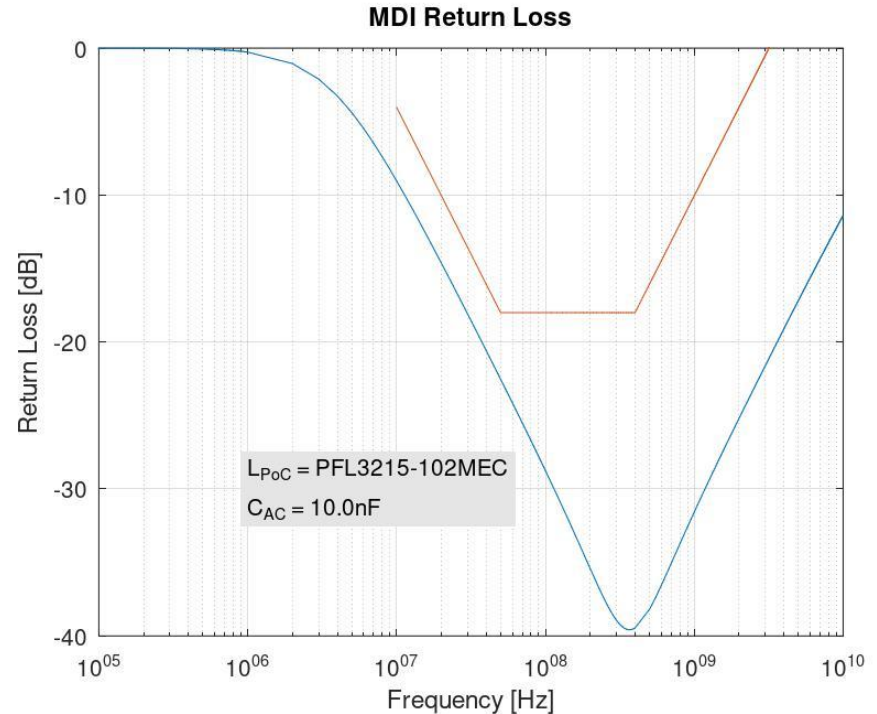
- The figure on the right is taken from the ACT EMC presentation [wu_3dm_01a_072925](https://www.ieee802.org/3/dm/public/0725/wu_3dm_01a_072925.pdf)
- The figure clearly show noise coming from the PMIC at frequency around 2MHz, which is very typical
- If nothing is done to block it, the same PMIC noise will also propagate from the PMIC back through the PoC inductor, onto the line and into the PHY
- This is a very important consideration when selecting inductors for the PoC



From https://www.ieee802.org/3/dm/public/0725/wu_3dm_01a_072925.pdf

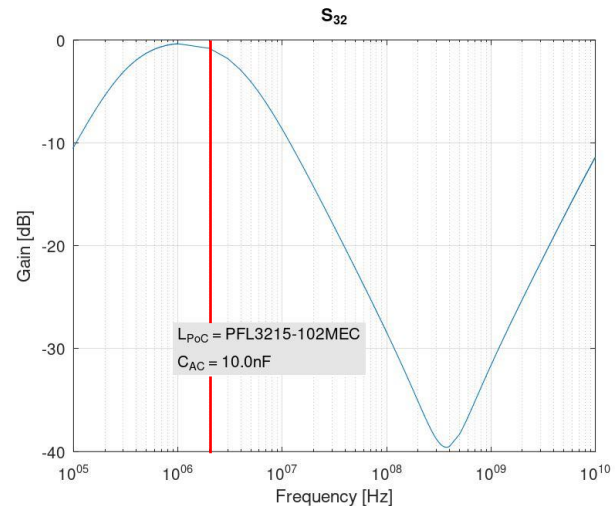
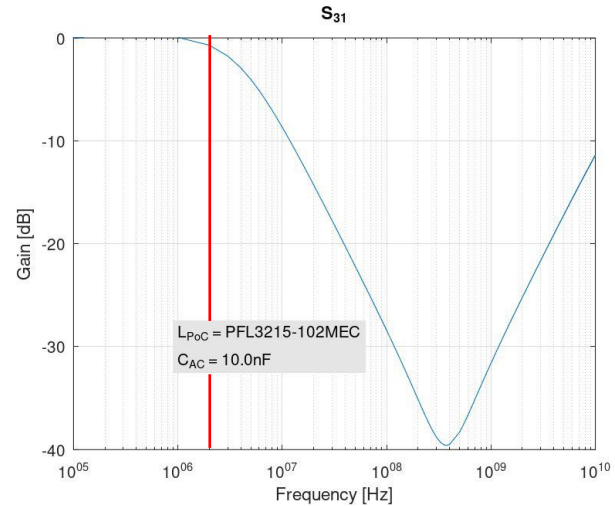
Return Loss for $L_{\text{poc}} = 1\mu\text{H}$

- The figure on the right shows the calculated MDI return loss for $L_{\text{poc}}=1\mu\text{H}$ and $C_{\text{ac}}=10\text{nF}$
- The MDI return loss meets the MDI RL limit defined for 802.3dm
- Does this mean that $1\mu\text{H}$ is a great inductor choose?
 - Not if we are concerned about noise from the PMIC



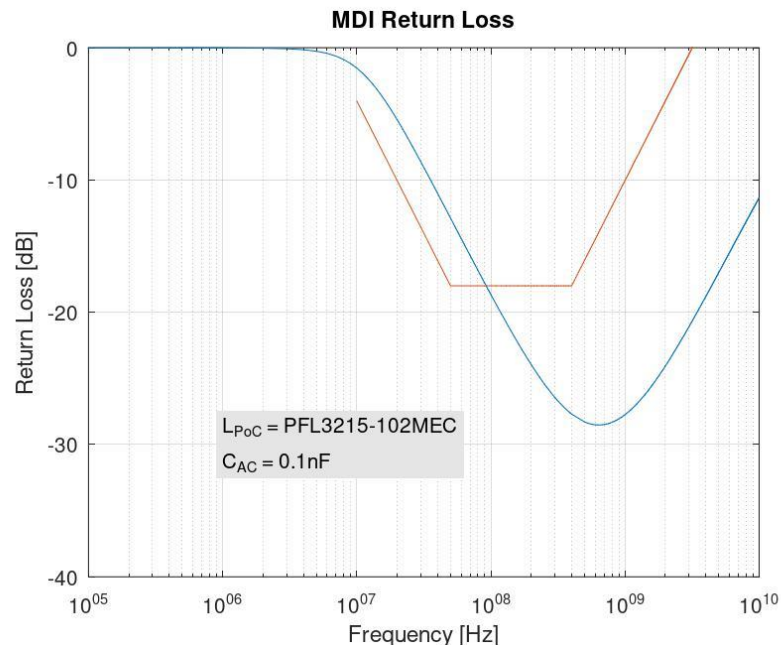
Blocking the PMIC Noise

- The plots on the right show the signal transfer functions from the PMIC (Port 3) to the MDI (Port 1) and the PHY chip (Port 2), for a 1uH inductor
- Both transfer functions have almost no suppression of the 2MHz noise, so the PIMIC noise would go out on both the line and to the PHY input
- This will degrade both local and remote PHY performance unless it is filtered out by other means



Changing the AC-Coupling Capacitor

- One way to reduce the PMIC noise that goes into the local PHY is to use smaller AC-coupling capacitor
- While this can help, it will also change the MDI return loss characteristic
- The plot on the right shows the MDI RL for 1uH PoC inductor and 0.1nF AC-coupling capacitor
- This configuration clearly violates the MDI return loss requirements



Summary

- While it may be possible to use a single 1uH PoC inductor, the analysis in [Chini_3dm_01b_07272025.pdf](#) is insufficient, because it does not analyze the suppression of the PMIC noise
- The local PHY silicon may be designed to filter out the PMIC noise, but this would increase the complexity of the PHY silicon
- The “noise pollution” from the PMIC on the cable (Coax or STP) can lead to interoperability issues, if the link partner is not designed to handle this noise

The Task Force should consider constraining the noise the PHY can output on the cable



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