MultiGBASE-A PHYs use a time-division transmission structure between two active PHYs, in which one link partner transmits a burst while the other is silent. Each link partner transmits according to a TDD cycle consisting of the following three phases:

1. a PAM 2 modulated burst refresh header,
2. a PAM 2 or PAM 4 modulated burst payload,
3. and a QUIET period during which the transmitter is off.

Bursts are aligned so that a PHY transmits its refresh header and burst payload during its link partner's QUIET period. The burst timing provides a gap between transmitted and received bursts to allow for signal propagation delay.

Ethernet frames are encoded in 64/65B blocks and protected in RS-FEC frames (with interleaving at 5 Gb/s and 10 Gb/s data rates). The RS-FEC frames comprise the burst payload portion of the TDD cycle. Asymmetric data rates are achieved by asymmetric transmission times for the link partners, with one transmitting 25 RS-FEC frames per burst and the other transmitting one RS-FEC frame per burst. See 202.3.5 for more detail on TDD bursts.

A MultiGBASE-A PHY may operate as the LEADER or the FOLLOWER. The LEADER-FOLLOWER relationship is predetermined via management control during initialization or via default hardware setup. The LEADER PHY uses a local clock to time its transmitter operations. The FOLLOWER PHY recovers the clock from the received signal and uses it to time its transmitter operations. The LEADER-FOLLOWER relationship is predetermined via management control during initialization or via default hardware setup.