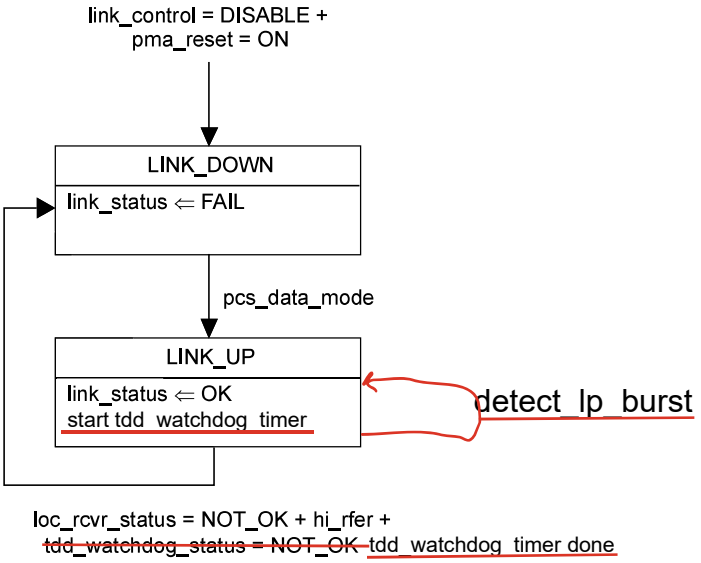

Figure 202–28—Link Monitor state diagram

202.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

202.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 202–14. If MDIO is not implemented, then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Test mode 1 enables testing of timing jitter on the LEADER and FOLLOWER transmitters. The LEADER and FOLLOWER PHYs are connected over a link segment defined in 202.7 or 202.8. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5. TX_TCLK_187.5 is equal to 187.5 MHz and is a divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous repeating pattern of {+1, -1} symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference.