Automotive camera side PHY requirements study from CMOS Image Sensor (CIS) perspective

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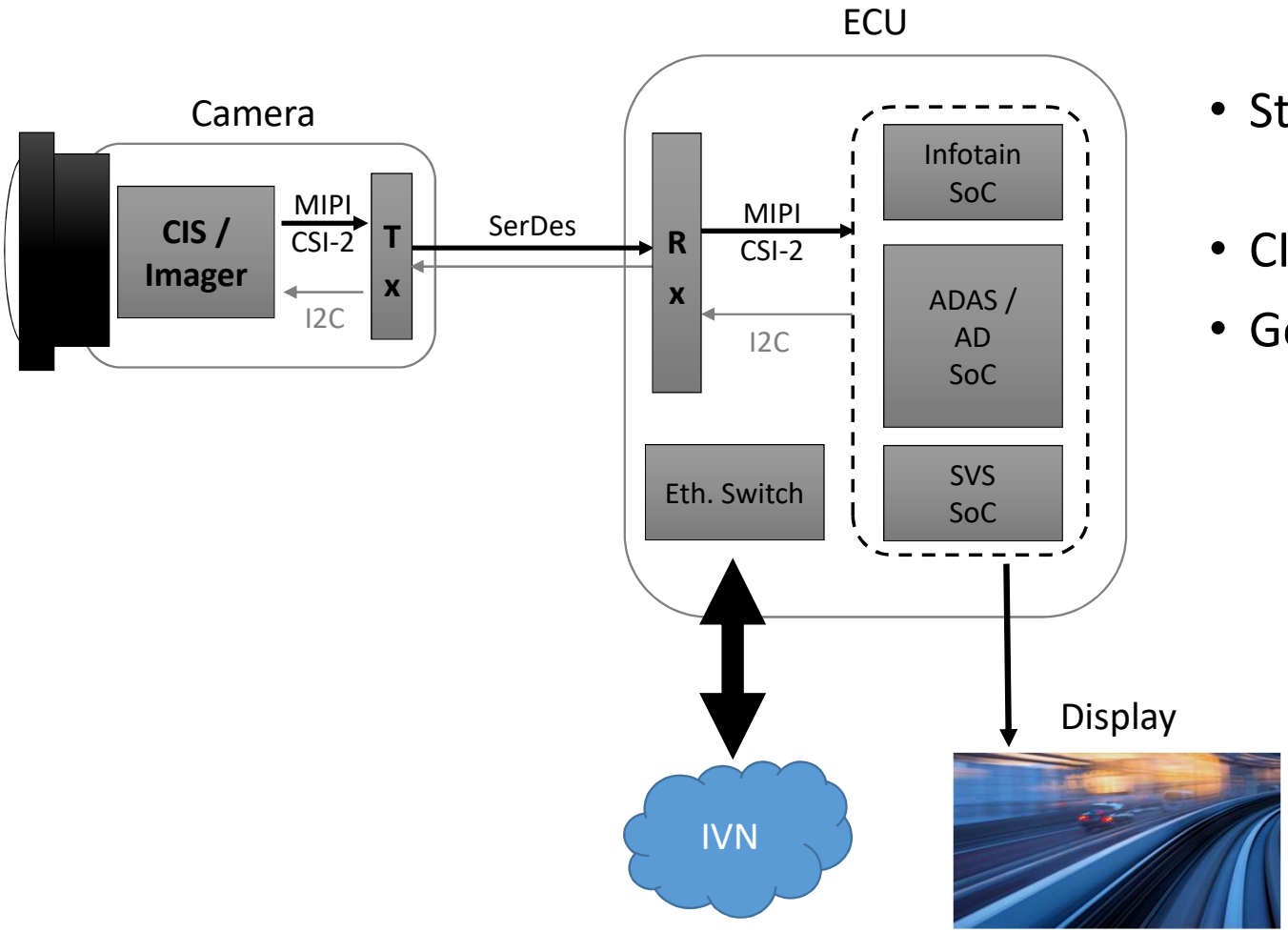
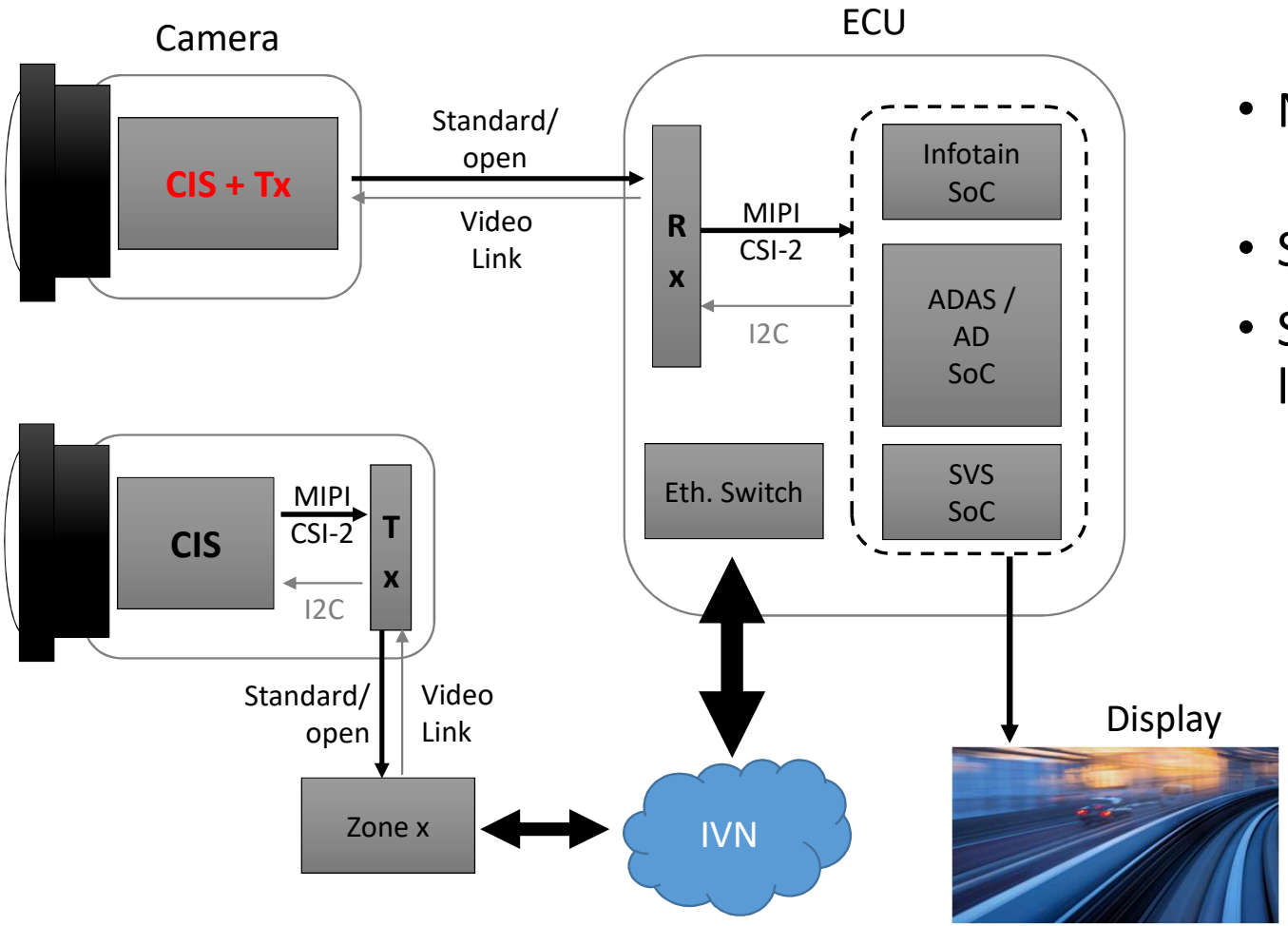
OMNIVISION

Automotive camera architecture – typical today



- Standalone video link ICs
  - Mostly proprietary P2P SerDes
- CIS/imager agnostic to link technology
- General setup/requirements:
  - MIPI CSI-2 IF
  - Camera video data rate support
  - Control/-backchannel (I2C)
  - FuSa and CS concept support
  - Camera power budget constraints
  - Cost budget

Automotive camera architecture – future evolution



- Network architecture change
  - E.g. (partly) zonal architecture
- Standard/ open video link(s)
- Standard video link enables higher levels of IC integration
  - E.g. camera side intergration of Tx into imager

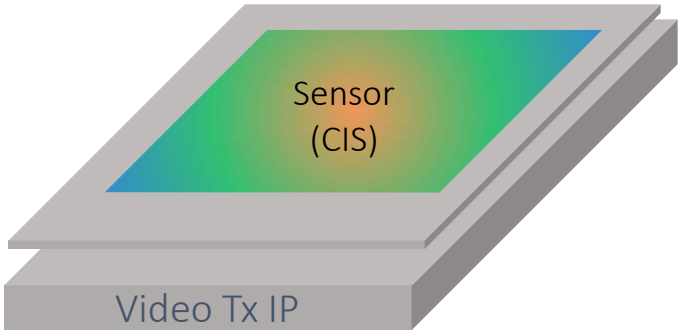
Potential advantages of imager (CIS) + Tx integration

- Smaller size camera modules
- Less complex camera PCB
- Lower BOM cost
- Lower overall power dissipation
- Potentially better thermal management

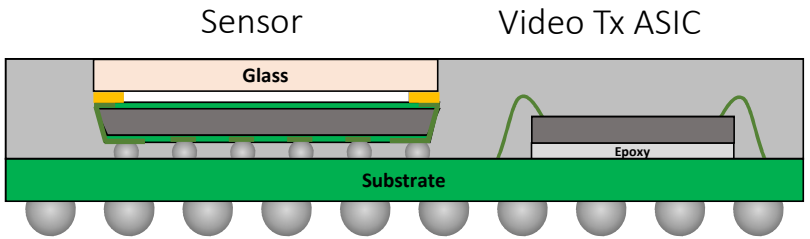
General imager (CIS) + Tx integration requirements

- Video and control bandwidth support
  - Multi Gb/s downstream <= 5 Gb/s (net), higher Gb/s initially not targeted for integration
  - <100Mb/s upstream
- Tx IP complexity / gate count limitation
  - Limited space for additional IP available in modern CIS design
- Technology / process node compatibility
- Power dissipation / thermal management constraints
- Overall BOM cost efficiency
- Support of essential functionality: FuSa, CyberSecurity, Power Over, Sync clock, etc

Integration options



Monolithic integration

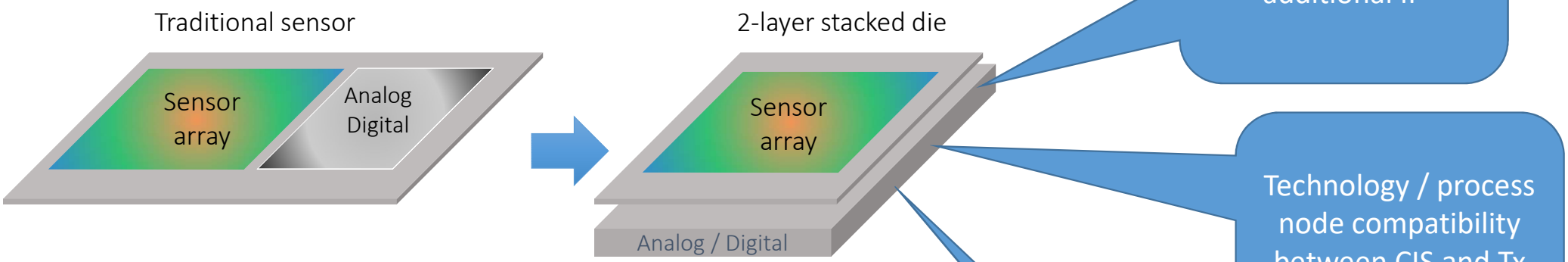


System in a package – SiP

Multi-chip module – MCM

I am discussing the monolithic integration option in this presentation

CIS chip architecture evolution



- Size reduction
- Improve sensor performance
  - Top die optimized for pixel array
- Power reduction
- More digital functions /integration
  - Bottom die optimized for digital logic

Limited space and power budget for additional IP

Technology / process node compatibility between CIS and Tx IP required

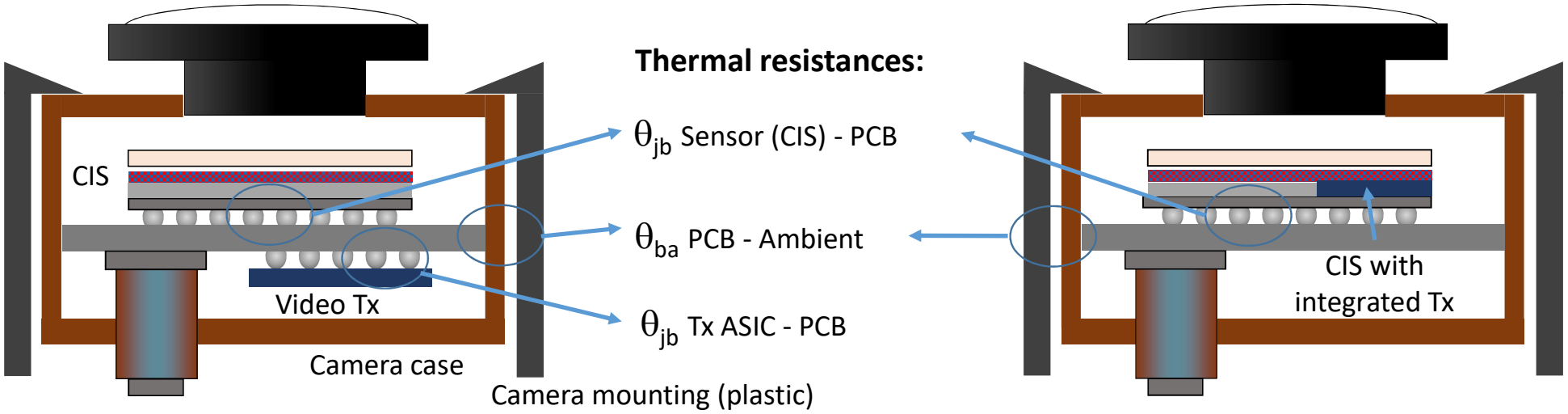
Process node limited by cost / camera BOM

Camera power dissipation and thermal management

- Camera power dissipation and thermal management are key:
  - Automotive cameras are passively cooled (for cost reasons)
  - Smallest size camera housings are desired
  - Thermal connectivity is not good (plastic mounting clamps)
  - Solar loading on top of self heating
  - Data bandwidth (speak camera resolution, fps, etc) and processing complexity is steadily increasing
  - Image quality degrades very rapidly at elevated temperatures
    - Image noise increases (exponentially) with sensor Tj
    - Image unevenness increases with temperature gradients across pixel array

→Thermal management is one of the key constraints for camera design and evolution
  - Power dissipation of key components / silicon IP in the camera needs to be as low as possible

Thermal management – camera level / CIS Tj



$Tj_{CIS} = Ta + \theta_{ba}(P_{CIS} + P_{CSI2} + P_{Tx} + P_{IC}) + \theta_{jb}(P_{CIS} + P_{CSI2})$

$Tj_{CIS/Tx} = Ta + \theta_{ba}(P_{CIS} + P_{Tx} + P_{IC}) + \theta_{jb}(P_{CIS} + P_{Tx})$

→ $Tj_{CIS/Tx} - Tj_{CIS} = \theta_{jb}(P_{Tx} - P_{CSI2}) - \theta_{ba}P_{CSI2}$

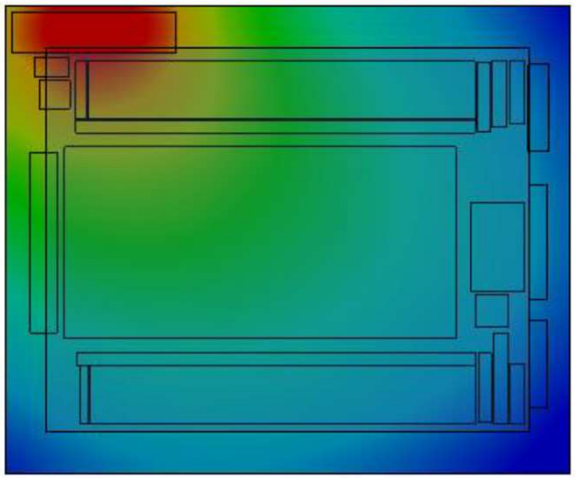
Key findings for integrated Tx version:

- Total camera power consumption is lower (one less IF)
- Imager T_j is lower ($\theta_{ba} >> \theta_{jb}$ in the real application)

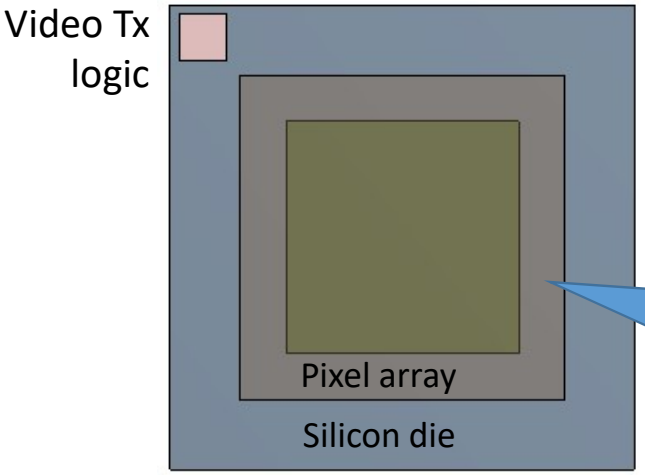
Thermal Management – CIS chip Level

Image sensor heat map simulation for integrated Video Tx CIS chip architecture

CIS floor plan and temperture profile



Simulation condition



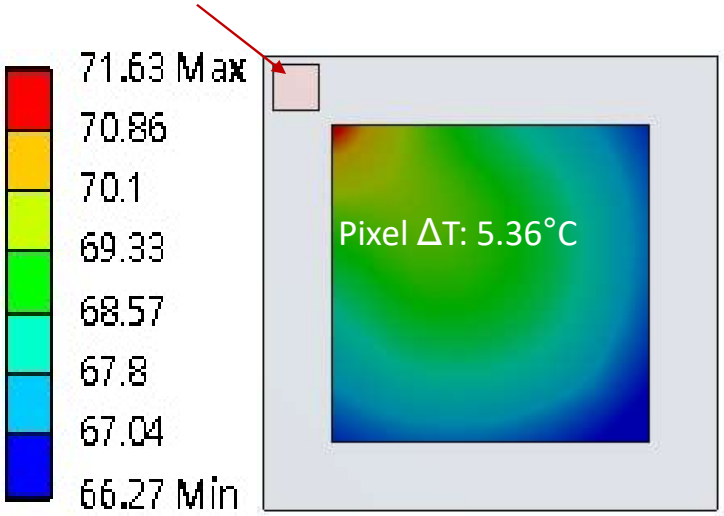
Goal is to keep temp gradient accross Pixel area <2°C, in order to keep Dark Image Non-uniformity (DINU) on acceptable level

- Total die size: 10x10mm
- Pixel area: 7x7mm
- Video Tx logic size: 1x1mm
- CIS chip power: 400mW
- T ambient: 40°C
- Heat sink: standard OMNIVISION prototype camera PCB

Thermal Simulation

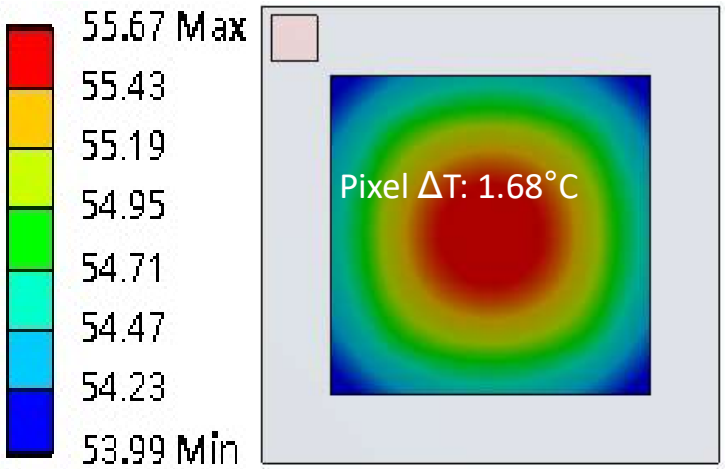
Image sensor heat map with and without integrated Video Tx

w/ Video Tx induced power of 400mW



Pixel array temperature profile (°C)

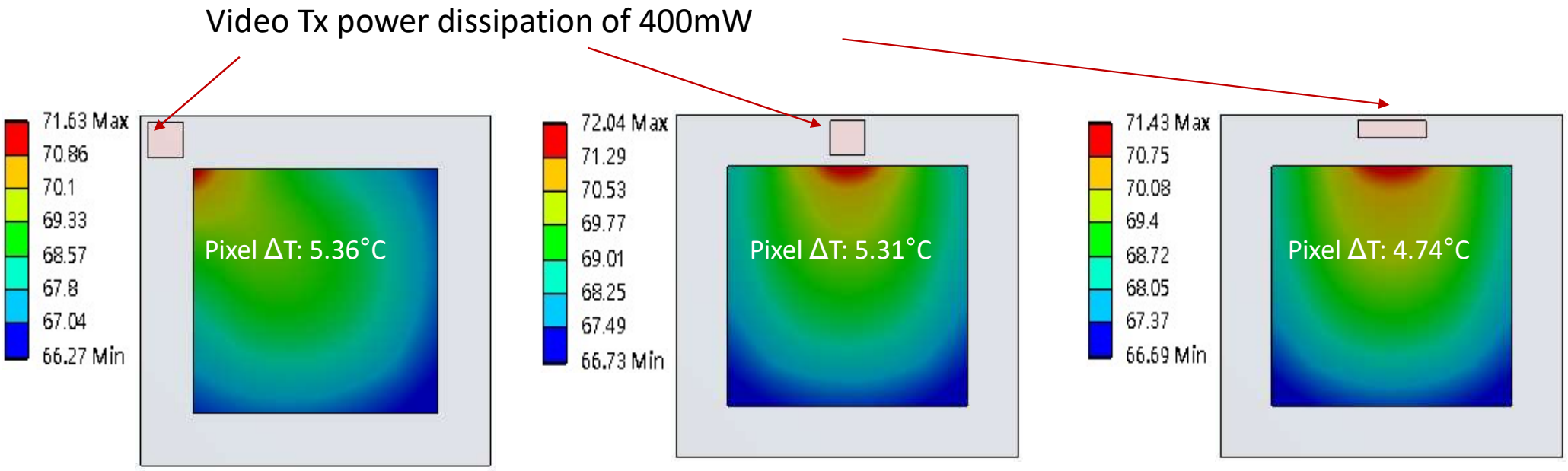
w/o Video Tx induced power of 400mW



Pixel array temperature profile (°C)

Thermal Simulation

Change of Video Tx logic location and shape

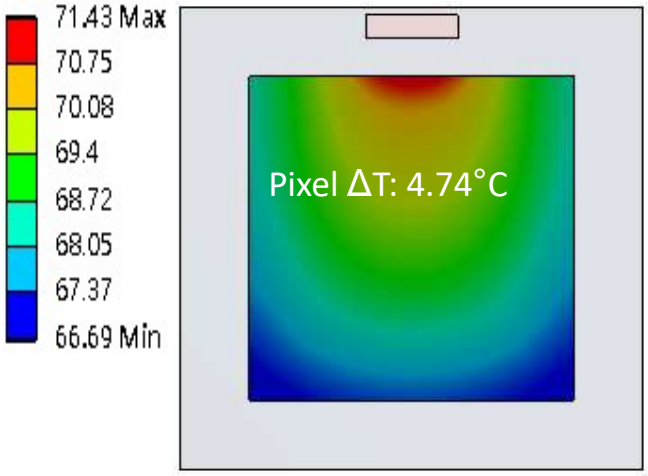


Pixel array temperature profiles (°C)

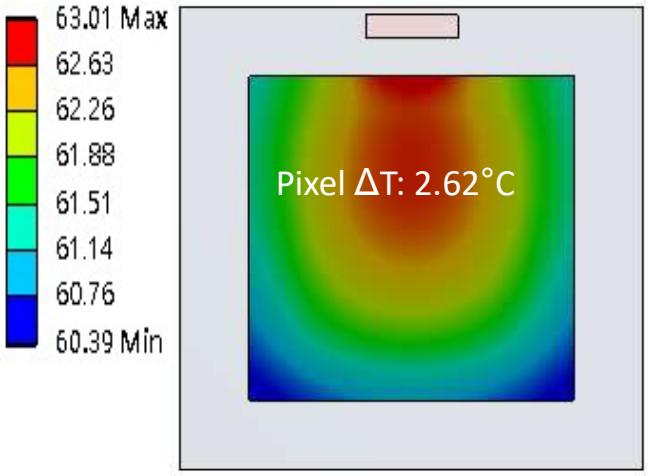
Thermal Simulation

Change of Video Tx logic IP power dissipation

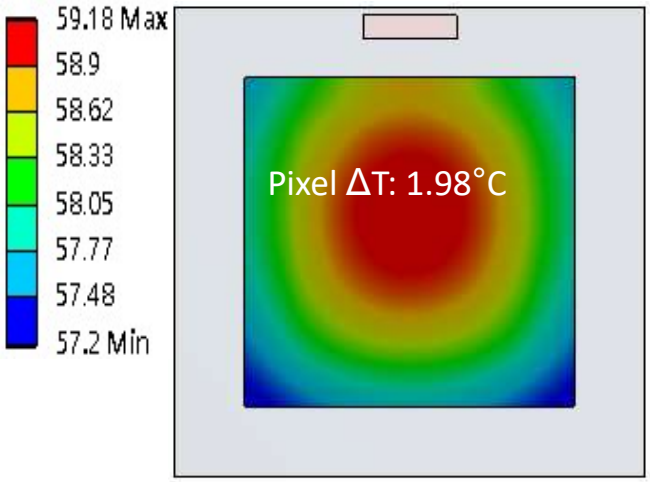
Video Tx power of 400mW



Video Tx power of 200mW



Video Tx power of 100mW

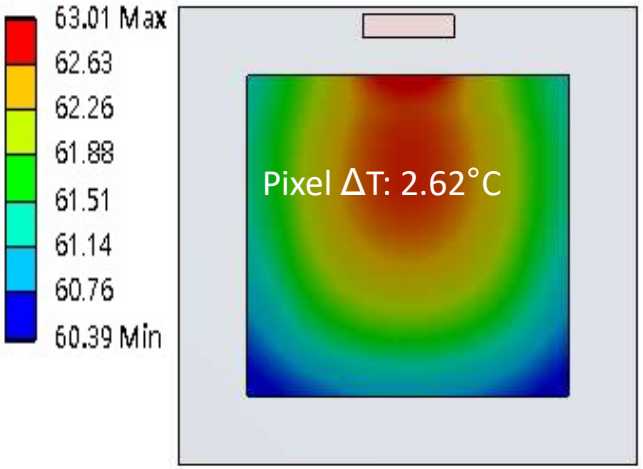


Pixel array temperature profiles (°C)

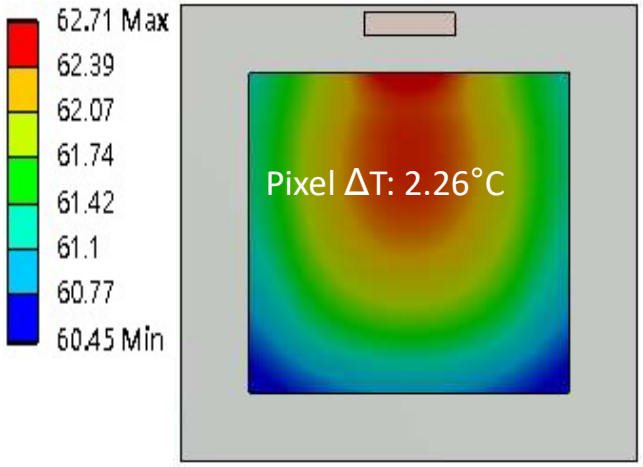
Thermal Simulation

Change of silicon thickness

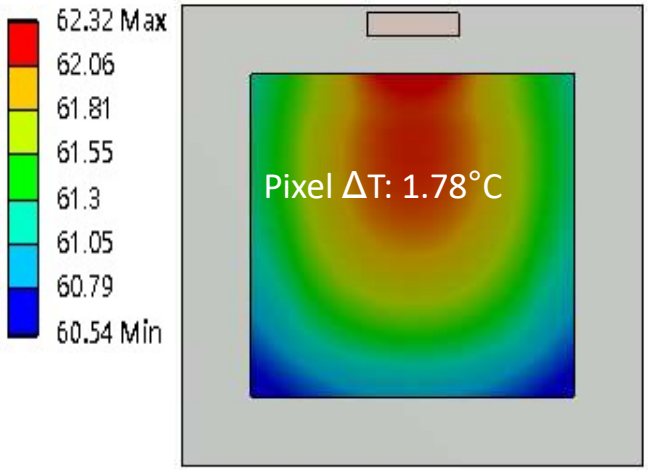
Silicon thickness: 150μm
(Video Tx power: 200mW)



Silicon thickness: 200μm
(Video Tx power: 200mW)



Silicon thickness: 300μm
(Video Tx power: 200mW)

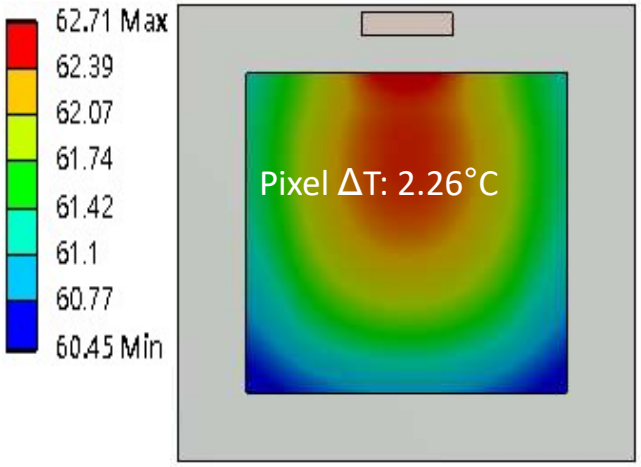


Pixel array temperature profiles (°C)

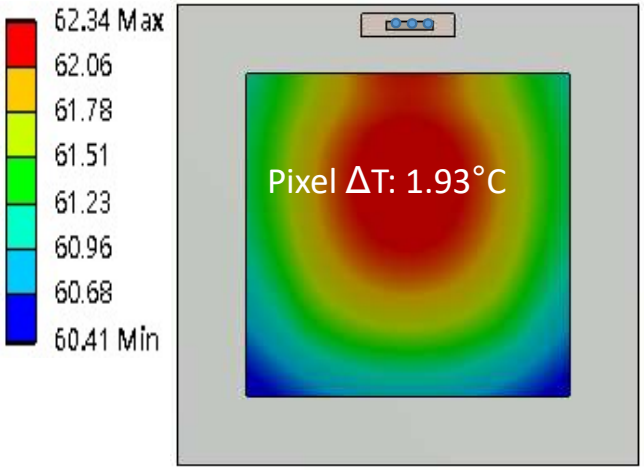
Thermal Simulation

Optimized heat transfer / thermal via

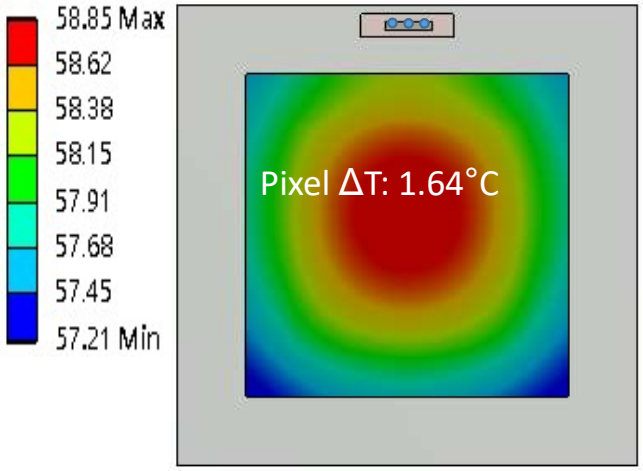
w/o thermal via
Silicon thickness: 200μm
Video Tx power: 200mW



w/ thermal via
Silicon thickness: 200μm
Video Tx power: 200mW



w/ thermal via
Silicon thickness: 200μm
Video Tx power: 100mW



Pixel array temperature profiles (°C)

Thermal Simulation Summary

Parameter	Worst case	Improved
Tx location and shape	Corner block	Edge strip
Tx logic IP power	400mW	< 200mW
Si thickness	150µm	> 200µm
Thermal design	w/o thermal via	w/ thermal via
Pixel ΔT	> 5°C	< 2°C

→Pixel array temp gradient goal of <2°C can be achieved with:

- optimized CIS chip architecture and
- efficient power dissipation figures of the integrated Tx IP

Summary

- Standardized automotive data/video link can create a case for Tx integration into CIS on camera side
  - Drivers are reduction of camera complexity, size and cost
- Besides obvious specs (like data rate) the key requirements are:
  - Lowest possible Tx IP complexity / gate count in order to fit CIS size and process node constraints
  - Lowest possible power dissipation of Tx IP
    - To fit overall camera power buget
    - To achieve manageable temp gradients accross CIS pixel array