PHY Technical Options

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Presentation Goal

- List out some technical paths that project can take
  - Use 10 Gb/s downstream as examples
  - Similar concept for 1, 2.5, 5, and 25 Gb/s

- We are not
  - Choosing a solution
  - Saying which options are better or worse

Basic Assumptions

- Technical feasibility of 802.3bw, 802.3bp, 802.3ch, 802.3cy are taken as a given
  - i.e. 100BASE-T1, 1000BASE-T1, 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1, 25GBASE-T1
  - Technical feasibility work has been done already – no need to rehash
  - Includes EEE where applicable

- We are looking for a more optimal solution for asymmetrical use case

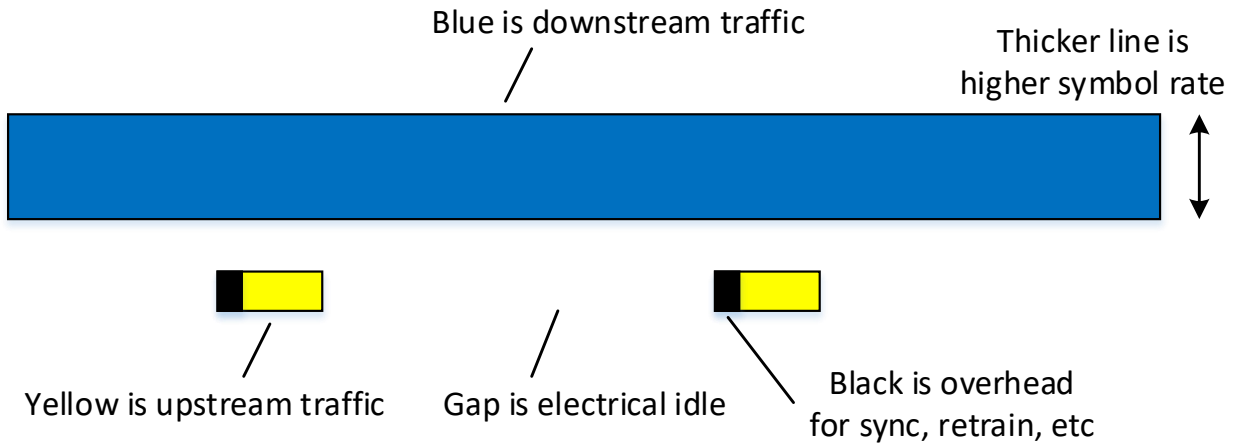
Basic Assumptions

- Assume 10G downstream is PAM4 in all examples
  - Uniform comparison
  - Does not preclude solution that is not PAM4

- Upstream speed is 100 Mb/s
- Running slower is easier than running faster
- Requirement is to run on single cable

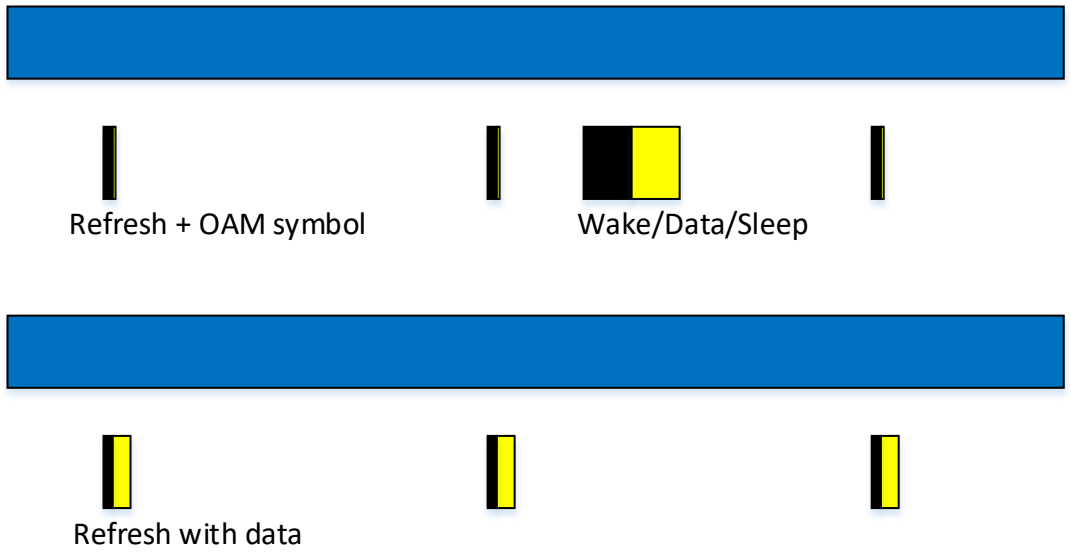
Key to Diagrams

- Following diagrams helps with qualitative understanding on the signaling over the PHY
  - Both width and height are not to scale
  - Elements are not proportional in size (be able to see details but also fit on page)



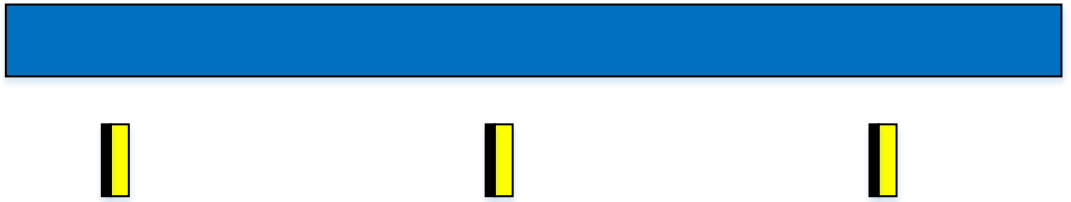
EEE Option – Basic Optimization

- Baseline – Quiet/Refresh, Wake/Sleep – (As currently defined)
  - Refresh in PAM2
  - Need to recover OAM symbol near end of refresh
  - Refresh cycle active ratio 1:96
- Basic Optimization
  - Tag additional data with refresh
  - Refresh + data cycle active ratio approx 3:96 in PAM2, 2:96 in PAM4
  - Startup optimization
- Downstream 5.625 Gbaud
- Upstream data 5.625 Gbaud PAM2 or PAM4

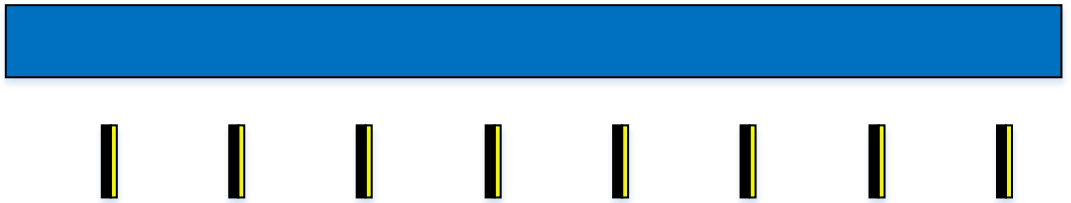


EEE Option – Lower Latency

- Basic Optimization
  - Refresh + data cycle active ratio
    approx. 3:96 for PAM2

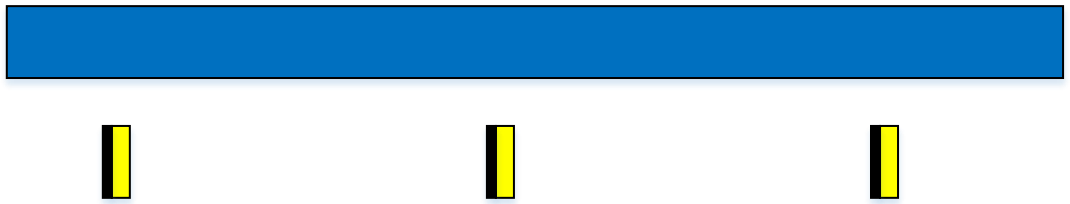


- Lower Latency
  - Trade cycle time for latency
  - example 3x lower latency
  - Refresh + data cycle ratio approx 5:96 for PAM2

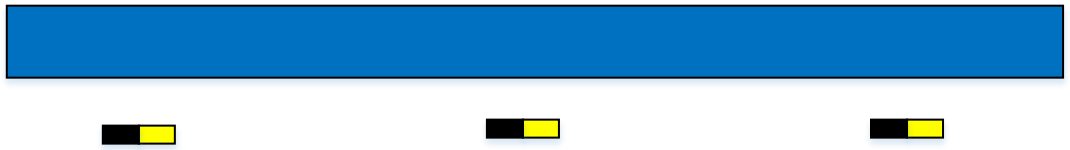


EEE Option – Slower Upstream

- Basic Optimization
  - 5.625 Gbaud upstream



- Slower Upstream Burst Rate
  - Trade cycle ratio for lower upstream speed
  - Example 4x slower:
    - 1.4 Gbaud, ratio ~ 12:96, PAM2

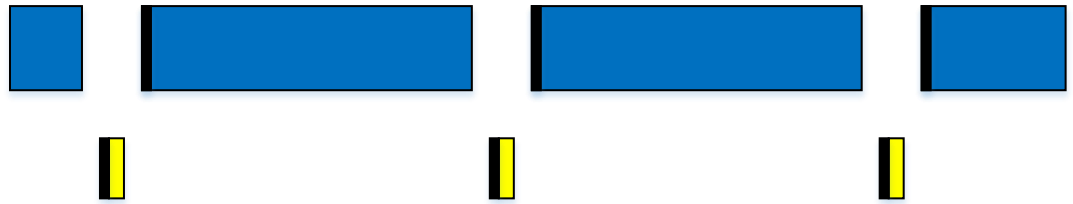


FDD Option

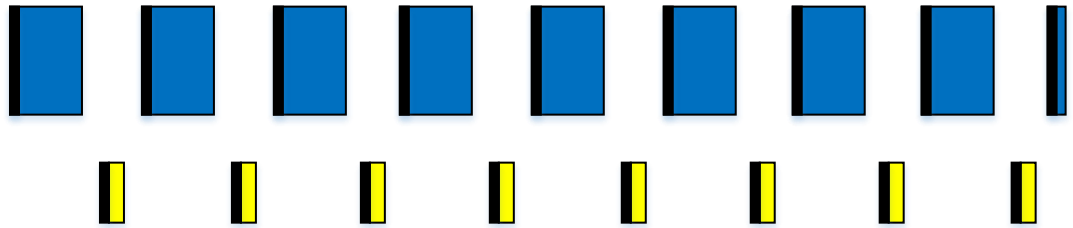
- No overhead needed
- Ratio 1:1
- Downstream 5.625 Gbaud
- Upstream approx. 0.1 Gbaud +/-
  - Can be like 100BASE-T1 or slowed down 1000BASE-T1
  - Modification to carry OAM channel, possibly lightweight FEC

TDD Option

- Baseline Case
  - Run slightly faster since half duplex
  - Downstream ~6 Gbaud
  - Upstream 2 to 4 Gbaud PAM2



- Lower latency
  - Trade increased downstream speed for latency
  - Downstream ~7 to 8 Gbaud
  - Upstream 2 to 4 Gbaud PAM2



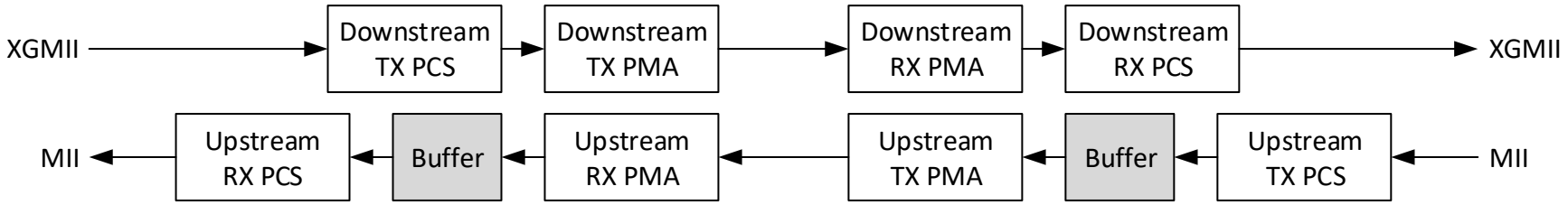
Making MAC Interface Full Duplex

- Internal buffering in PHY smooths out stop and go

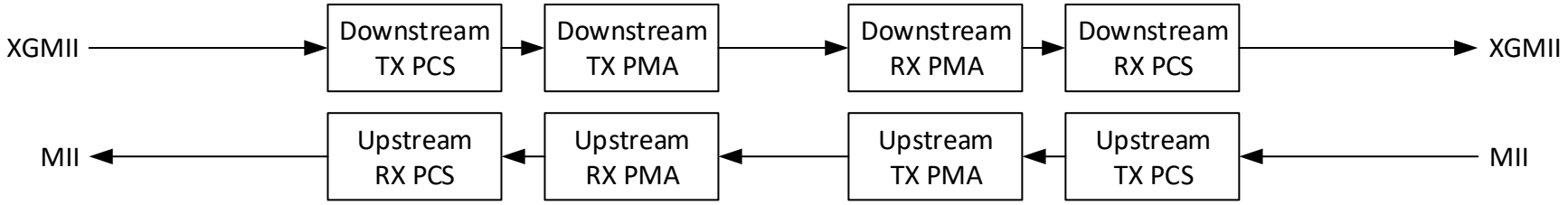
- We are not buffering Ethernet Frames
- We are buffering the stop and go nature of the layer 1 bit stream
- Buffer somewhere between PCS and PMA (roughly)

Buffer Placement (Approx)

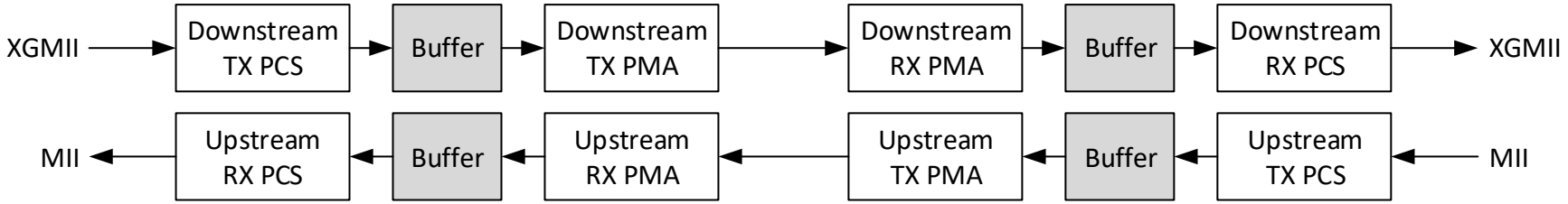
- EEE



- FDD



- TDD



MAC Interface & Buffering

- Buffers are constant latency
- Size of buffer proportional to latency
- MAC interface is constant speed to defined IEEE interface
  - 10G downstream XGMII, 100M Upstream MII
- Buffer latency if MAC interface is constant speed
  - Store up delay at the TX side
  - Playback at RX side – minimal delay

Summary Table of Examples

- 10 Gbps downstream, 100 Mbps upstream

Mode of Operation	Downsteram Symbol Rate (PAM4)	Upstream Symbol Rate	Buffering/ Latency	Upstream Active Ratio
Basic Optimized EEE	5.625 Gbaud	5.625 Gbaud	Upstream Only	~ 3:96
3x Lower latency EEE	5.625 Gbaud	5.625 Gbaud	Upstream Only	~ 5:96
4x Slower Upstream	5.625 Gbaud	1.406 Gbaud	Upstream Only	~ 12:96
FDD	5.625 Gbaud	0.1 Gbaud +/-	None Needed	
TDD	~6 Gbaud	2 to 4 Gbaud	Both Directions	
TDD Lower Latency	~7 to 8 Gbaud	2 to 4 Gbaud	Both Directions	

Conclusion

- There are many viable options that are technically feasible

- Task Force to evaluate direction we take

THANK YOU