General Feasibility of Key Goals

Contribution to ISAAC Study Group

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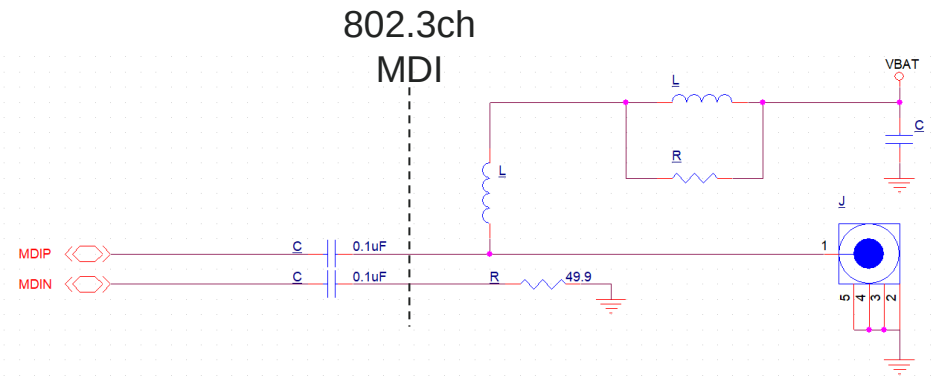
Introduction

In this presentation we look into the feasibility of some of our key goals:

- ❑Operation over coax
- ❑Operation with power delivery
- ❑Reduced power consumption
- ❑Reduced complexity and relative cost

Operating IEEE 802.3ch Link Over Coax

- IEEE 802.3ch is intended to operate over balanced differential pair
- The block diagram on the top right shows circuitry to operate IEEE 802.3ch over single coax
- Simulations and lab experiments have demonstrated that this setup works for IEEE 802.3ch



IEEE 802.3ch PHY can operate over coax cable

☑ Operation over coax is feasible

Operating IEEE 802.3ch with PoDL

- IEEE 802.3ch is intended to operate with PoDL over balanced differential pair (see clause 1.4.494)
- The block diagram on the right shows PoDL IEEE 802.3bu system block diagram
- Simulations and lab experiments have demonstrated that the PoDL setup works for IEEE 802.3ch

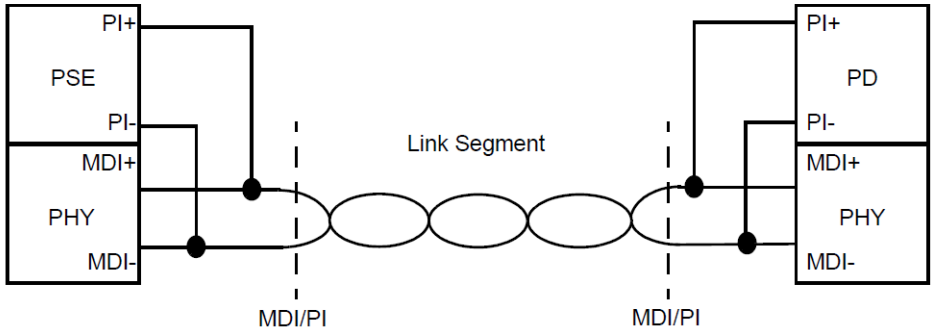
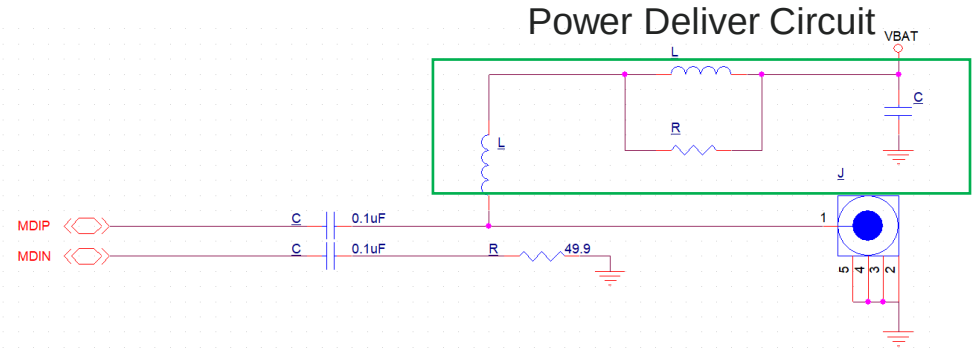


Figure 104–3—PoDL system block diagram

IEEE 802.3ch PHY can operate with PoDL

IEEE 802.3ch Link Over Coax with Power Delivery

- The block diagram on the right shows circuitry to operate IEEE 802.3ch over single coax
- Simulations and lab experiments have demonstrated that this setup works for IEEE 802.3ch link
- Power delivery over coax link have also been demonstrated with proprietary technologies



IEEE 802.3ch PHY can operate over coax cable with power delivery

- [x] Operation with power delivery is feasible

Relative Cost and Power Saving Opportunities

Among key things that determine the complexity, relative cost and power consumption of a PHY are:

- Symbol rate, which typically increases complexity and power with higher data rate
  - For asymmetric links we can potentially reduce the symbol rate in the low data rate direction, which results in complexity reduction and power savings
- Multi-Gbps data processing will typically require parallelism in the digital implementation
  - For the low data rate direction we will potentially be able to reduce the parallelism (reduce HW), which results in lower relative-cost and power
- Duplexing schemes, which typically increases power for symmetric data rate
  - Duplexing schemes, such as Echo Cancelation, Frequency Domain Duplexing, and Time Domain Duplexing all increase the complexity and power consumption of the HW (compared to no duplexing)
  - Using simpler duplexing due to lower upstream data rate will reduce relative cost and power

Power and relative cost saving is feasible on asymmetric camera link

Reduced Symbol Rate

- Symbol rate is one of the key things that determine power consumption and complexity in PHY design
- One possible way to reduce power consumption and complexity for the asymmetric link is to use lower symbol rate for the low data rate direction
- The data rate at 100Mbps is 25 times lower than the data rate for 2.5Gbps and 100 times lower than the 10Gbps data rate
- There is an opportunity to significantly simplify the low data rate path, by using lower data rates (this applies to EC and FDD systems)

Lower symbol rate can reduce PHY power and PHY complexity

- [x] Reduction in power consumption is feasible
- [x] Reduction in complexity and relative cost is feasible

Summary

In this presentation we saw that some of our key goals are feasible:

✓Operation over coax is feasible

✓Operation with power delivery is feasible

✓Reduced power consumption is feasible

✓Reduced complexity and relative cost is feasible

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