Camera and Sensors Protocols in Automotive IVN

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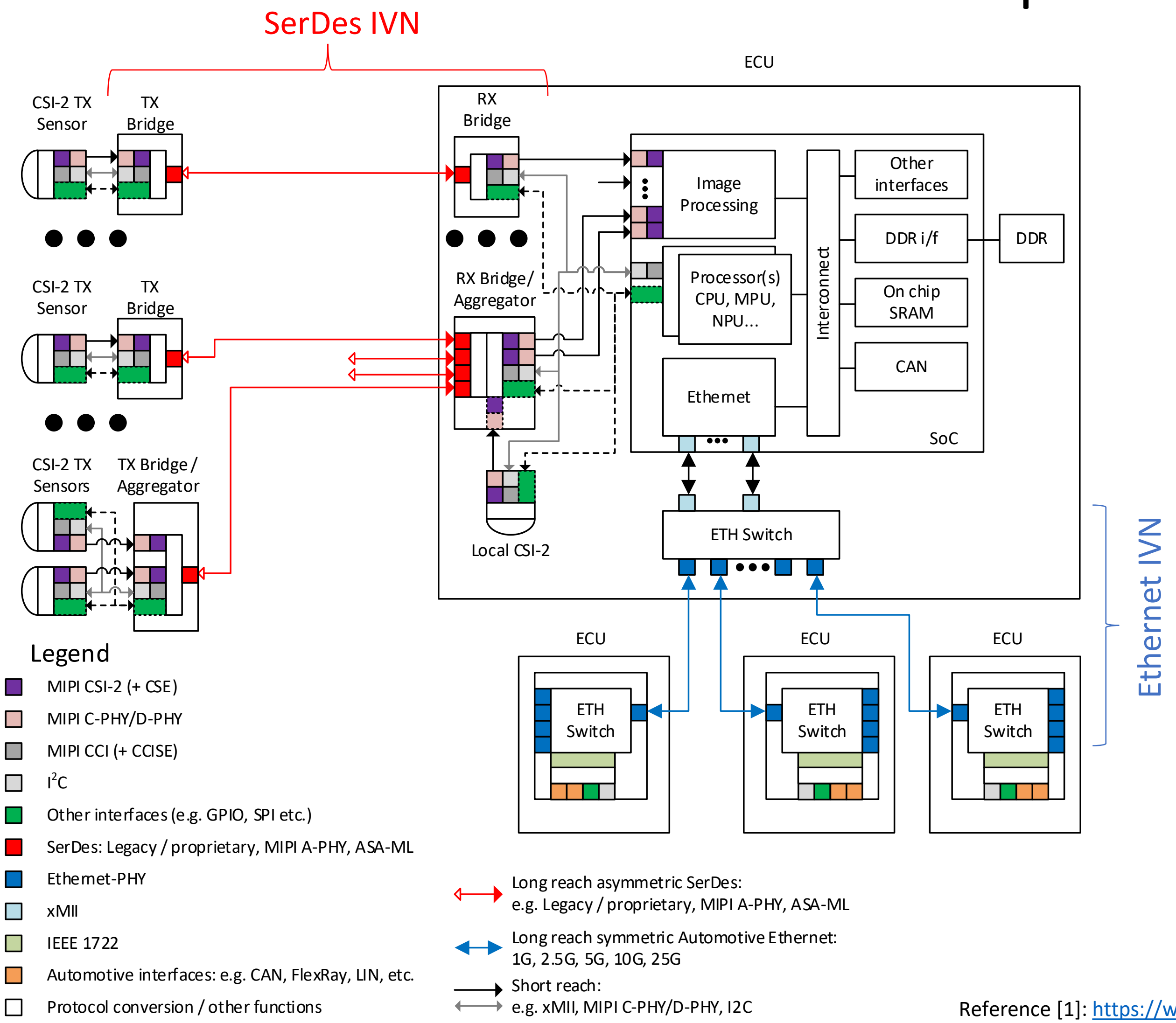
Purpose & Scope

- Attempt to reply to questions raised in CFI presentation [1]
  - What does the evolution to zonal architecture need?
  - Is the Camera side PHY same as the network side?
  - What data rate(s) are needed?
- Current architecture for Camera/Sensors IVN
- Sensor SerDes and aggregation options

Reference [1]: https://www.ieee802.org/3/cfi/0723_1/CFI_01_0723.pdf

Current architecture: separate Camera & Ethernet IVN



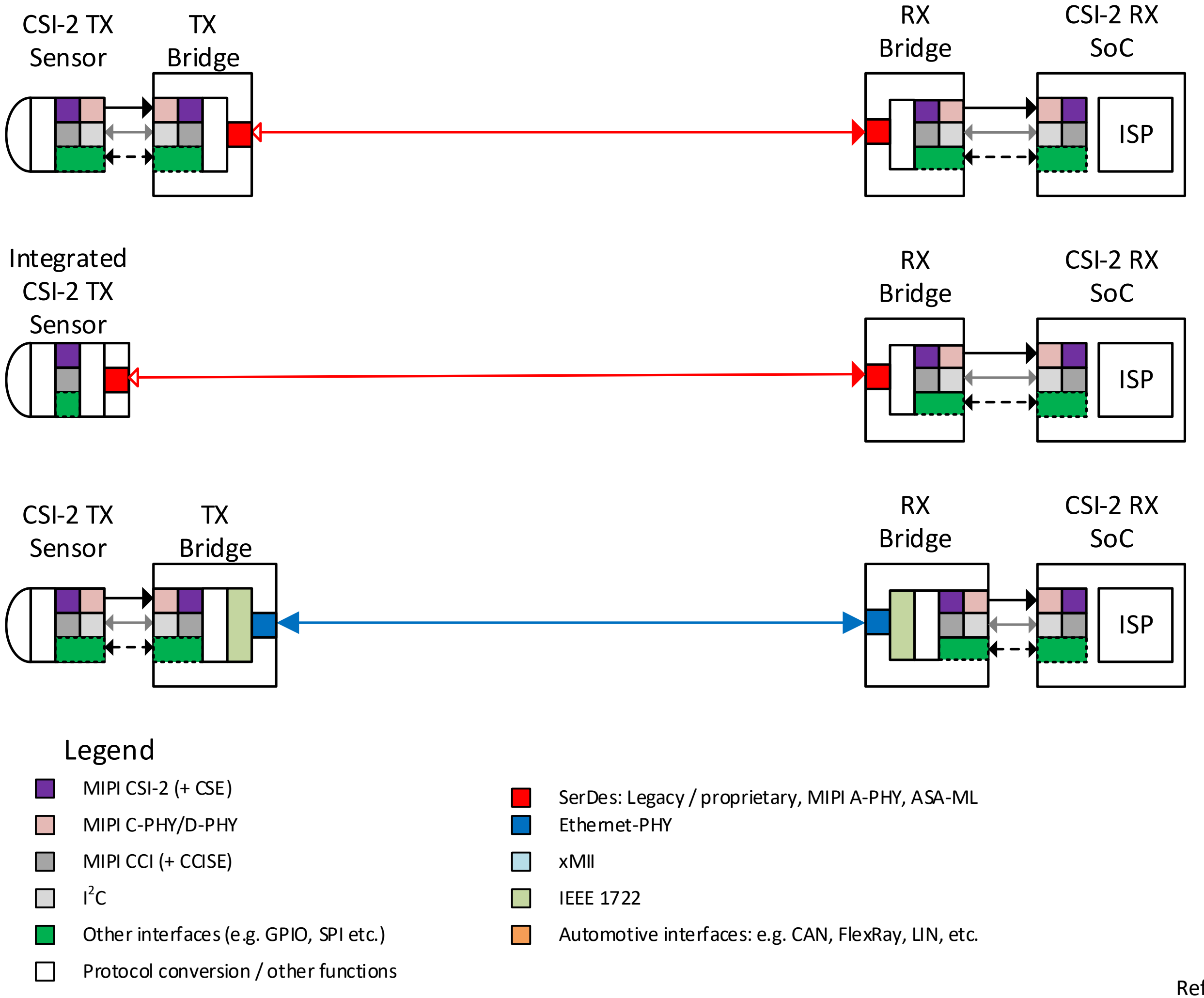
Example diagram

- Sensor SerDes IVN is separated from Ethernet IVN
  - Sensor SerDes IVN > 32Gbps
  - Ethernet IVN without sensors ≤ 10Gbps
  - Power delivery to Sensors
- Direct path from sensors to central ECU image processing
  - No SW overhead
  - Lowest latency, complexity/cost and power
  - Simple SerDes IVN → simple QoS
- Highly asymmetric traffic
  - Increasing number of sensors > 16 → sensor aggregation required to reduce # cables and input ports on SoC
  - High throughput aggregated sensors traffic to SoC MIPI® CSI-2SM RX port. Upto ~41Gbps / CSI-2 RX Port with C-PHY[1]
  - Control traffic: Mbps range
- PHY agnostic end-to-end FuSa and Security protection[2] with MIPI CSESM / CCISESM

Reference [1]: https://www.mipi.org/specifications/c-phy

Reference [2]: https://2384176.fs1.hubspotusercontent-na1.net/hubfs/2384176/Automotive-Workshop/MIPI-2022-Automotive-Workshop-MASS.pdf

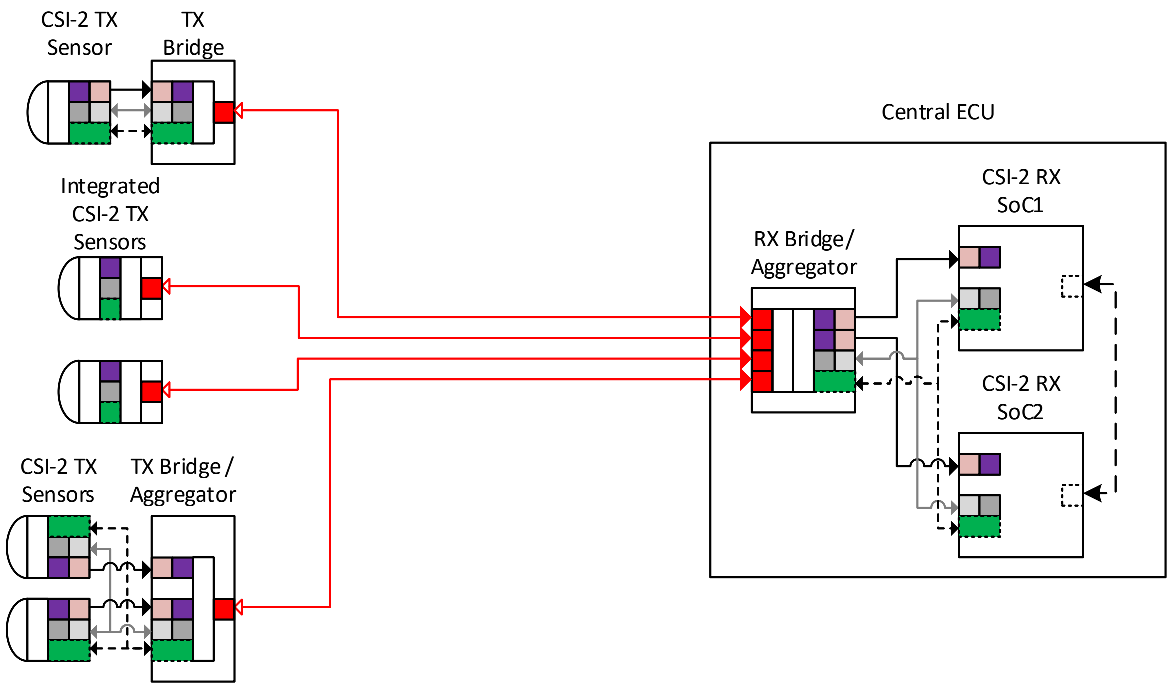
Sensor SerDes options (simple case)



- Protocol: MIPI CSI-2
  - De-facto standard used in billions of devices
  - Used for Camera, Radar and Lidar
  - MIPI CSE for end-to-end FuSa & Security extensions
- Long reach PHY choice:
  - SerDes: Legacy, MIPI A-PHY, ASA-ML
    - Native PHY integration possible[1]
  - Ethernet
  - Tunnels several interfaces over single cable
- Short reach PHY
  - Always MIPI C-PHY or D-PHY
  - May differ between TX and RX
    - e.g. CSI-2 TX with D-PHY; CSI-2 RX with C-PHY
- Point to point direct connection to ISP for lowest latency

Reference [1]: https://www.mipi.org/press-releases/mipi-asa-enter-liaison-agreement-to-enable-native-mipi-csi-2-implementation

Sensor aggregation with Sensors SerDes

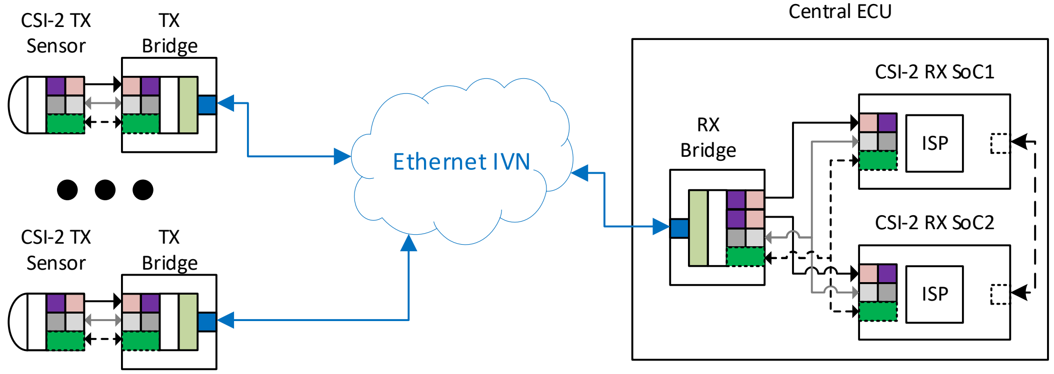


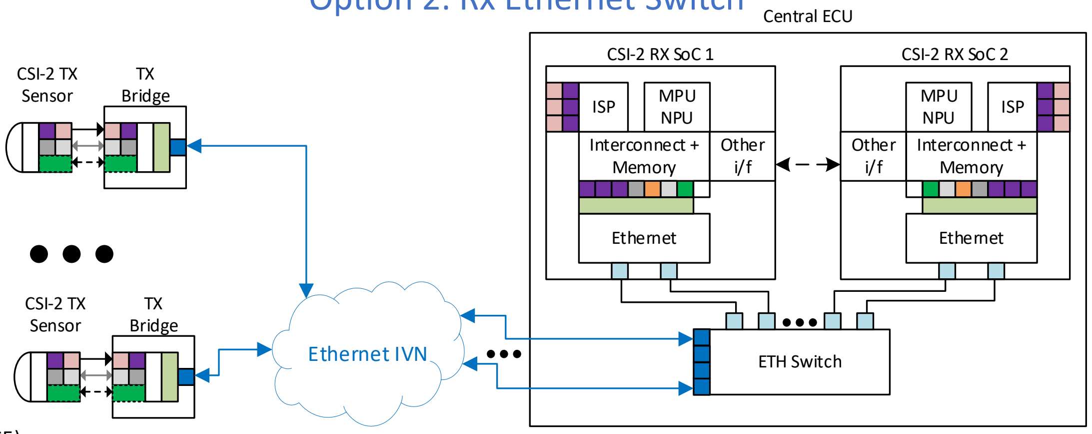
Legend

- MIPI CSI-2 (+ CSE)
- MIPI C-PHY/D-PHY
- MIPI CCI (+ CCISE)
- I²C
- Other interfaces (e.g. GPIO, SPI etc.)
- Protocol conversion / other functions
- SerDes: Legacy / proprietary, MIPI A-PHY, ASA-ML
- Ethernet-PHY
- xMII
- IEEE 1722
- Automotive interfaces: e.g. CAN, FlexRay, LIN, etc.

- Aggregation can be done both on the TX side and on the RX side.
- RX aggregation requires very high throughout on short reach PHY to SoC.
  - Upto ~41Gbps per aggregated CSI-2 RX port
  - RX throughput is ~N x TX throughput
- Multicast aggregated streams to multiple SoCs
- Simple QoS with effective use of CSI-2 Virtual Channels
- Control channel aggregation over Long Reach PHY reduces the effective throughput, when I²C clock stretching is used
- Control channel will require more deterministic latency for Radar/LiDar, when processing will move to central ECU

Sensor aggregation with Ethernet – two options





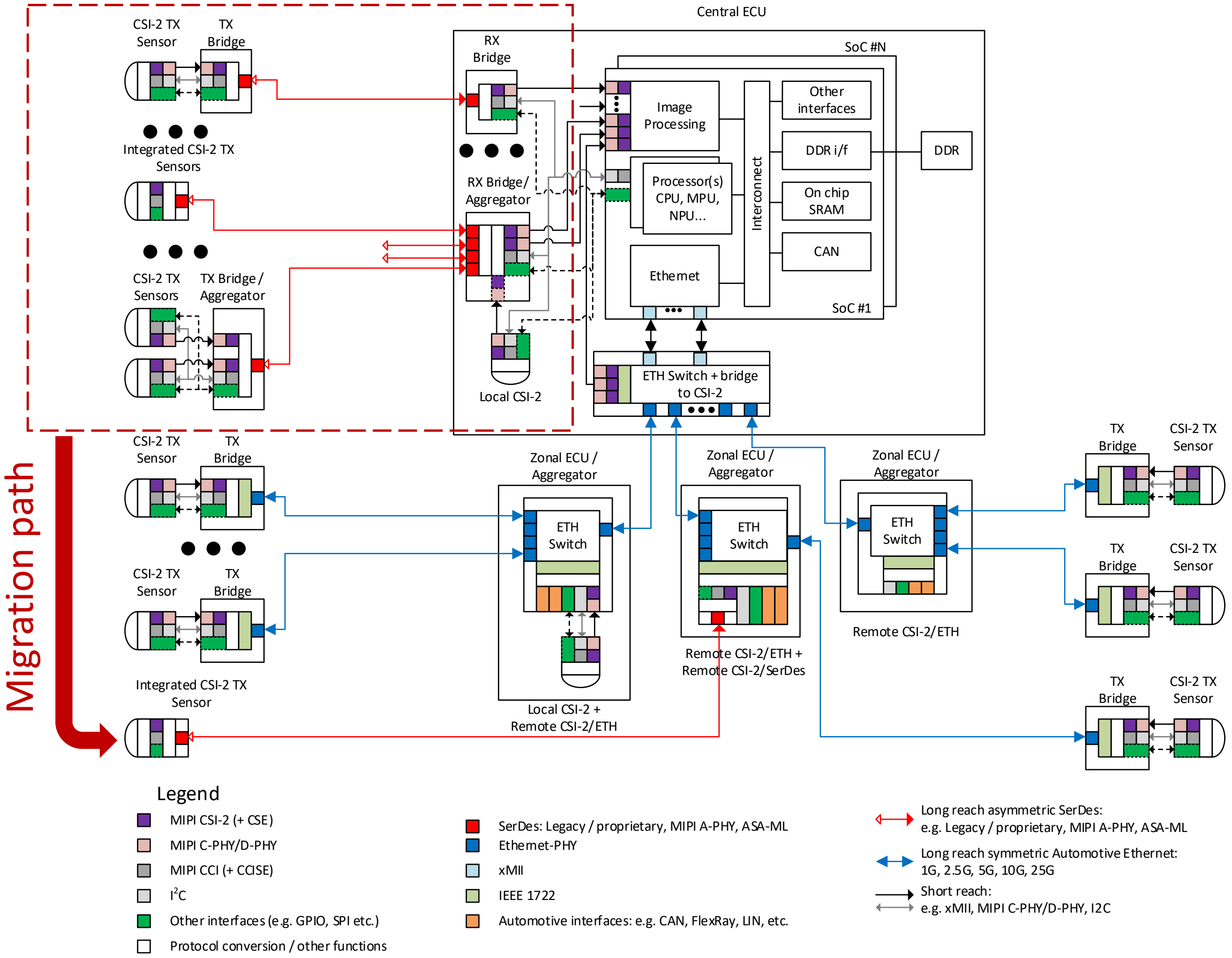
Legend

- MIPI CSI-2 (+ CSE)
- MIPI C-PHY/D-PHY
- MIPI CCI (+ CCISE)
- I^2C
- Other interfaces (e.g. GPIO, SPI etc.)
- Protocol conversion / other functions
- SerDes: Legacy / proprietary, MIPI A-PHY, ASA-ML
- Ethernet-PHY
- xMII
- IEEE 1722
- Automotive interfaces: e.g. CAN, FlexRay, LIN, etc.

- Aggregation can be done anywhere in the Ethernet IVN.
- Aggregated RX Ethernet requires very high throughout ≥ 32Gbps
- Multicast aggregated streams go to multiple SoCs
- Option 1 – direct connection to the ISP
  - Evolution of current architecture
  - Lower latency than option 2
  - QoS: limited number of streams in RX Bridge.
- Option 2
  - Higher latency than option 1 due to additional ETH frames processing and transfer to ISP
  - QoS: high number of streams. Very high throughput TSN switching
  - Control channel can make effective use of 1722b GBB instead of I^2C, but competes with other streams in SoC and Ethernet IVN
  - SoC likely to keep the direct CSI-2 connection to the ISP for use-cases that require SerDes

Architectural evolution towards converged IVN

Example diagram



- Keep flexibility for CSI-2 aggregation over native CSI-2 VC, SerDes or Ethernet IVN
  - Zonal ECU as aggregator. Processing in Central ECU.
- Direct connection required
  - Early video services to meet regulatory requirements for low latency → Booting
  - Low power / low duty cycle – e.g. intrusion detection, calibration (development & manufacturing)
- Ethernet switching on Central ECU
  - Includes a bridge to CSI-2
  - CSI-2 sensors streams keep the short reach PHY (C-PHY / D-PHY)
  - Other streams use xMII
    - Sensor's control channel with 1722b GBB
- Two types of Asymmetric throughput
  - Very High: Zone ECU to Central ECU
  - High: Sensor to Zone ECU
- Stepwise migration path towards a converged IVN

Summary

- Evolution to Zonal IVN with a Central ECU
  - Re-use of well proven sensor protocol: MIPI CSI-2
  - Protocol extensions provide end-to-end FuSa and Security
  - End to end protections are agnostic to underlying PHY can be used with Legacy SerDes, MIPI A-PHY, ASA-ML and Ethernet
  - Easy migration path for a converged IVN
- Data Rates: camera side PHY is not the same as network side
  - 2 types of asymmetric long reach throughput
    - "Very High": Zone ECU to Central ECU. Examples: 32G/1G or 32G/2.5G
      - With 10G/100M more ports are required
    - "High": Sensor to Zone ECU. Example: 8G / 100M
  - Today short reach throughput is up to ~41Gbps