

Proposal for a 100BASE-T1L PHY using PAM-3 8b6T

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Proposal for 100BASE-T1L PHY Encoding



- PAM3 modulation at 80 MSym/s using 8b6T coding in conjunction with an 8N/8N+1 block code and with a low latency mode and a burst error protection mode
 - Using the list of non-negative disparity codewords in <u>ctl_data_code_groups_07152024</u>
 - This file has 256 lines and each line has 7 entries.
 - The first entry is the 8-bit binary selection
 - The remaining 6 entries provide the ternary values for the code-group
 - The control of running disparity on the transmit side as described in slide 3
 - The low latency mode using a 16B/17B block code as described in slide 4
 - The burst error protection mode using a 64B/65B block code and a RS (128, 122, 3, 8) FEC code as described in slide 5
 - The sequence of transmit bits and symbols is constructed as described in slides 3 to 6

Control of Running Disparity



- ► The running disparity (RD) at the transmitter is controlled as follows
 - Each 8-bit value from the encoder is associated with a 6-tuple with non-negative disparity
 - If the 8-bit value from the encoder is associated with a 6-tuple with zero disparity, then the 6-tuple is transmitted as is
 - If the 8-bit value from the encoder is associated with a 6-tuple with positive disparity, then the following rules apply
 - If RD is negative, then the 6-tuple associated with the 8-bit value from the encoder is transmitted as is
 - If RD is positive, then the 6-tuple associated with the 8-bit value from the encoder is negated before transmission
 - If RD is zero, then a pseudo random Boolean value derived from the scrambler determines whether to negate the 6-tuple before transmission
 - RD is recomputed after transmission of each 6-tuple

Low Latency Mode 100BASE-T1L PHY



- ▶ Use PAM-3 modulation with an 8b6T code at 80 MSym/s
 - Use an 8N/8N+1 block code with N = 2: a 16B/17B block code
 - With L = 15 and a data block size of 15 x 16 = 240 bits
 - With L = 15 and 1 x OAM bit we have 15 x 17 + 1 = 256 bits after the block code
 - Transmitted as 32 x 8b6T symbols
 - The symbol rate is (256/240) x (6/8) x 100 = 80 MSym/s

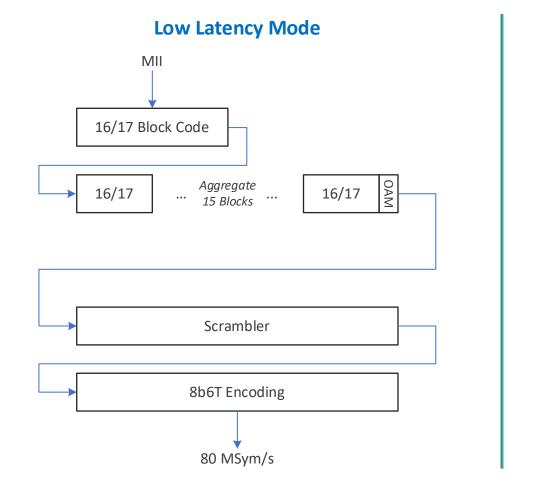
Burst Error Protection Mode 100BASE-T1L PHY



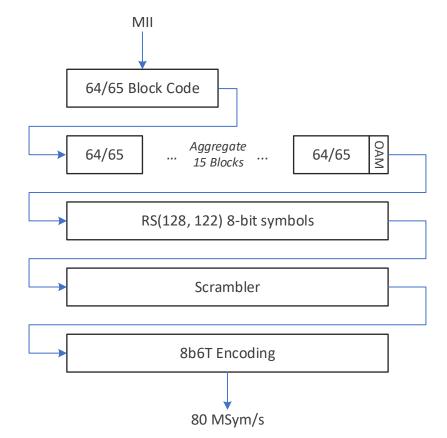
- ▶ Use PAM-3 modulation with an 8b6T code at 80 MSym/s
 - Use an 8N/8N+1 block code with N = 8: a 64B/65B block code
 - Use a Reed Solomon FEC code over a Galois Field GF(2⁸): RS(128, 122, 3, 8)
 - With 3 correctable symbols for 225 ns of burst error protection
 - The details of RS FEC is described on slide 5 of <u>Tingting_3dg_02_16_07_2024</u>
 - With L = 15 and a data block size of 15 x 64 = 960 bits and thus a block length of 9.6 μ s
 - With L = 15 and 1 x OAM bit we have 15 x 65 + 1 = 122 x 8 = 976 bits after the block code
 - And a total RS block size of 128 x 8 = 1024 bits
 - Transmitted as 128 x 8b6T symbols
 - The symbol rate is (1024/960) x (6/8) x 100 = 80 MSym/s

Block Diagram of Transmit Path for each Mode





Burst Error Protection Mode



*The scrambler and OAM details to be defined