Jitter Specifications for 1000Base-T

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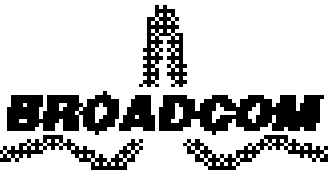
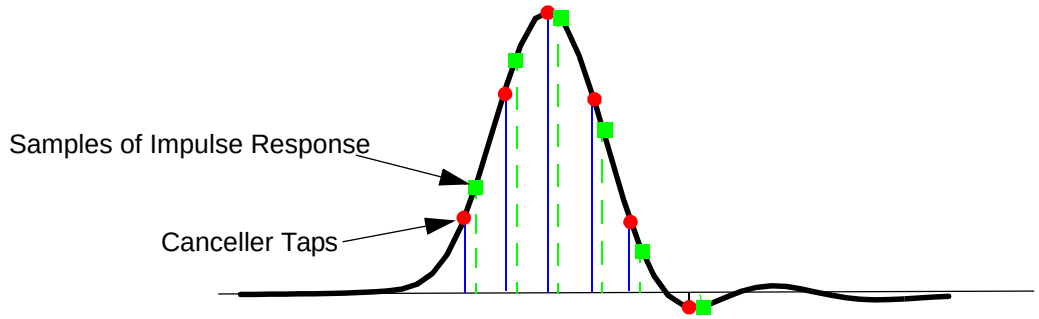


Jitter Issues in Echo Canceller Based Systems

- **Jitter degrades the performance of the echo and NEXT cancellers, because it creates a transient mismatch between the samples of the echo or NEXT impulse response and the taps of the canceller.**



- **This effect has been extensively studied in the literature [1].**
- **This is an issue for both baseband and passband systems.**

Jitter Issues .... (continued)

- **Although DSP based jitter compensation techniques exist [2,3], the simplest solution is to use low jitter phase locked loops for timing recovery.**

- **As a result of the use of echo cancellation, jitter specifications for 1000Base-T will have to be significantly tighter than they are for 100Base-TX.**

[1] D.D.Falconer, "Timing jitter effects in digital subscriber loop echo cancellers: Part I - Analysis of the effect," IEEE Trans. Commun., vol. COM-33, No.8, August 1985, pp.826-832.
[2] D.G.Messerschmitt, "Asynchronous and timing jitter insensitive data echo cancellation," IEEE Trans. Commun., vol. COM-34, Dec.1987, pp.1209-1217.
[3] O.E.Agazzi et al. "A single-chip ANSI standard ISDN U-interface transceiver," Proceedings of the 1992 Custom Integrated Circuits Conference.

A Possible PLL Implementation for 1000Base-T

- **Phase locked loops based on phase interpolation of a crystal oscillator have been extensively used in 100Base-TX transceivers, read channel devices for magnetic recording, etc.**
- **Jitter in this type of PLL comes from substrate noise pick up by the ring oscillator and the frequency multiplier to up the frequency of the crystal.**
- **Low jitter implementations have been demonstrated. Reynolds [1] described a 320MHz PLL with 9ps rms and 60ps peak-to-peak jitter in 1994.**
- **Even better performance is possible today (50ps peak to peak jitter for a 250MHz phase controlled oscillator is reasonable in today's technology, according to experts).**
- **[1] D.Reynolds, "A 320 MHz CMOS triple 8 bit DAC with on-chip PLL and hardware cursor," IEEE Journal of Solid-State Circuits, vol.29, No.12, December 1994, pp.1545-1551**

Jitter in 1000Base-T

- **The following sources of jitter exist in a 1000Base-T transceiver:**
- **Intrinsic jitter of the phase controlled oscillator (caused by switching noise pick up). This is 50ps or less (possibly at high frequencies).**
- **Phase steps introduced by the timing recovery system in order to control frequency and phase. If the baud clock is interpolated by 64, the phase steps are:**

$$\Delta t = 8ns/64 = 125ps$$

- **The frequency of phase steps needed to pull the baud clock by 100ppm is:**

fstep = fbaud x 1e-4 x 64 = 800KHz

- **A 125ps phase step causes tolerable degradation in PAM-5.**

Criteria to Limit Jitter in 1000Base-T

- **A reasonable criterion to establish the range of permissible jitter in the received signal is to demand that the instantaneous frequency deviation caused by sinusoidal jitter $(\Phi/2)\sin(2\pi ft)$ of peak-to-peak amplitude Φ and frequency f shall not exceed 100ppm of the baud clock f_B. Then:**

$$2\pi f\Phi/2 = 10^{-4} f_B$$

$$\Phi \text{ [radians]} = 10^{-4} f_B/\pi f$$

$$\Phi\text{[Baud Periods]} = 10^{-4} f_B/2\pi^2 f = 12500/(2\pi^2 f)$$

Criteria to Limit Jitter in 1000Base-T
(continued)

- However, the limit on high-frequency jitter should not be less than 1/64 of the baud period, to allow implementation of analog phase interpolation based PLLs with reasonable complexity (64-stage ring oscillators)
- It should also allow for the intrinsic jitter of the frequency multiplier and ring oscillator (~50ps peak to peak)
- Therefore we establish the upper limit for high-frequency peak to peak jitter at 0.02 baud periods (=160ps)
- Also, the low-frequency jitter should be bounded to a reasonable value. We propose 0.3 baud periods (2.4ns).

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Permissible Jitter in Signal