Considerations for Electrical Interfaces Beyond 200Gb/s per lane

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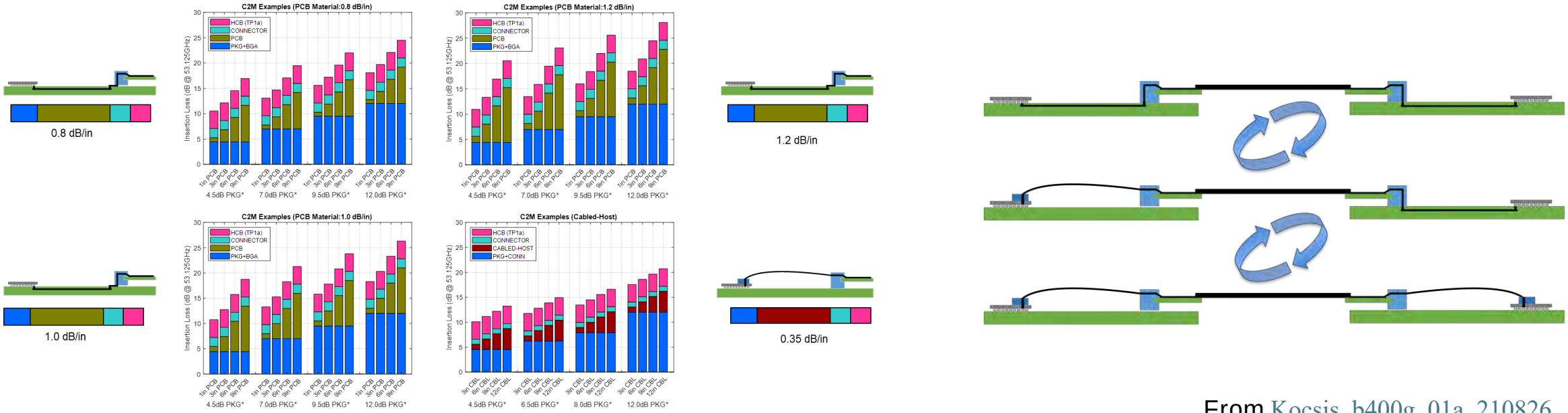
Motivation

- Goal: To stimulate discussion related to physical layer specification
- Assumptions: data rate, modulation, form factor are unknown



From Kocsis_b400g_01a_210826

Standardizing Passive Copper Cabling

IEEE Project	“3bj”	“3cd”	“3ck”	“3dj”	TBD
Timeline	2014	2018	2021	2025	-
Per-lane Rate	25G	50G	100G	200G	TBD
Modulation	NRZ	PAM-4	PAM-4	PAM-4	TBD
Insertion Loss	35dB	30dB	28.5dB	40dB*	*40dB***
Reach Target	5m Cu Cable	3m Cu Cable	2m Cu Cable	1m Cu Cable	*1m Cu Cable***

* die-to-die budget
** no formal adoption/consensus

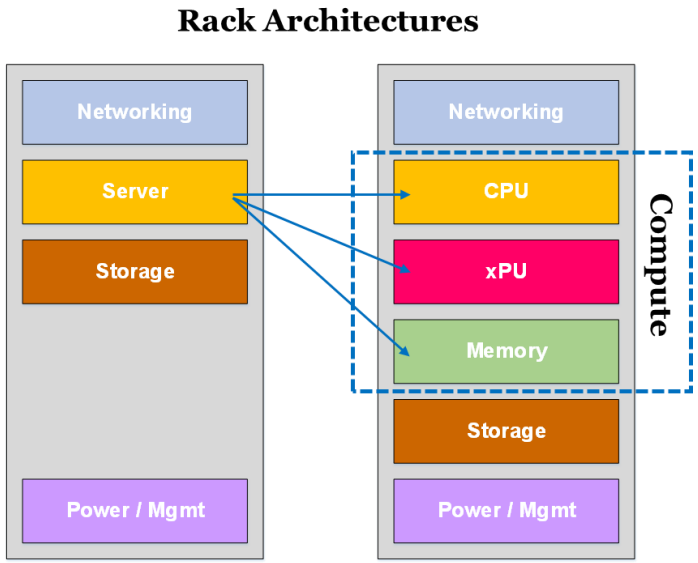
Standardizing Chip-to-Module

IEEE Project	“3by”	“3cd”	“3ck”	“3dj”	TBD
Timeline	2016	2018	2021	2025	-
Per-lane Rate	25G	50G	100G	200G	TBD
Modulation	NRZ	PAM-4	PAM-4	PAM-4	TBD
Host Insertion Loss	8.5dB	8.5dB	13.5dB	28.2dB*	TBD*
Nyquist	12.89GHz	12.89GHz	26.56GHz	53.13GHz	TBD

* ”die-thru-MDI” budget

Ethernet for AI

- (3) Types of Networks
  - Front-End / Traditional
  - Back-End / Scale-up
  - Back-End / Scale-out
- Bandwidth Density is critical
- Interconnect requirements are unknown
  - Modular compatibility
  - Architectural compatibility
  - Latency/Power



Beyond 200Gb/s per lane…

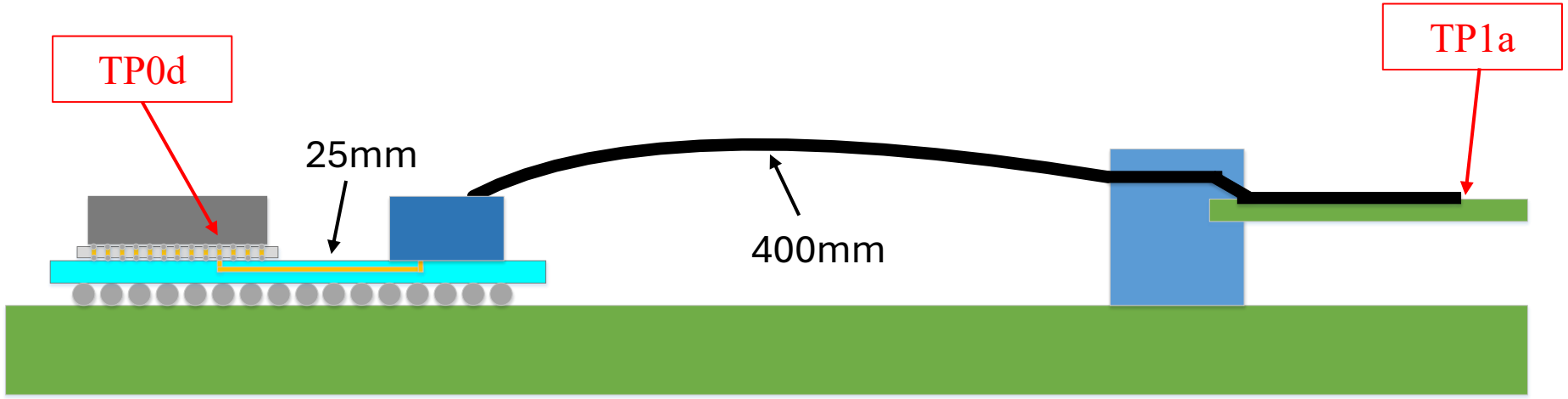
	"224G"				"448G"		
Number of signal levels (M)	8	6	4		8	6	4
Bits per symbol	3	2.5	2		3	2.5	2
Signaling rate*, GBd	75	90	112		150	180	224
Nyquist frequency, GHz	37.5	45	56	…	75	90	112

* Signaling rate rounded for simplicity

For now, we can evaluate trade-offs of channel performance (bandwidth) at a per lane basis

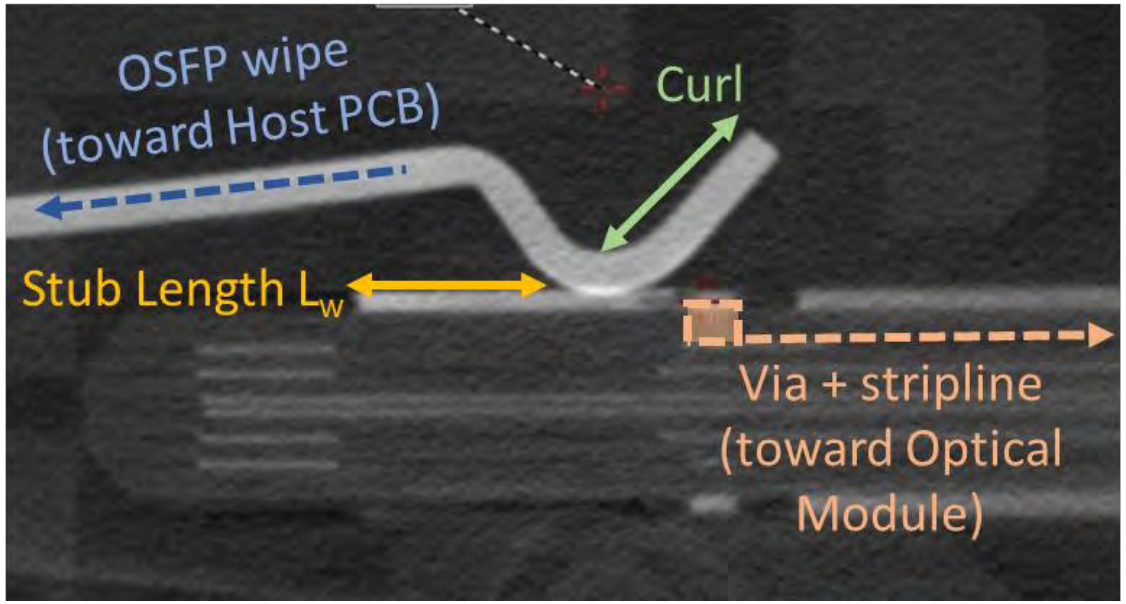
Defining the Electrical Interface

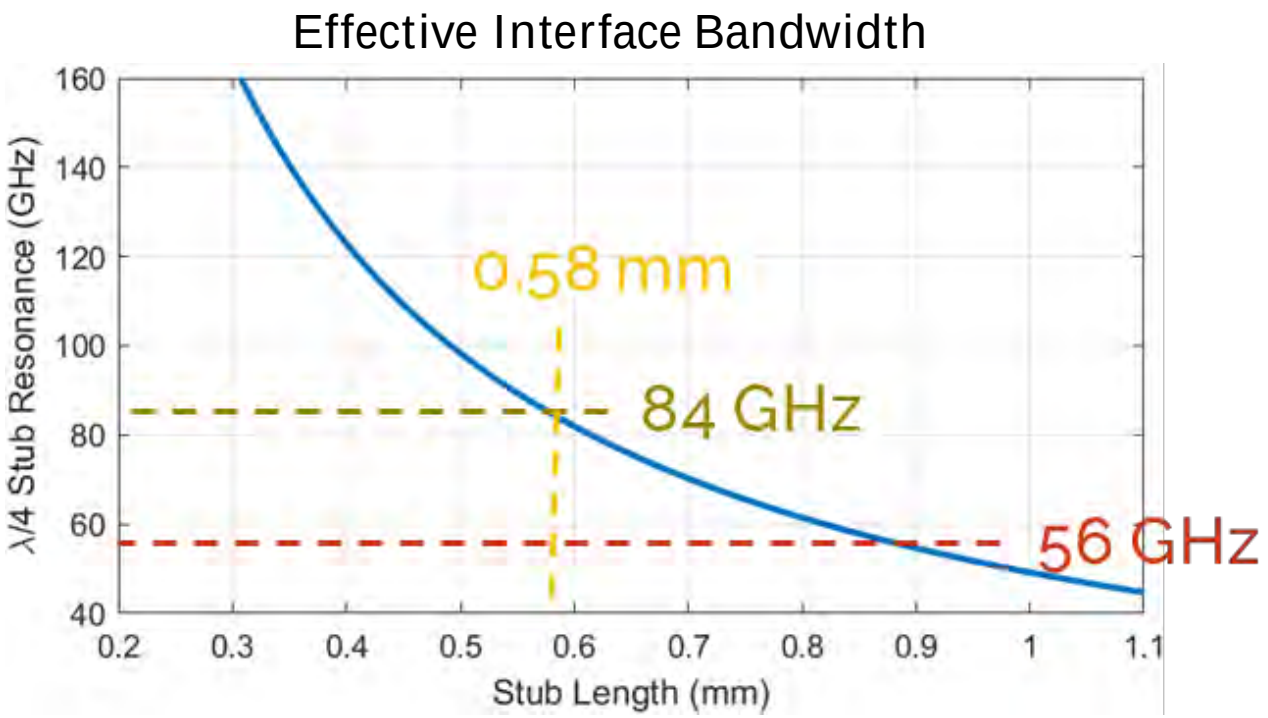
At 200Gb/s there are two bottlenecks in need of attention:
(1) Chip package breakout
(2) Front-panel interfaces



The channels in this contribution will focus on implementation options for the topology above.

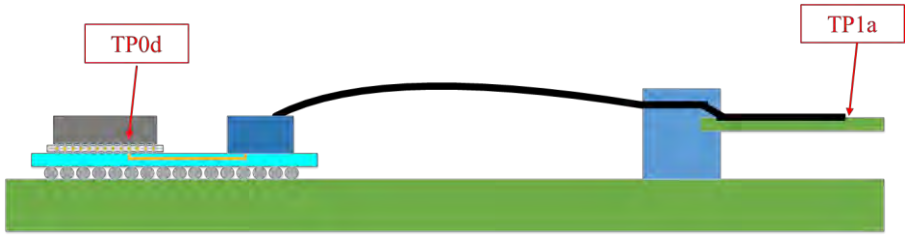
Pushing Limits for Today's Pluggable IO

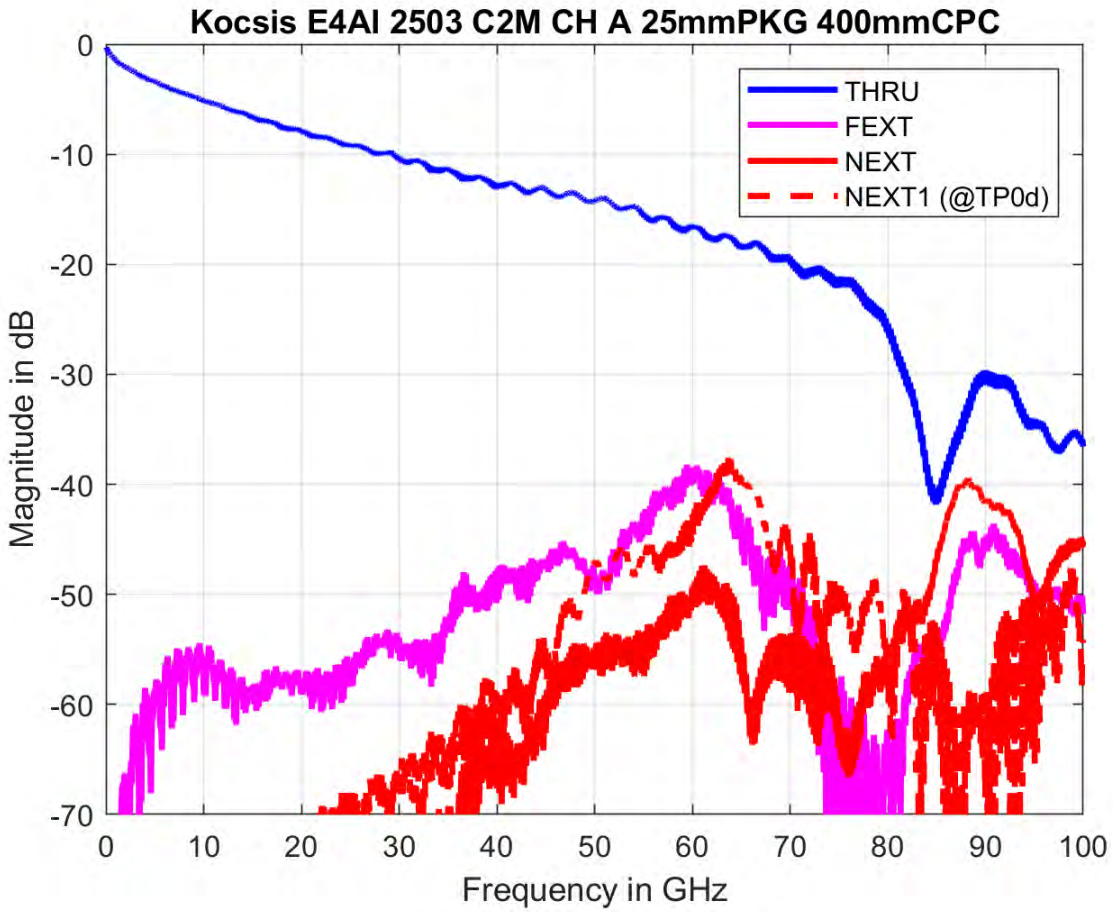


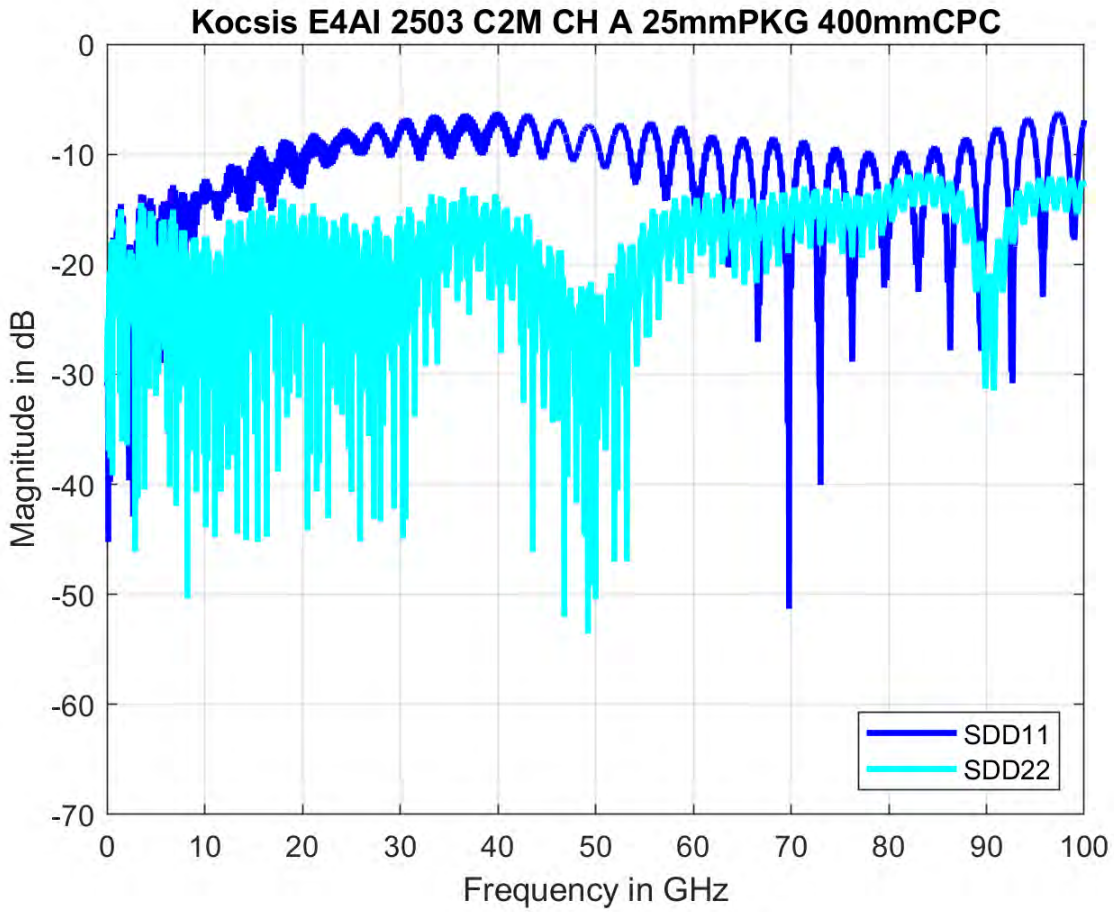


Channel “A”

“Limit of Today’s Pluggable”

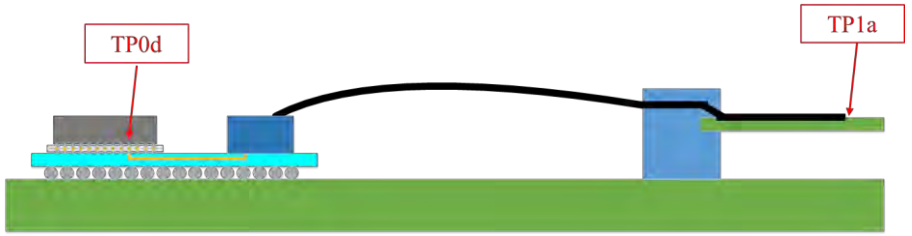


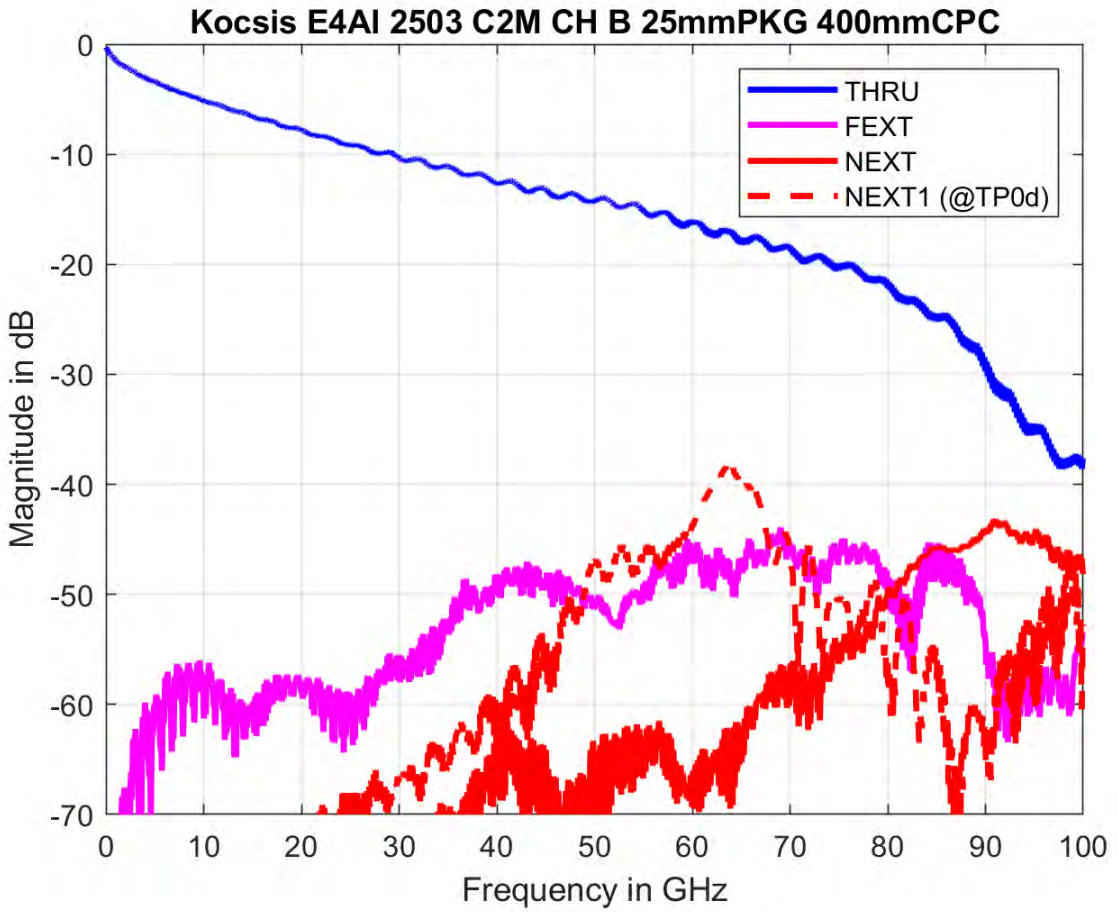


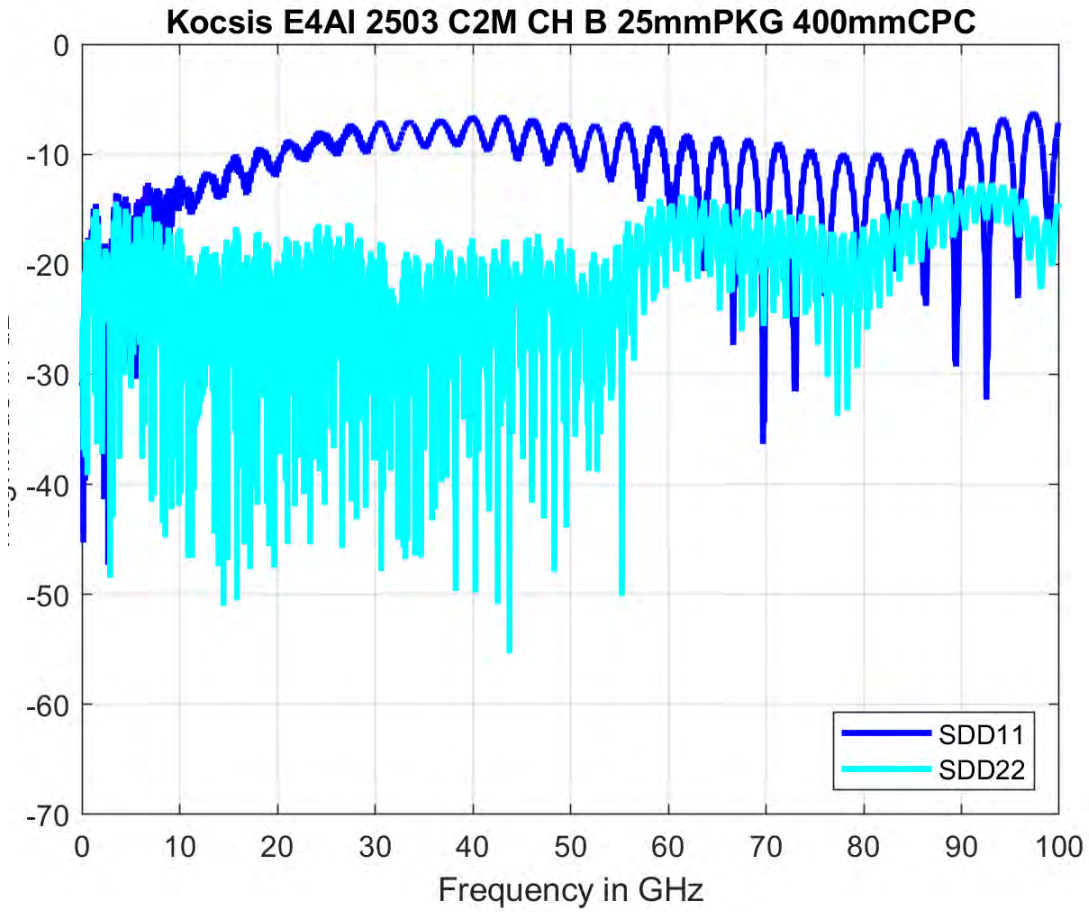


Channel “B”

“New Pluggable, Familiar Feel”

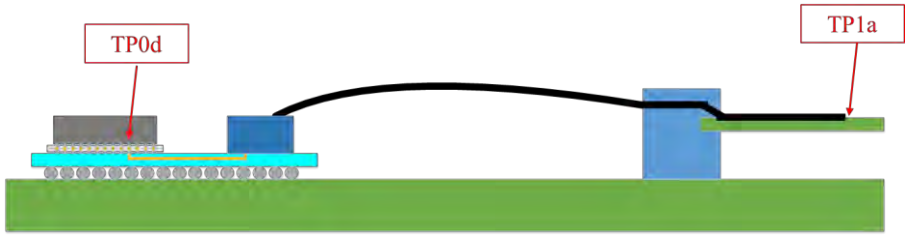


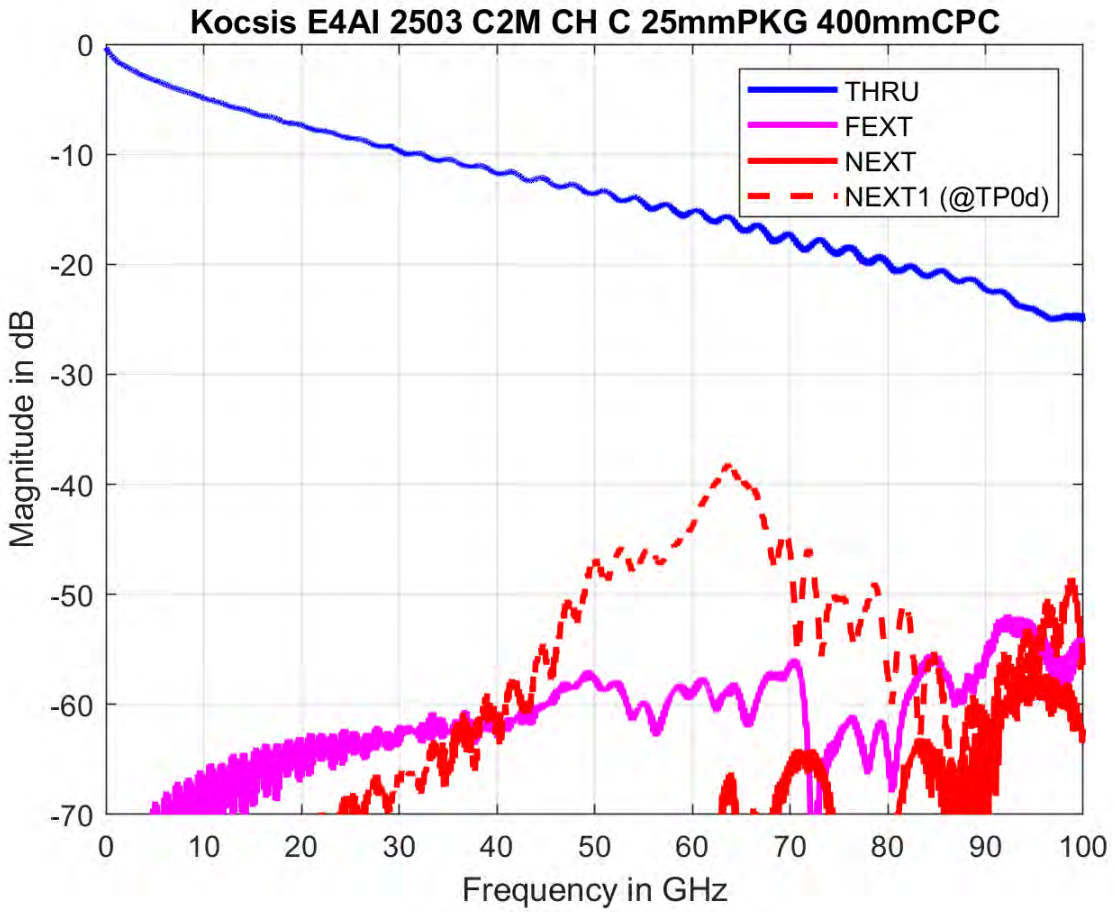


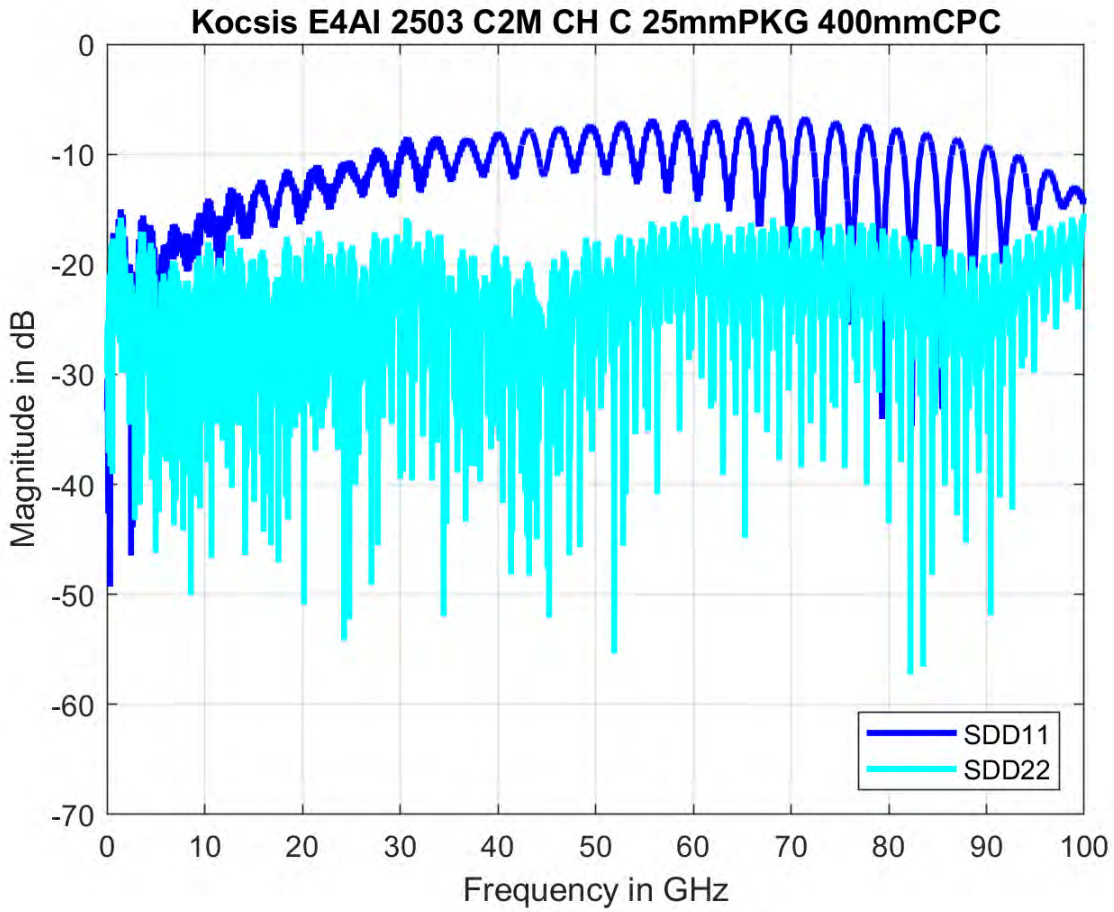


Channel “C”

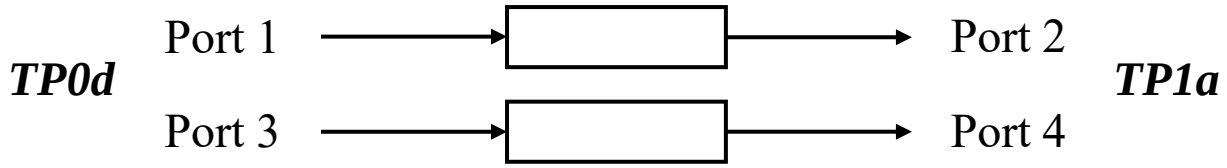
“New Pluggable, New Paradigm”







E4AI Channels



- (1) THRU, (1) FEXT, (2) NEXT for each “type” (A,B,C)
  - (1) NEXT at TP0d, (1) NEXT at TP1a
- 10MHz – 100GHz (10MHz steps)

- Model Nomenclature:
  “Kocsis_E4AI_2503_C2M_CH_[#]_25mmPKG_400mmCPC_[#].s4p”

A, B, C ***THRU, FEXT, NEXT, NEXT1***

Discussion

- Goal: To stimulate discussion related to physical layer specification

- Feedback on model bandwidth
- Feedback on topology relevance
- Thoughts on reference/compliance points
- Opinions on data rate and modulation