IEEE 802.3 PDCC Ad Hoc
“Compatibility of PSE with non-PD MDI”

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Purpose

- IEEE Std 802.3-2022

> **1.4.358 IEEE 802.3 Power over Ethernet (IEEE 802.3 PoE):** A system consisting of one PSE and one PD that provides power across balanced twisted-pair cabling. (See IEEE Std 802.3, Clause 33 and Clause 145.)

- PSEs may be connected to MDIs that are not PDs
  - Connection of *apparently compliant* devices can result in **damaged devices**
    - On first power up or on first cable attachment

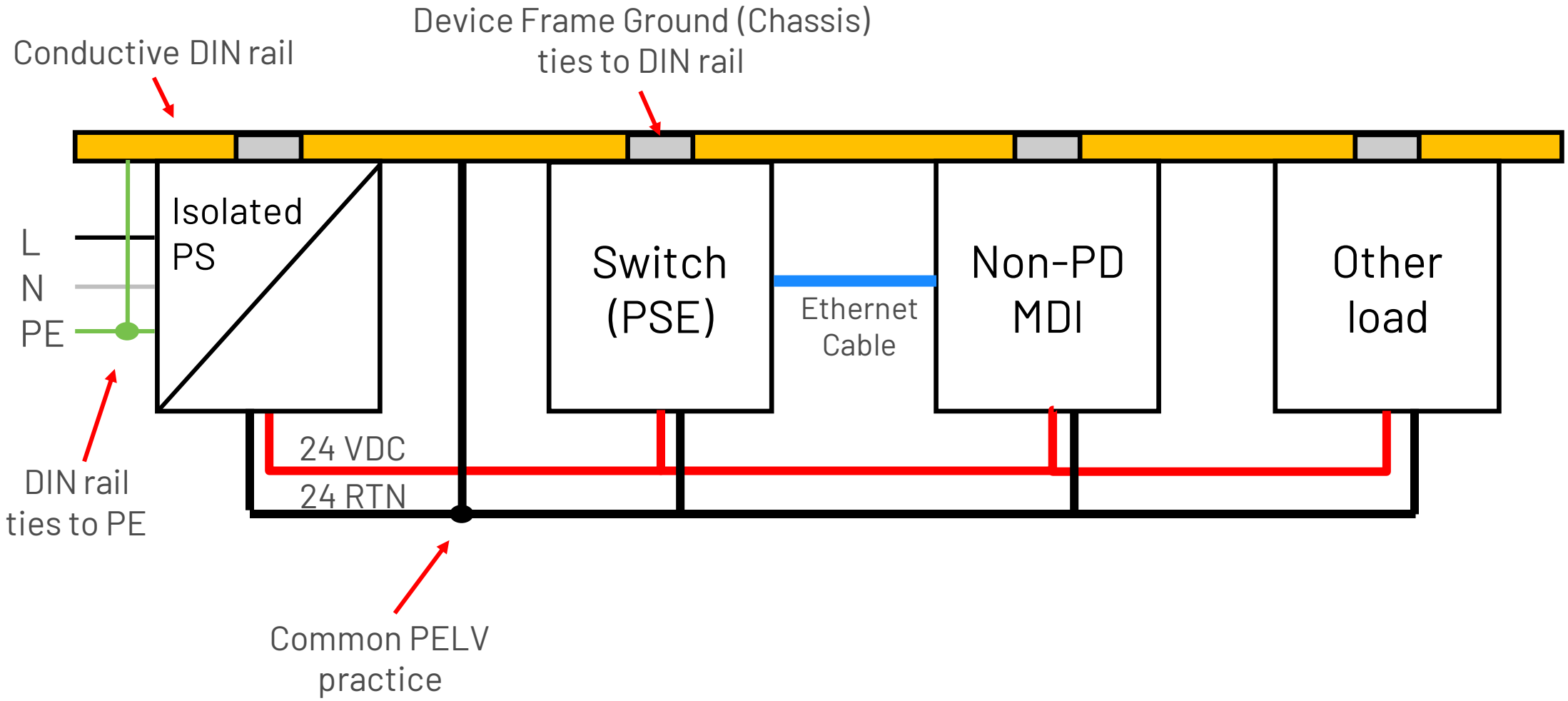
- Describe the problem…

Numerous PoE Alternative Circuits

- Power on alternative pair sets
- Power on 2-pairs or on 4-pairs
- Swapped polarity for MDI and MDI-X pinouts
- Power on multiple cables in network interface devices (NID)

Presentation focuses on a single PSE+ pair.

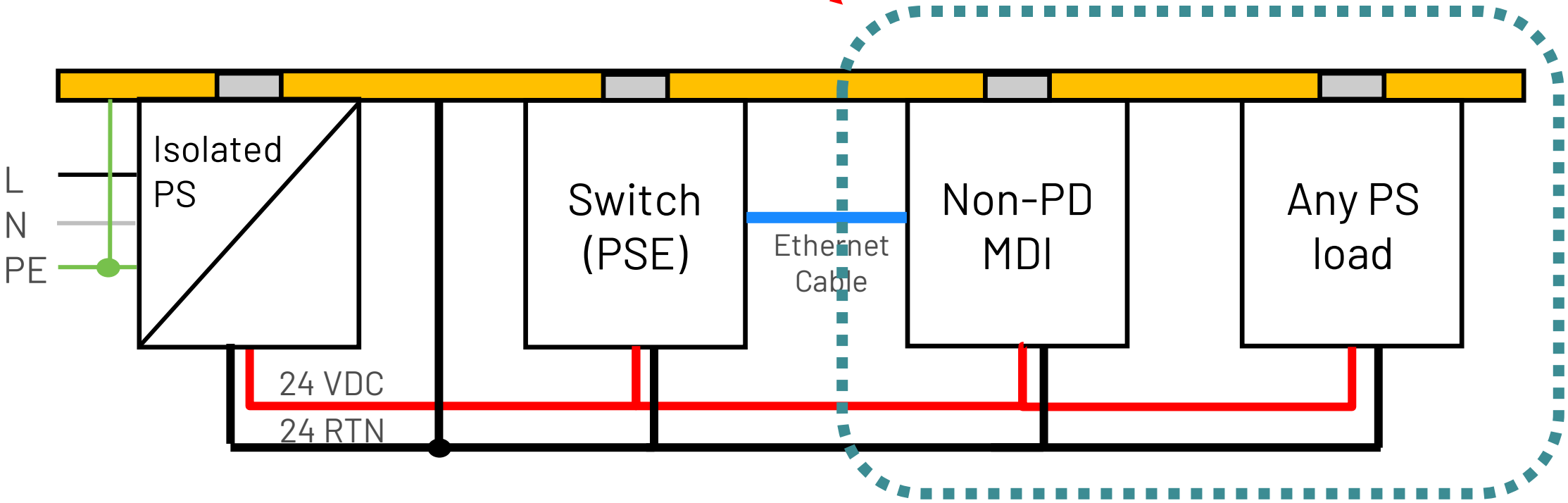
Example Installation



Incompatibility Situation

- These devices can be **damaged** by the PSE
  - Separate isolated power supplies are cost prohibitive
  - Unmanaged switches always have PoE present

- PSE voltage may be present <u>during</u> detection (no false triggering)
- There is no clear violation of IEEE requirements (no "shall")

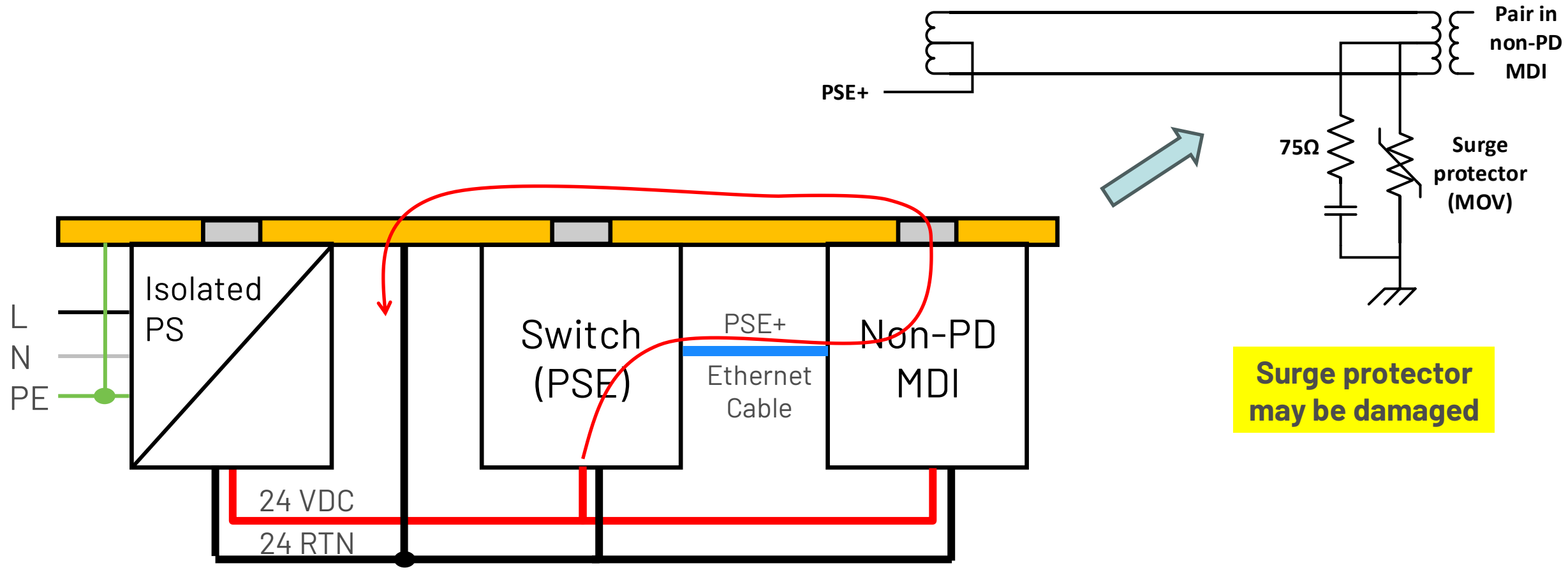


Problem Scope

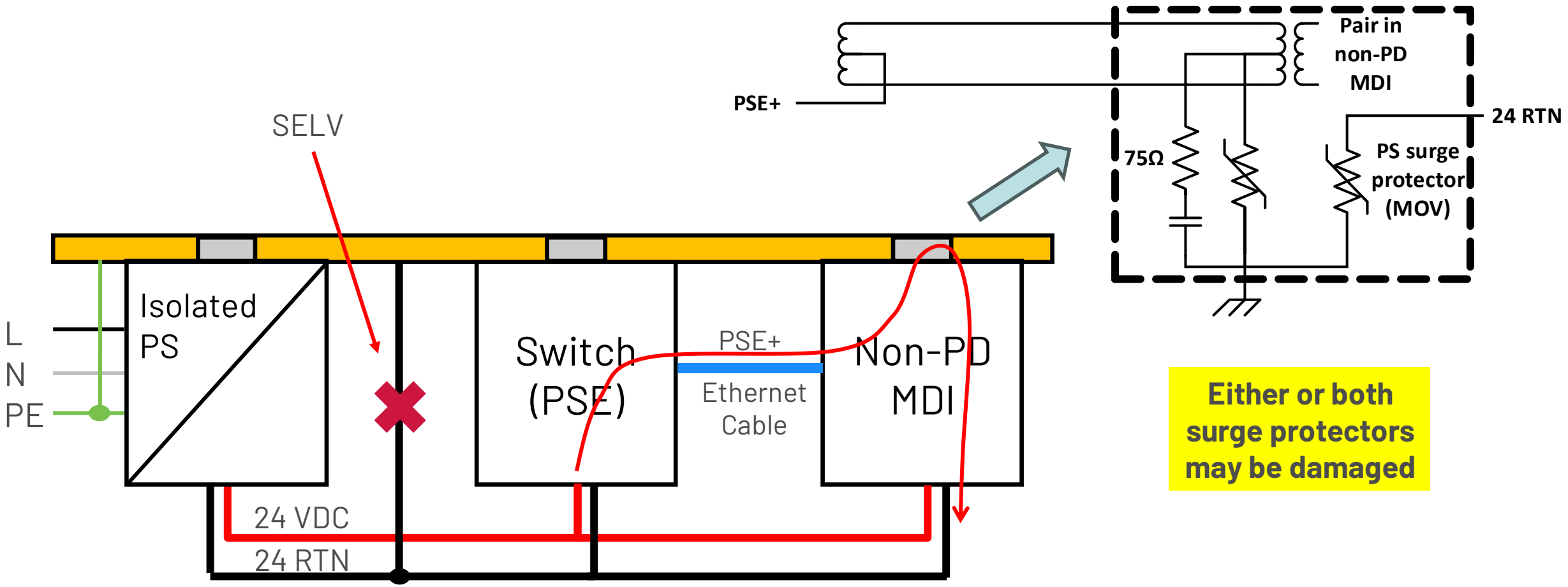
- PoE switches from 5 manufacturers are reported to exhibit problems
  - None of the data sheets are clear on installation rules

- One switch measures the following on PSE+ to FG:
  - Voc = 50 V, Isc > 20 mA, i.e., > 1W
    - Damaged MOVs can only tolerate 0.3 W continuous
  - Oscilloscope confirms detection pulses
    - PSE- is approximately 48 V during pulses
  - SELV installation minimizes failure modes

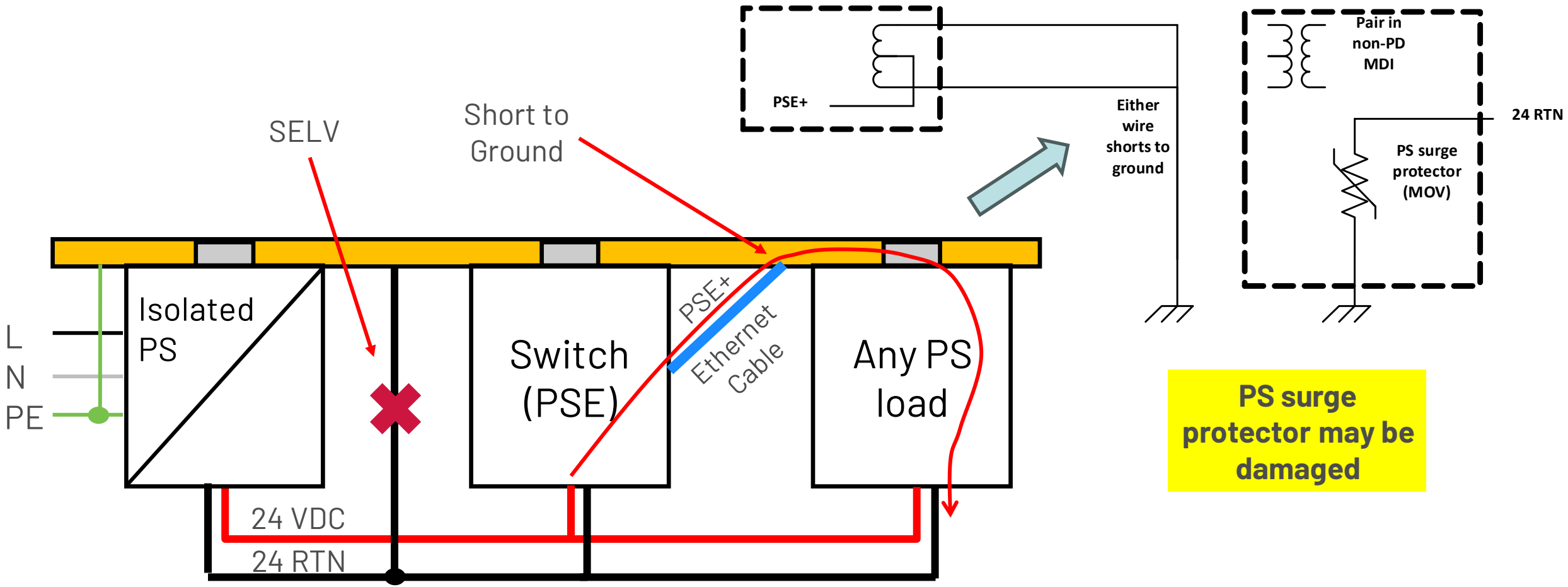
Primary Current Path



Secondary Current Path



Tertiary Current Path



MDI Questions

- Isn’t the MDI supposed to be isolated?
- Aren’t MDIs supposed to tolerate PoE voltages?

10BASE-T/Te, 100BASE-TX, and 1000BASE-T are the dominant multi-pair PHYs installed in industrial automation for the foreseeable future.

MDI Isolation Requirement (100BASE-TX)

- IEEE Std 802.3:2022
- Isolation is required
- Isolation exceeds PoE voltages
- IEC 60950-1 (withdrawn) contained the procedure for a) and b) – “no technical change is implied”

25.4.6 Replacement of 8.4.1, “UTP isolation requirements”

A PMD with a MDI that is a PI (see 33.1.3 and 145.1.3) shall meet the isolation requirements defined in 33.4.1 and 145.4.1.

A PMD with a MDI that is not a PI shall provide isolation between frame ground and all MDI leads including those not used by the 100BASE-TX PMD.

This electrical isolation shall meet the isolation requirements as specified in J.1.

NOTE—In the case of a PMD with a MDI that is not a PI, these requirements are equivalent to those found in TP-PMD.

40.6.1.1 Electrical isolation

A PHY with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

A PHY with a MDI that is not a PI shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall meet the isolation requirements as specified in J.1.

J.1 Electrical isolation

Electrical isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz. This test voltage amplitude is raised from zero to the prescribed voltage and held at that value for 60 s.

b) 2250 V dc. This test voltage is raised from zero to the prescribed voltage and held at that value for 60 s.

c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses is 1.2/50 (1.2 µs virtual front time, 50 µs virtual time to half value), such as one produced by a 1.2/50-8/20 combination wave generator, as defined in ITU-T Recommendation K.44.

NOTE 1—If the MDI is also a Clause 33 or Clause 145 PI then see 33.4.1 or 145.4.1 for specific requirements associated with option c).

There shall be no insulation breakdown during the test. Insulation breakdown is considered to have occurred when the current that flows as a result of the application of the test voltage rapidly increases in an uncontrolled manner; that is, the insulation does not restrict the flow of the current. Corona discharge is not regarded as insulation breakdown. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE 2—IEEE Std 802.3-2018 and previous revisions provided references to various editions of the IEC 60950-1 standard for guidance in performing the isolation test for options a) and b). IEC 60950-1 has been withdrawn. References to IEC standards are not essential to performing the isolation test specified in J.1. No technical change is implied by the removal of these references.

NOTE 3—Implementers should consider the effect of whether other ports are terminated or unterminated when testing the insulation of multi-port devices.

MDI Isolation Test Procedure

- IEEE Std 802.3:2018
- Referred to 5.2.2 of IEC 60950-1 for a) and b)

25.4.6 Replacement of 8.4.1, "UTP isolation requirements"

A PMD with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1.

A PMD with a MDI that is not a PI shall provide isolation between frame ground and all MDI leads including those not used by the 100BASE-TX PMD.

This electrical isolation shall withstand at least one of the following electrical strength tests.

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 µs (1.2 µs virtual front time, 50 µs virtual time of half value), as defined in IEC 60950-1:2001 Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE—In the case of a PMD with a MDI that is not a PI, these requirements are equivalent to those found in TP-PMD.

IEC 60950-1 5.2.2 Procedure

- Electric strength is a test of the SOLID INSULATION [e.g., the transformer as a boundary between telecommunication circuits]
- “Components providing a d.c. path in parallel with the insulation to be tested, such as discharge resistors for filter capacitors, voltage limiting devices or surge suppressors, should be disconnected.”
- “To avoid damage to components or insulation that are not involved in the test, disconnection of integrated circuits or the like and the use of equipotential bonding are permitted.”

- The test can be run in a **non-operational state** (parts removed).
- Isolation of MDI to frame ground may not be maintained (**no operational galvanic isolation**) when parts are replaced for operation.

MDI Fault Tolerance

- Multi-pair PHYs
  - Tolerate shorts within transmitter and receiver pairs + tolerate impulses
    - Clause 12, 1BASE-5
    - Clause 14, 10BASE-T/Te
    - Clause 23, 100BASE-T4
    - Clause 32, 100BASE-T2
  - Tolerate shorts across any wires + tolerate impulses
    - Clause 40, 1000BASE-T
    - Clause 55, 10GBASE-T
  - Tolerate shorts across any wires + tolerate impulses + tolerate PSE
    - Clause 113, 25G/40GBASE-T
    - Clause 126, 2.5/5GBASE-T
- Single-pair PHYs
  - Tolerate: shorts across pair + to PoDL voltages + to ground
    - Clause 96, 100BASE-T1
    - Clause 97, 1000BASE-T1
    - Clause 146, 10BASE-T1L
    - Clause 147, 10BASE-T1S
    - Clause 149, 2.5/5/10GBASE-T1

113.8.2.3 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

A 25G/40GBASE-T PHY shall be able to sustain, without damage, connection to a PSE and shall not cause damage to the PSE as defined in 33.2.

Each wire pair shall withstand without damage a 1000 V common-mode impulse of either polarity. The shape of the impulse is 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC 60060. See Figure 40–34 in 40.8.3.4.

Table 96–6—Connection fault

BI_DA+	BI_DA-
No fault	No fault
BI_DA–	BI_DA+
Ground	No fault
No fault	Ground
+50 V dc	No fault
No fault	+50 V dc
Ground	+50 V dc
+50 V dc	Ground

104.6.2 Fault tolerance

The PI for Type A, Type B, Type C, and Type F PSEs and PDs shall meet the fault tolerance requirements as specified in 96.8.3. The PI for Type E PSEs and PDs shall meet the fault tolerance requirements as specified in 146.8.6.

- Common multi-pair PHYs are not required to tolerate PSE voltages.

PSE Questions

- Isn’t the PSE supposed to be isolated?
- Doesn’t the PSE limit current during detection?

PSE Isolation Requirement

- IEEE Std 802.3:2022
  - Specifies J.1 and refers to IEC 60950-1 procedure for options a) and b) – "no technical change is implied" from 2018
  - And substitutes a new impulse option c) from ITU-T K.44
- IEEE Std 802.3:2018
  - Refers to IEC 60950-1 5.2.2 for procedure

  - Isolation test can be run in a **non-operational state** (parts removed).
  - Isolation of MDI to frame ground may not be maintained (**no operational galvanic isolation**) when parts are replaced for operation.

- *Accessible external conductors* are specified in subclause 6.2.1 b) of IEC 60950-1
  - "Part and circuitry that **can be touched by the test finger**…"

- "Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector."

33.4.1 Electrical isolation

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector.

This electrical isolation shall meet the isolation requirements as specified in J.1 with electrical strength test c) details being replaced by: "An impulse test consisting of a 1500 V, 10/700 waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses is 10/700 (10 µs virtual front time, 700 µs virtual time to half value), as defined in ITU-T Recommendation K.44."

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

Disect…

PSE-connected-equipment Isolation

- "Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector."

- PS connects to PSE through non-MDI connector
  - The PSE PS-connector APPEARS isolated from MDI (high resistance) in an unpowered PSE, and is not "accessible"
  - Assuming no isolation, SELV would be "needed" as FG is accessible - but damage can still occur
- This is not a PSE requirement: "any equipment", "needs to"
  - Installation PICS have similar purpose in assuring operation

PSE Current Limit

- Detection current limit is pair-pair and not pair-ground
- The example shows high-side current measurement, which COULD measure current from PSE+ to ground

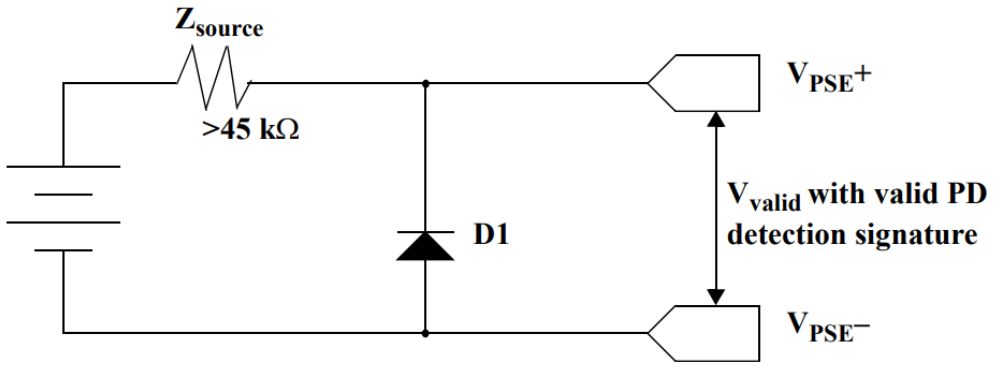


Figure 33–11—PSE detection source

Table 33–4—PSE PI detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30.0	In detection state only
2	Short circuit current	I_{sc}	A		0.005	In detection state only
3	Valid test voltage	V_{valid}	V	2.80	10.0	—
4	Voltage difference between test points	ΔV_{test}	V	1.00		—
5	Slew rate	V_{slew}	V/µs		0.100	—

PSE Switching

- The test switch uses a 4-port PoE Manager from a major vendor
  - PSE+ powers the chip and is supplied directly
  - PSE- is switched internally through a MOSFET on the chip
  - Current is sensed when PSE- is enabled

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.

33.4.1.1.1 Environment A requirements

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

- Low-side or high-side (or both) is inadequate to protect the output
- Current sensing must be considered for each leg

Observations

- The terms “isolated” and “accessible” have very specific meanings. Isolation is tested to frame ground, but protection circuits on each side of the barrier to frame ground are not considered an issue (not violating the isolation barrier). The IEEE isolation requirements are not for functional purposes, and it is apparently possible to design compliant PSE and PD that do not interoperate, and where damage can occur.
- Installation requirements appear inadequate - especially considering industrial power supply practice. There is no mechanism to assure adequate user guidance.
- MDI fault tolerance requirements in more recent SPE PHYs address shorts to power supplies and ground.
- New non-PD MDIs could design to tolerate PoE voltages.
- New PSEs could design to rapidly protect against output shorts to ground.

QUESTIONS?