The Reality of Channels Operating at 100Gbps

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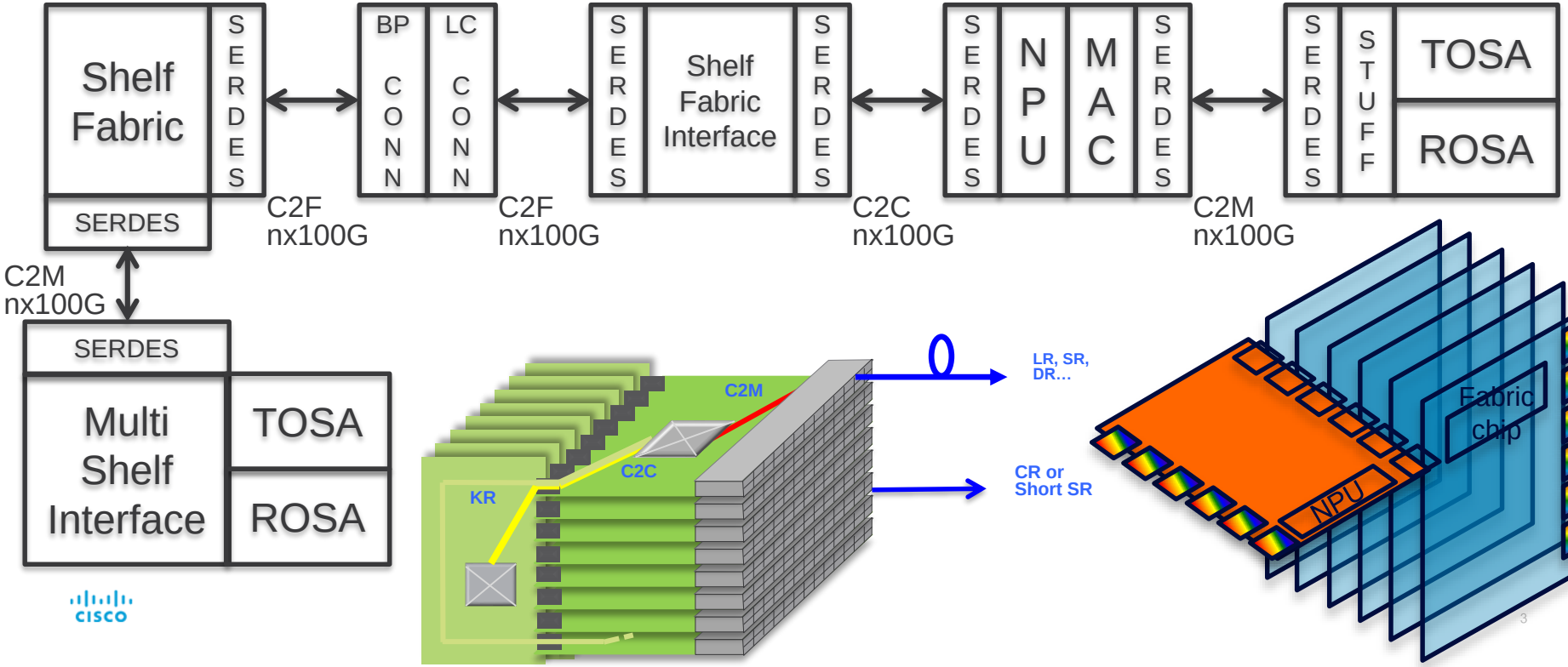
100Gbps Target Space

- C2M / C2C / C2F interfaces
- Single lane 100G optics
- 28G/56G/112G migration path for current platforms
- 56G/112G/224G migration path for next generation platforms

Point to Point Communications
Switch / Router SERDES Applications



112Gbps Fundamental BW and Harmonics

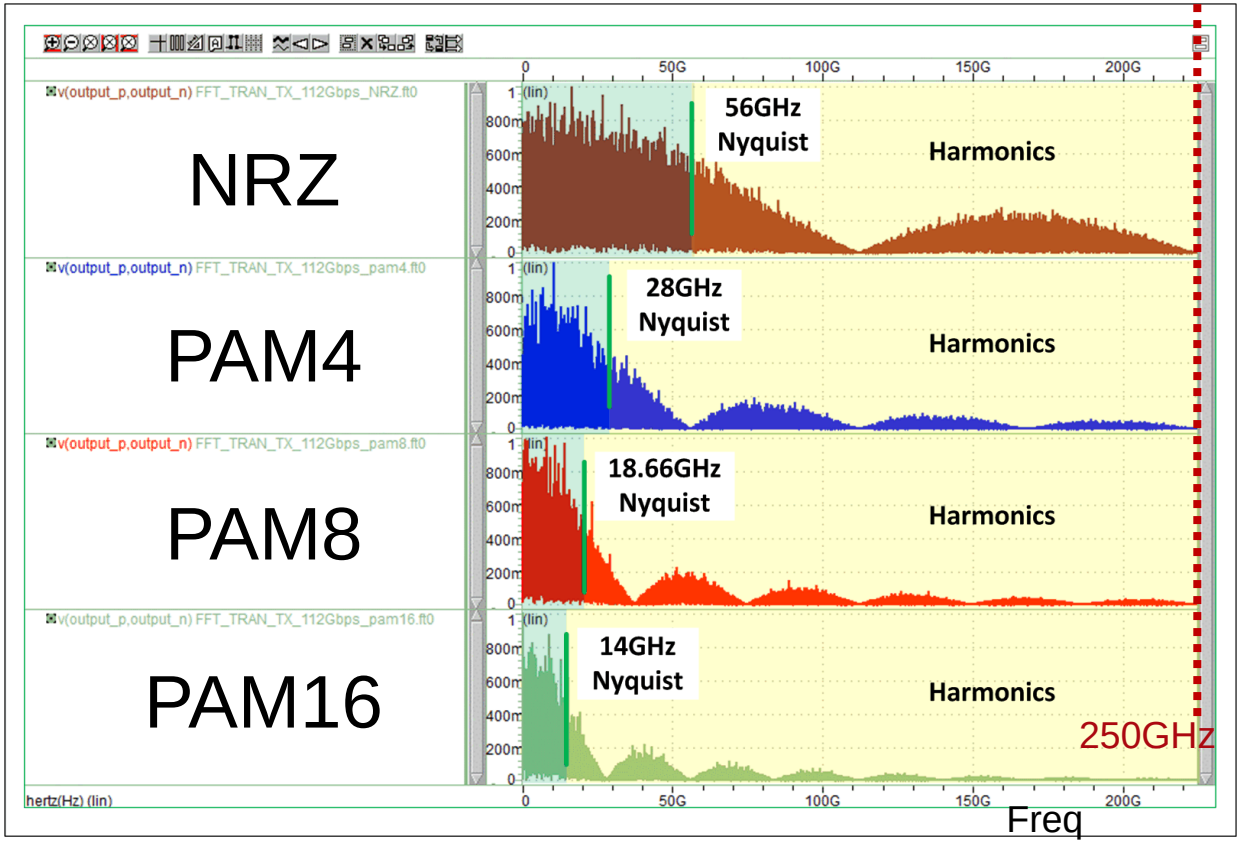
TX Signal FFT

Bandwidth of 4 Possible 112Gbps Choices

- Fundamental Bandwidth is at and below the Nyquist frequency

Fundamental BW in green

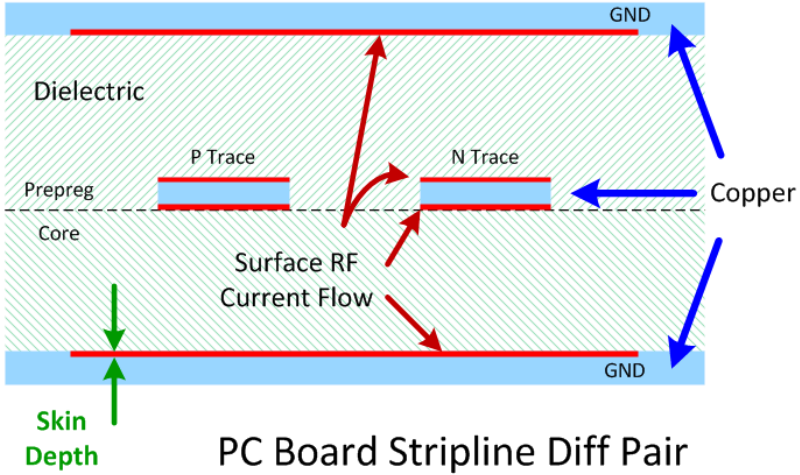
- Higher order modulation uses less overall bandwidth in the channel



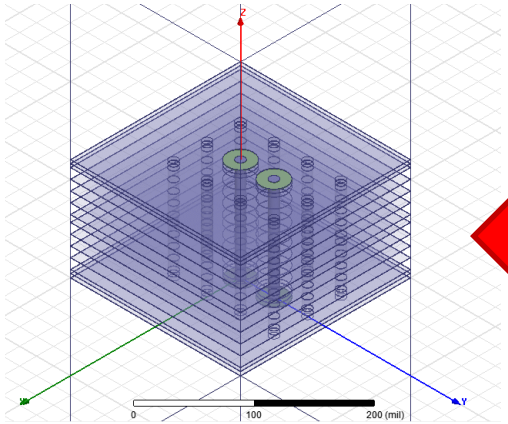
112G PAM4 Physics

- Assume 28GHz Nyquist
- At 28GHz the TEM wavelength, λ is 0.22” or 5.65mm with a Dk of 3.6
- At 28GHz, the skin depth in copper is 0.4µm, shown in red here
- The typical PC board stripline dimensions are under λ/10, so no modes for the traces and spaces

At 28GHz, the current is flowing in 2% to 3% surface of the copper



PC Board Stripline Diff Pair



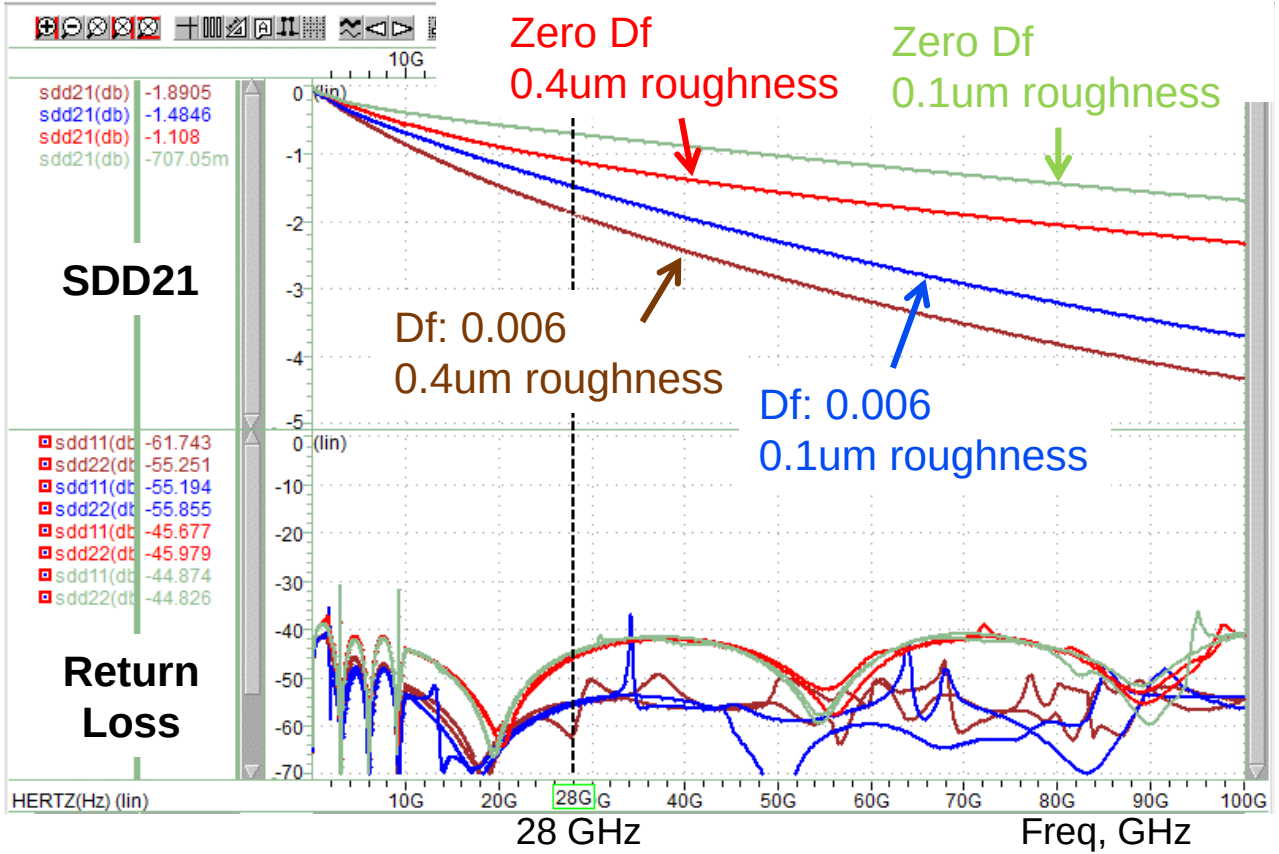
BGA patterns and connector footprints at 1mm or greater pitch are over λ/10 at 28GHz. This may pose a mode/resonance problem. Consider Hybrid designs.

Dielectric and Conductor Loss, 1” Trace

1” Diff Pair in HFSS
Single Stripline, Meg6
25C, no Vias, no Skew
½ oz copper, 4 mil traces

The Insertion Loss, SDD21 at 28GHz is:

SDD21	Df/ Cu Roughness
1.89dB	0.006/0.4um
1.485dB	0.006/0.1um
1.108dB	Zero/0.4um
0.707dB	Zero/0.1um

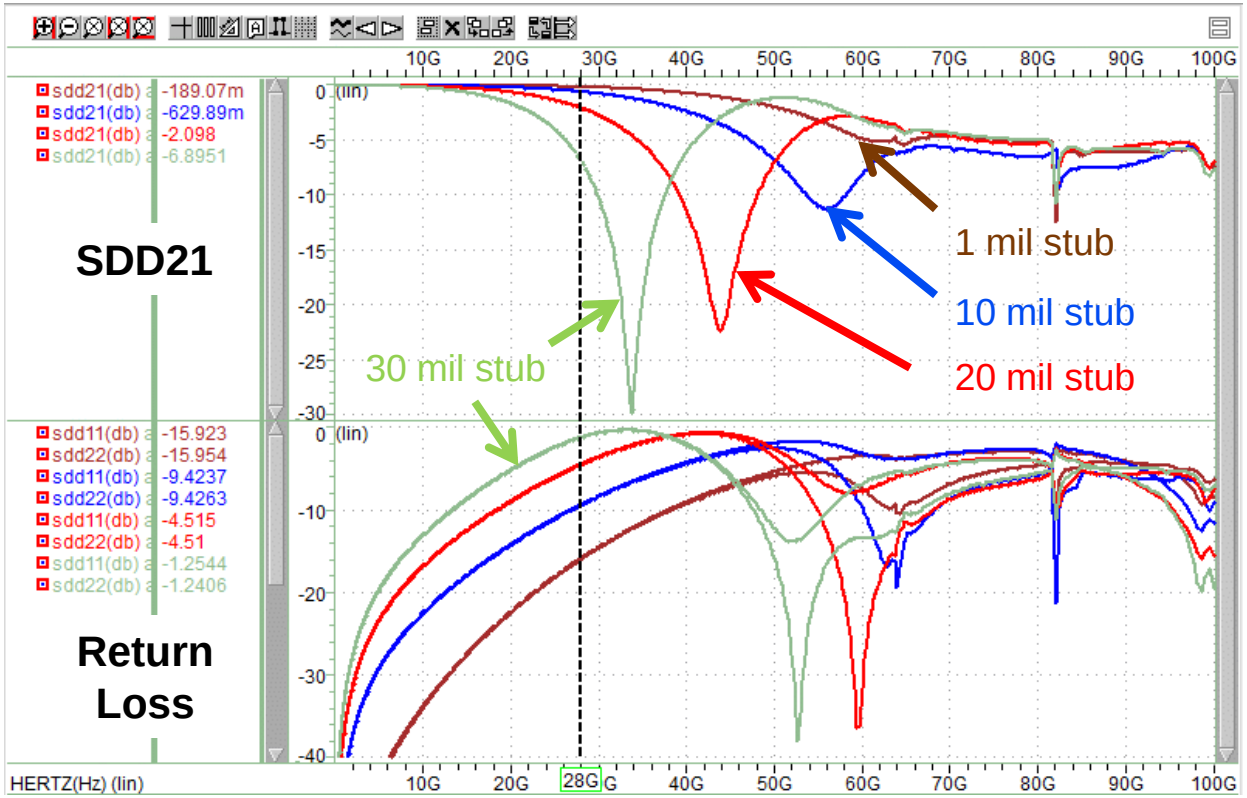


PC Board Via Stubs on Shallow Layers

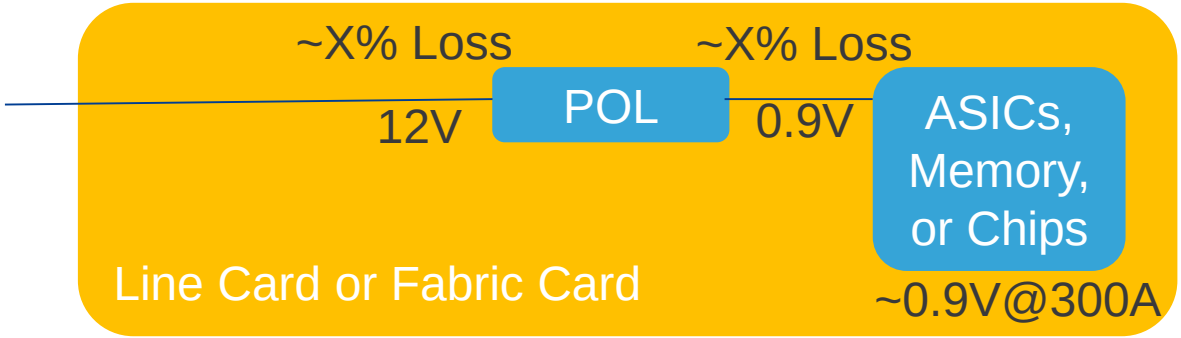
1mm Pitch BGA Via, Meg6
19 mil pads, 30 mil antipad
Shallow Via: layer 1 → 3
No P/N Skew

Insertion Loss at 28GHz is:

SDD21	Stub Length
0.19dB	1 mil
0.63dB	10 mil
2.1dB	20 mil
6.9dB	30 mil

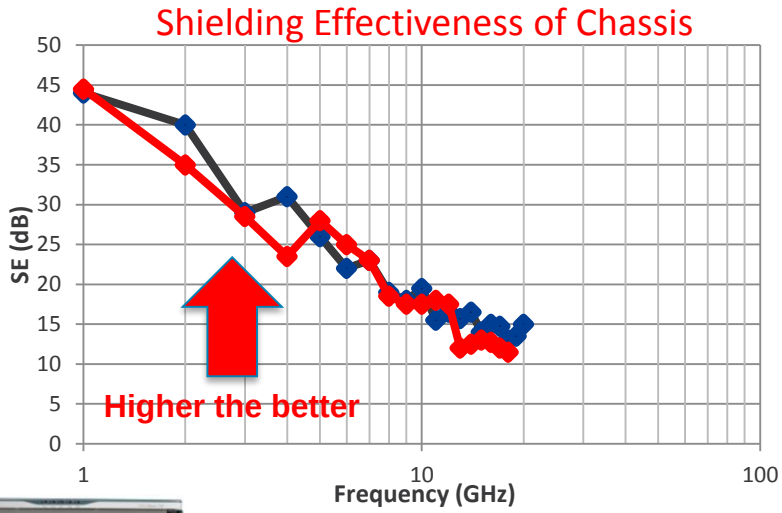


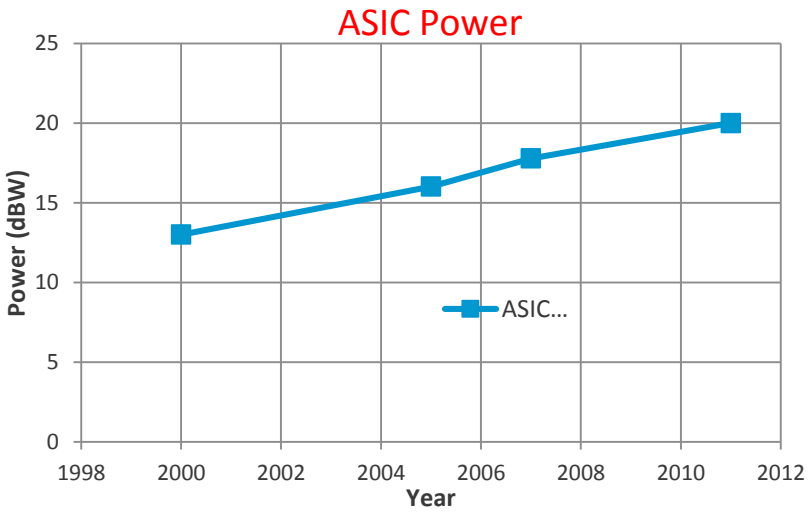
Other Hurdles to Address: Power / Ground Layers

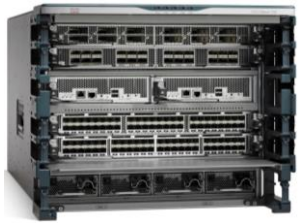


- ASIC dynamic + static operating current has dramatically increased over the last 5 years from 60A range to 300A range.
- This has caused a shift in both power layer thickness and power layer count. Ground layer performance has also been impacted in ASIC pin fields because of plane to VIA clearance issues.
- The change in power layers has seriously impacted SI performance at the higher frequencies because of limited ground-only coupling layers.

Other Hurdles to Address: Shielding Effectiveness







f (GHz)	SE (dB)
1	45
5	27 (18)
10	17 (28)
15	12 (33)
20	10 (35)

- **SE of chassis decreases with increase in data rates/frequency**
- **System power requirements are increasing on new products**

100Gbps Target Channel

- 30dB@28GHz target channel performance.
- 16in to 20in for orthogonal back plane designs. Longer for cable type back planes. Traditional back plane designs may not be feasible at this speed.
- Ground layers should handle minimum current densities of 400A. This will have serious impact on both SI performance and plane-plane coupling.
- Chassis shield effectiveness needs to be evaluated. Board edging and 20H rule should be considered.