Working Towards 100Gb/s Serial Electrical Channel Technical Feasibility

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Contribution Acknowledgements

- Scott McMorrow, Samtec
- Keith Guetig, Samtec

Agenda

- Channels, Form, and Fit
- History
- One approach to channels
- Results showing feasibility
- Early actions for moving forward
- Summary

Scope

- Only electrical technical possibilities
- No other CSD's (Criteria for Standards Development) discussed

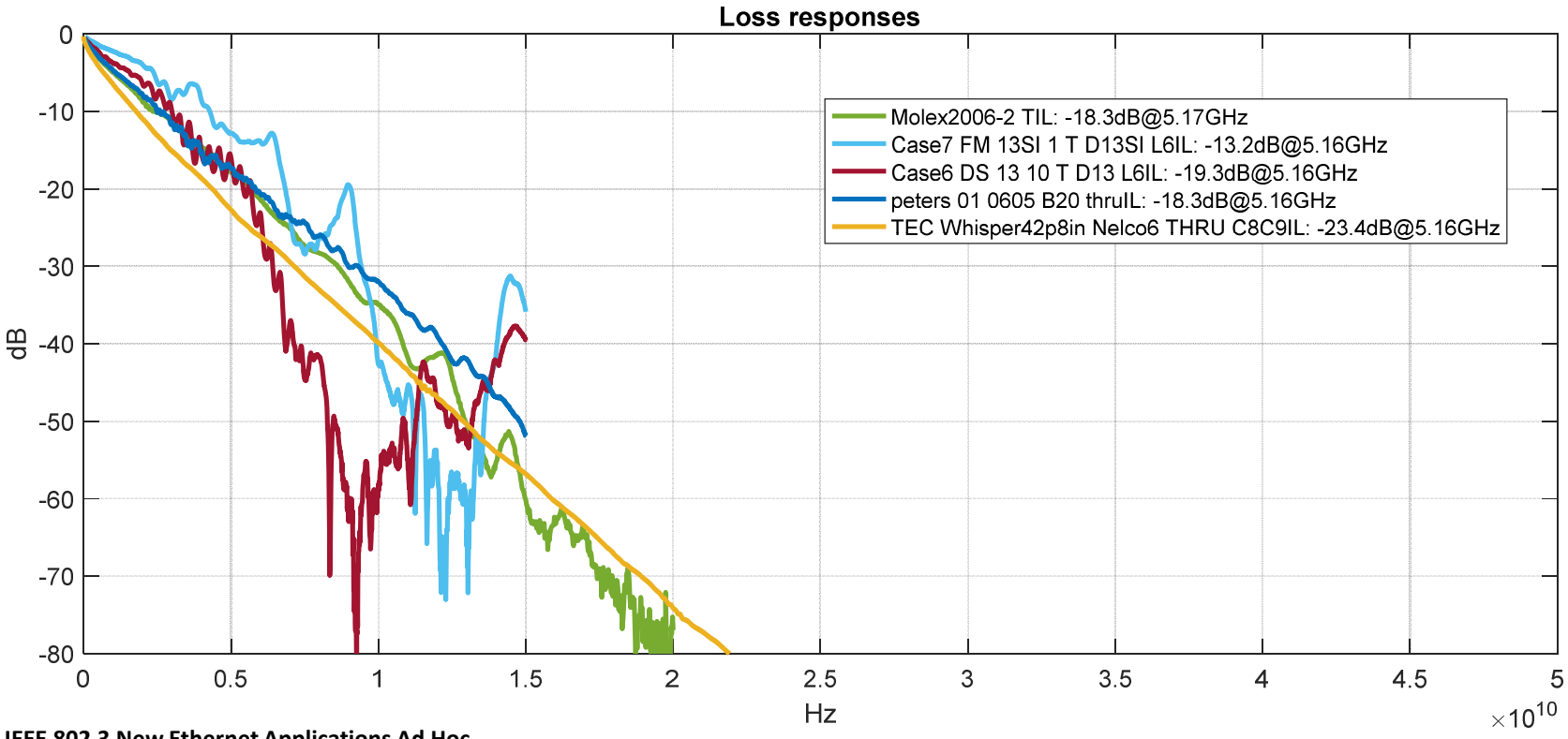
Electrical Landscape

- Backplane
  - 19 inch Rack
  - 2 connectors
    - Sometimes more
  - Device to device requirements in neighborhood of 1 meter
- Electrical Twin Axial Cable
  - 3 to 5 meters supported for latest 25G serial data rate
  - Longer for rates
- Chip to Chip
  - 1 connector
  - Around ½ meter reach
  - Similar to backplane
- Chip to Module
  - Compatible with both for twin axial cable and optics modules
  - Around 10 inch reach
  - Significantly less electrical capability

Decreasing Loss & Serdes Complexity

History: Backplane Represents the Baseline Channel Budget

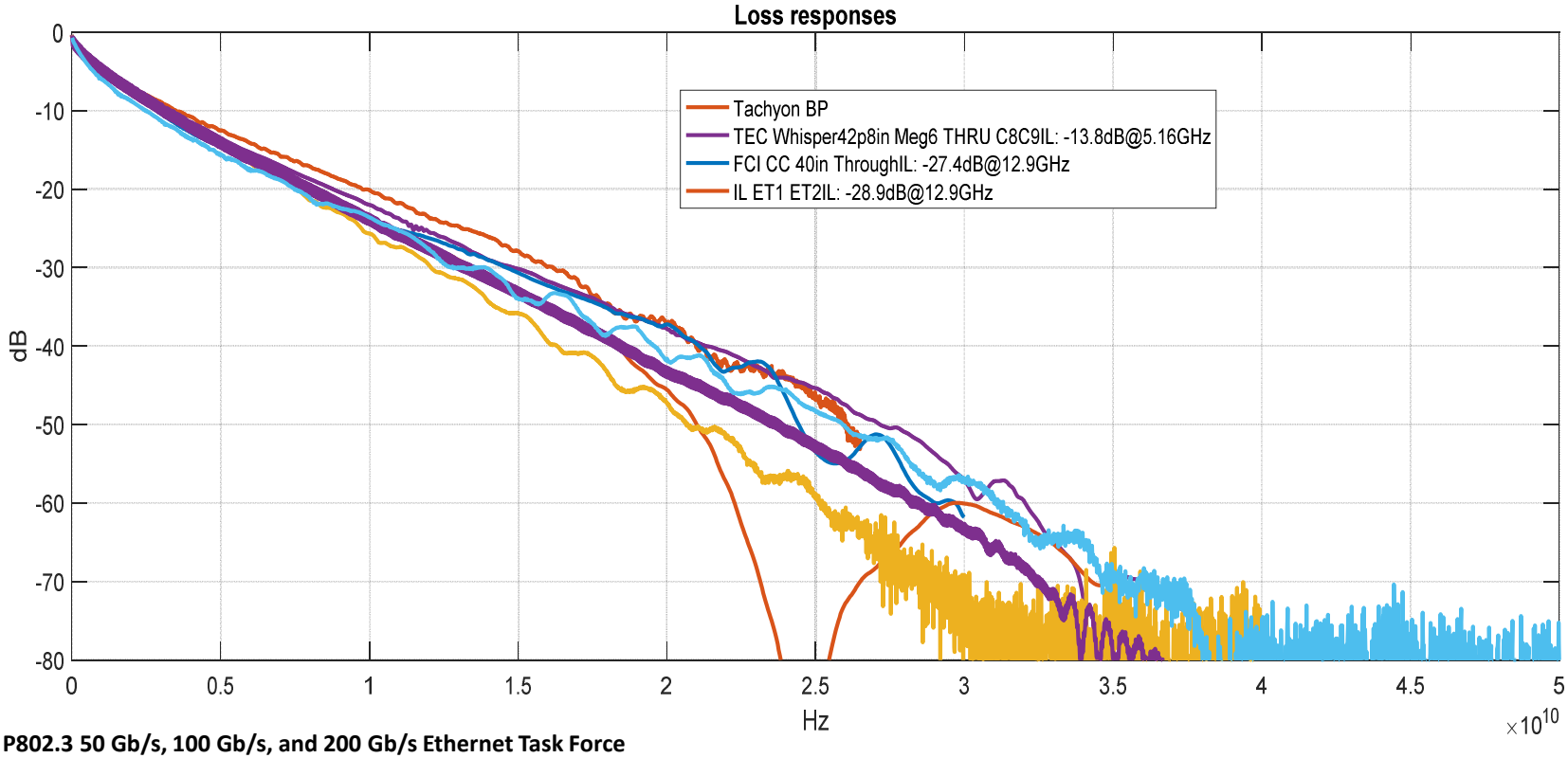
10 Gb/s serial Example: (10G Base KR) – 1 meter reach, ~23 dB



25 Gb/s: More Loss But at a Higher Frequency

Example of 25 Gb/s backplanes

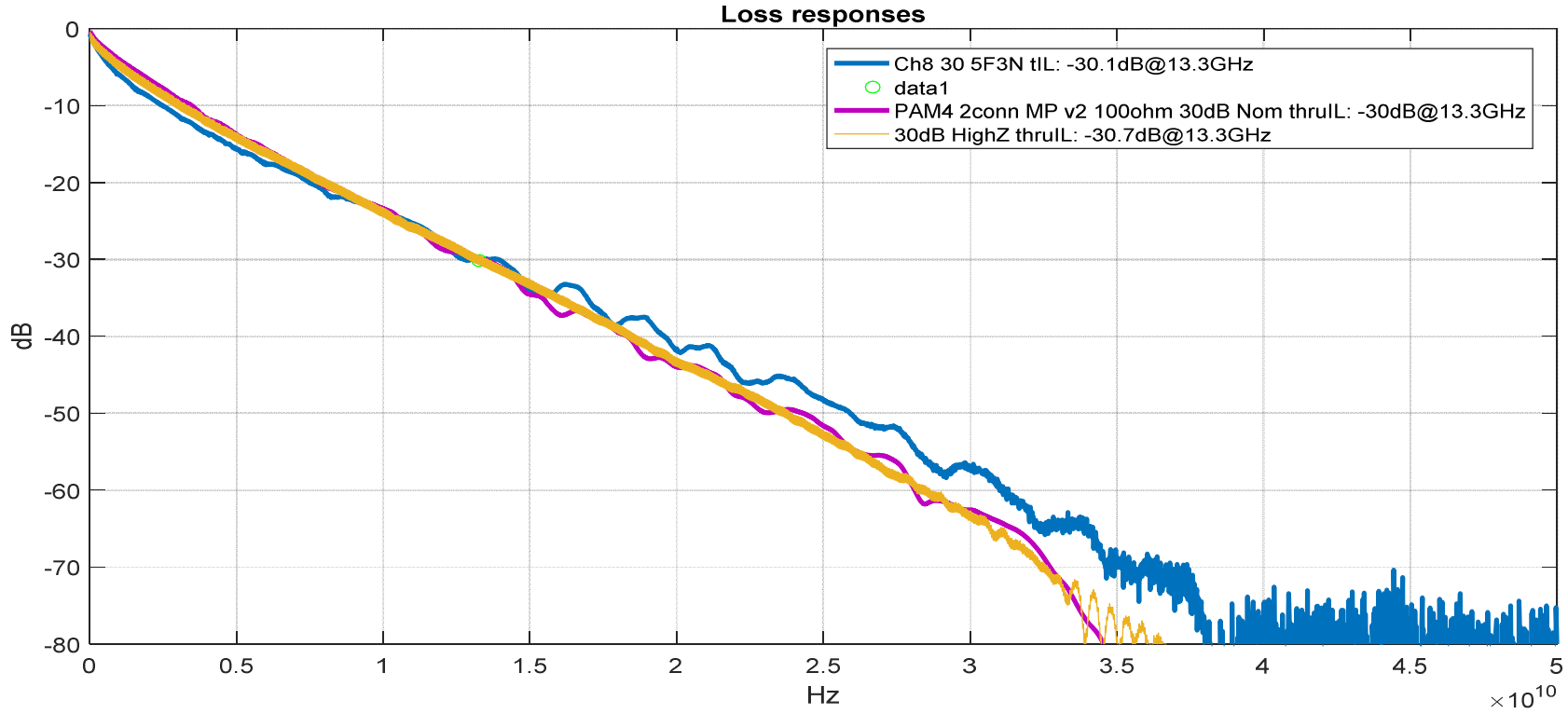
- Crosstalk not shown here



50 Gb/s PAM4 Serial: “Cleaner” Channels Needed

Examples of 50 Gb/s PAM4 Backplanes

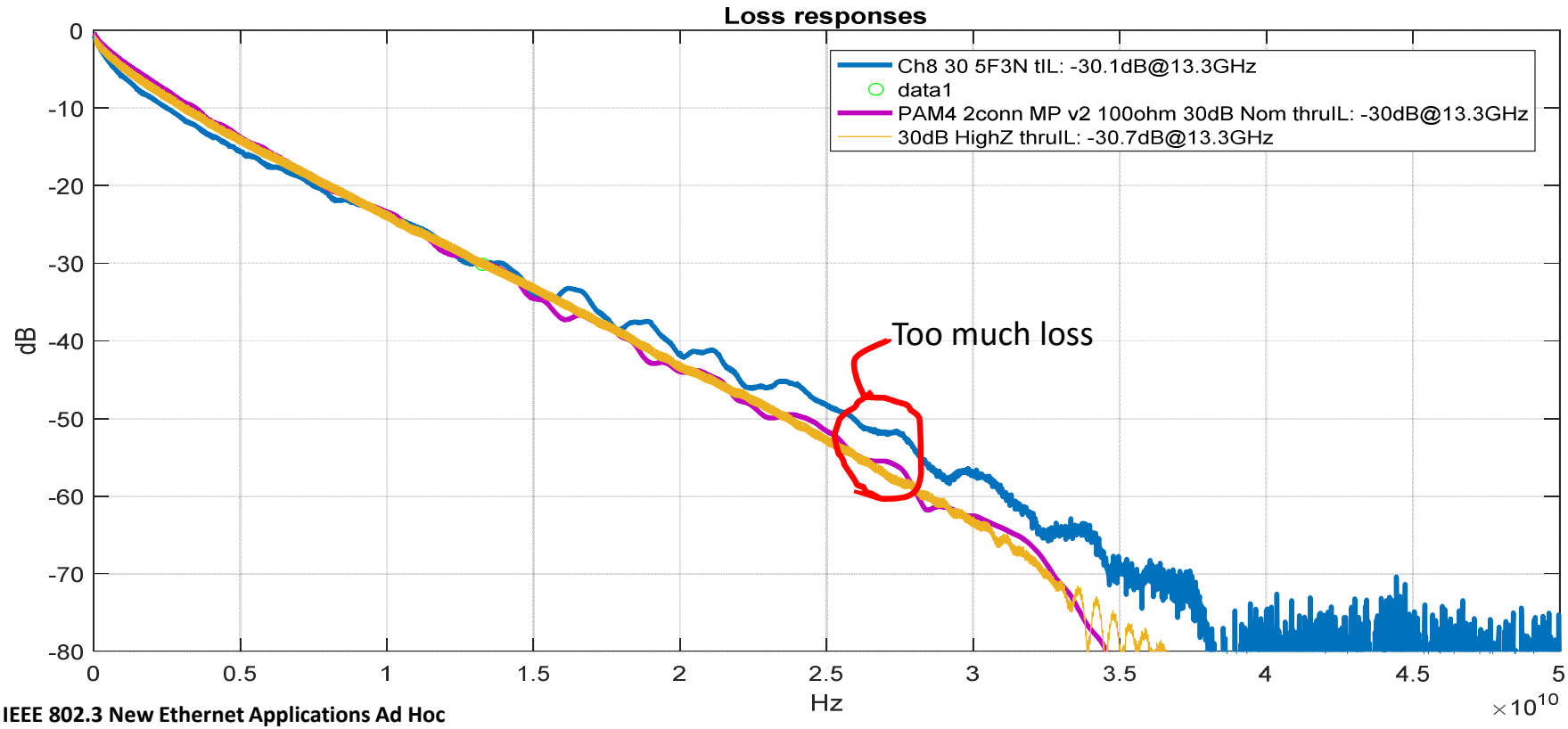
- Crosstalk not shown here



100 Gb/s PAM4 Signaling Rate ~ 26 GHz

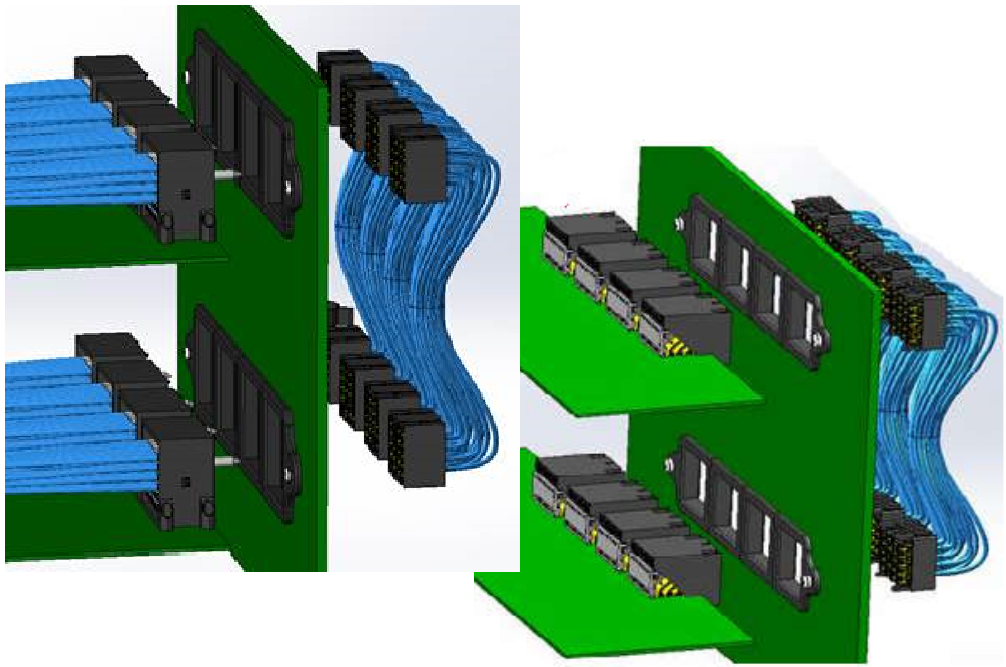
50 Gb/s PAM4 designs have too much loss!

- Crosstalk not shown here



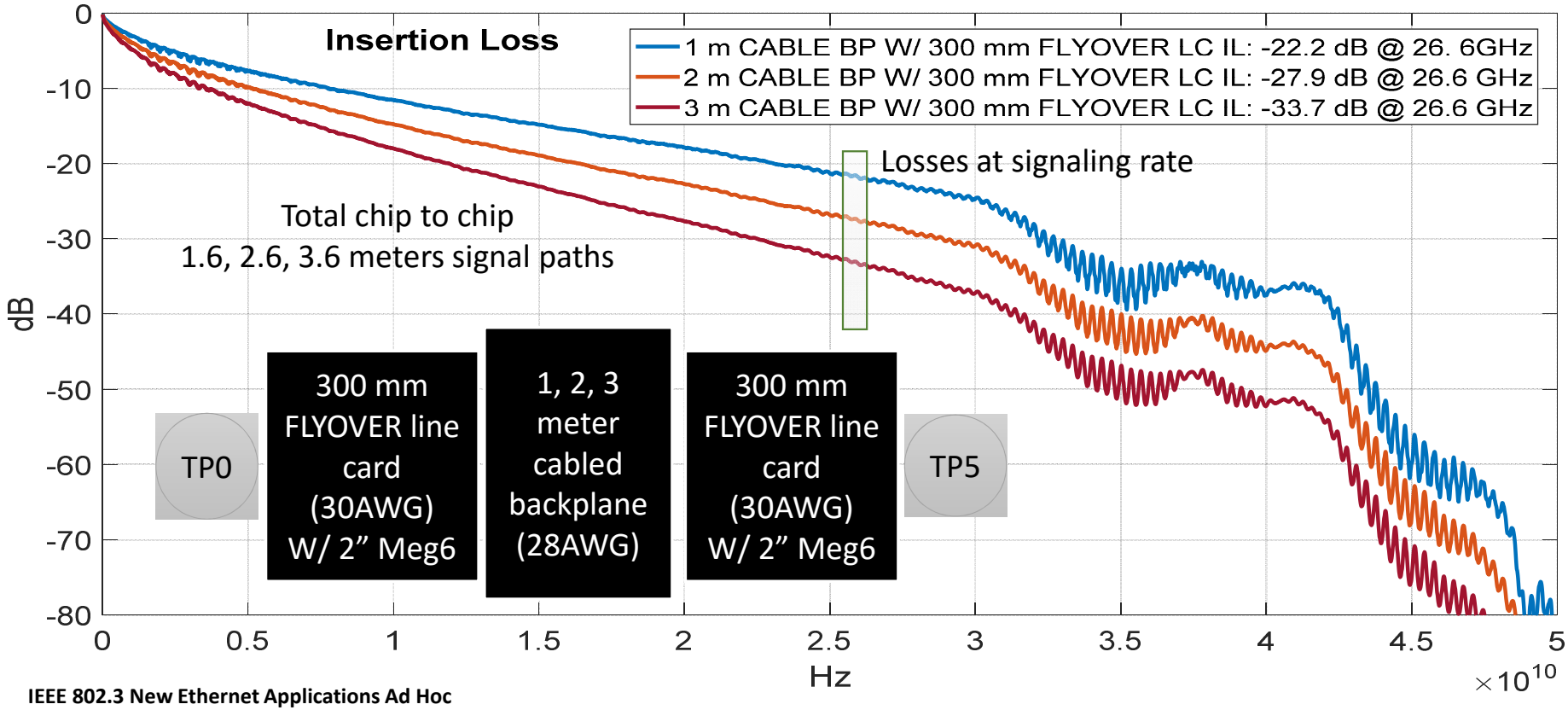
What Fits into the 19” Rack Backplane Paradigm? and Has Acceptable Losses

- Cabled backplanes can achieve between 20 dB and 30 dB loss at 26 GHz
  - chip to chip
  - AKA BGA to BGA
- Maybe a basis for a channel budget
- Other designs could fit the bill too
  - Such as orthogonal backplanes

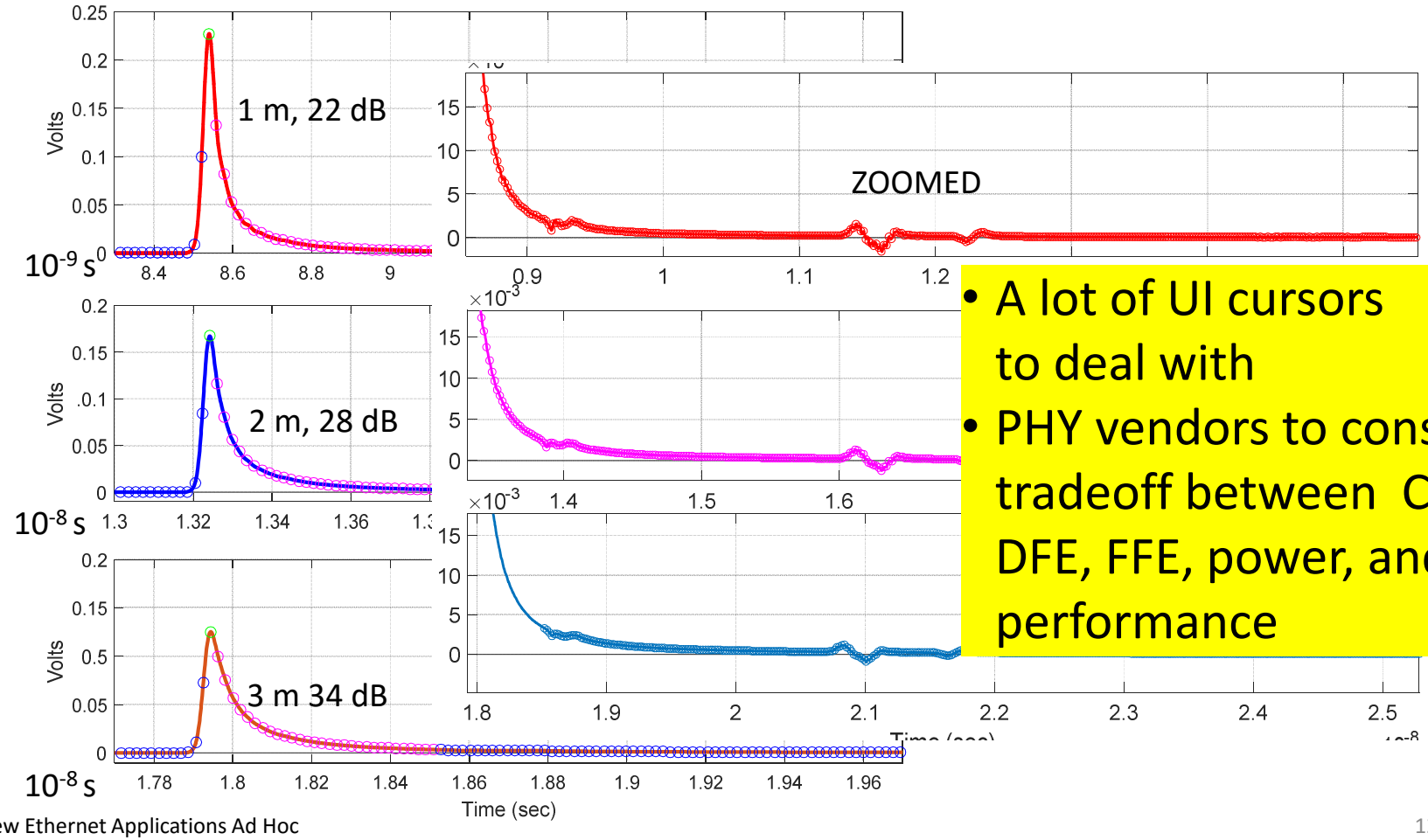


Between 20 dB and 30 dB loss is achievable in a cable backplane design

- This loss seems reasonable. This is not the whole story



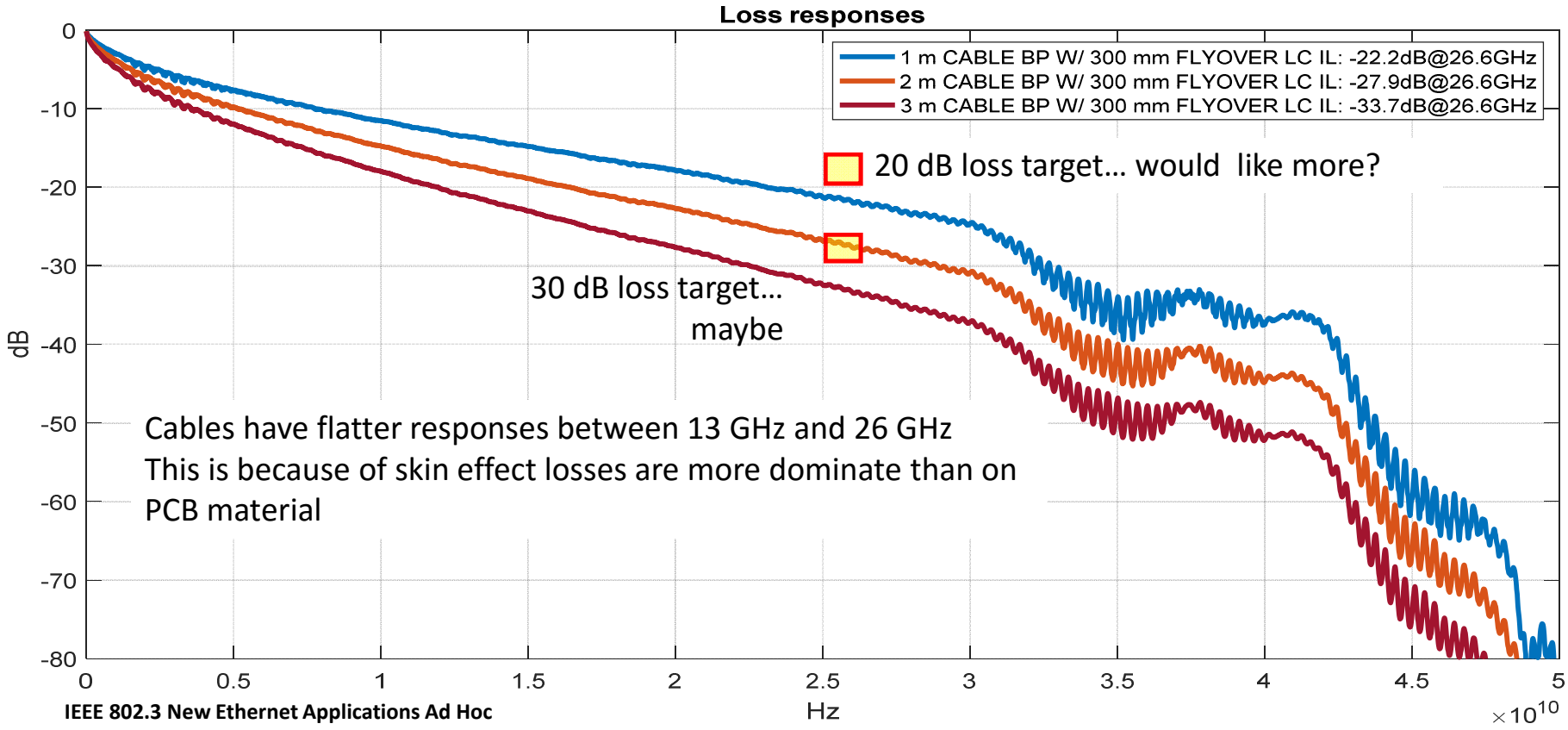
Pulse response: 3 UI cursors on rising edge



- A lot of UI cursors to deal with
- PHY vendors to consider tradeoff between CTF, DFE, FFE, power, and performance

Between 20 dB and 30 dB Loss Is Achievable for a Cabled Backplane Design

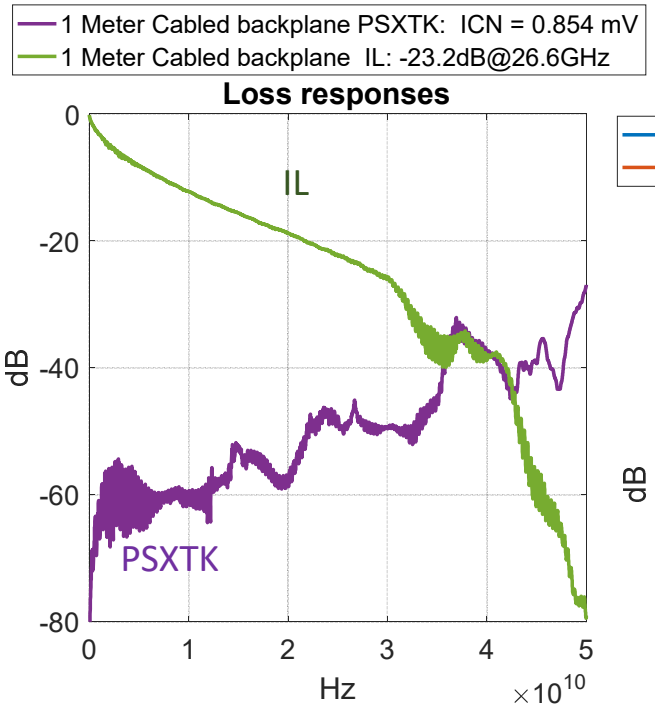
This loss seems reasonable. This is not the whole story

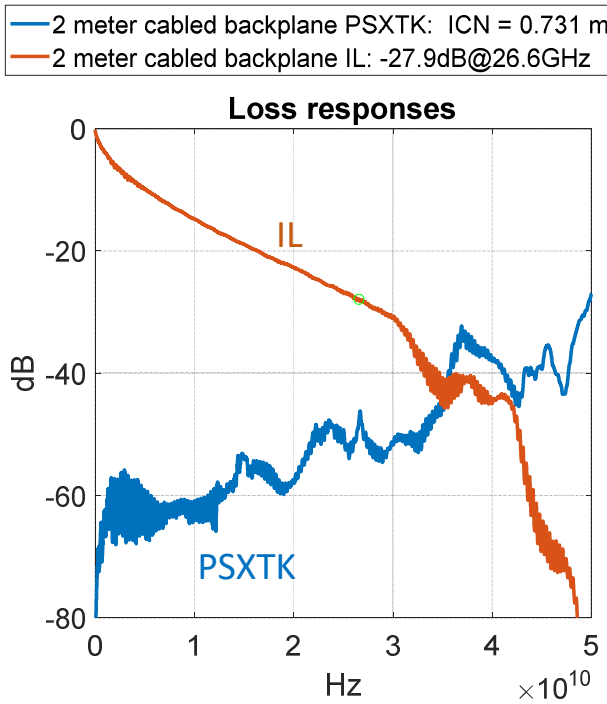


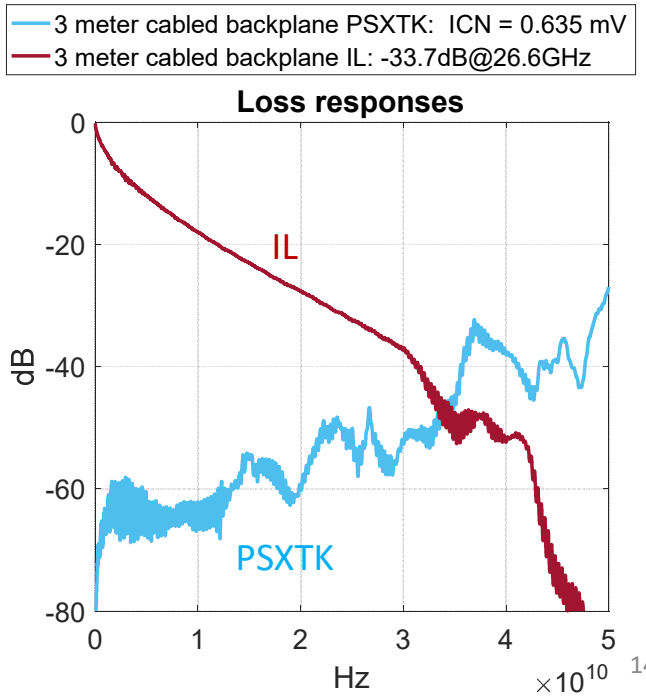
Keeping Crosstalk Below 0.7 mV ICN will be a Challenge, but Feasible

Physical isolation between ports and Tx/Rx helps

ICN may not be “the” metric. But, a relative goal?







Modified COM shows better than 3 dB for the 1 meter cabled backplane

The COM package assumptions = 14 dB loss at the signaling frequency!

3rd precursor

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.0e-4 1.0e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.25:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.15]		[min:step:max]
c(-3)	[-0.15:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
g_DC	[-20:1:-6]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
A_v	0.45	V	tdr selected
A_fe	0.45	V	tdr selected
A_ne	0.63	V	tdr selected
L	4		
M	32		
N_b	30	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	1.64E-08	V^2/GHz	
SNR_TX	34	dB	tdr selected
R_LM	0.95		
DER_0	1.00E-04		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
Display frequency domain	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\D1p2_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	V175_m9_dfe38_	
T_r	0.007	ns
FORCE_TR	1	logical

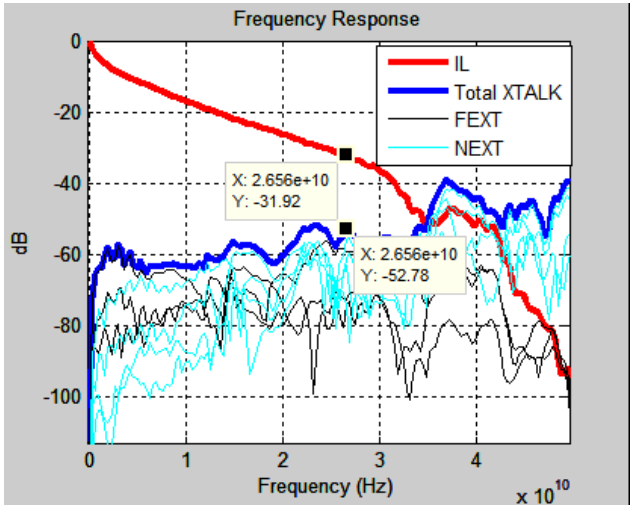
Table 93A–3 parameters		
Parameter	**Setting**	
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	
package_Z_c	90	

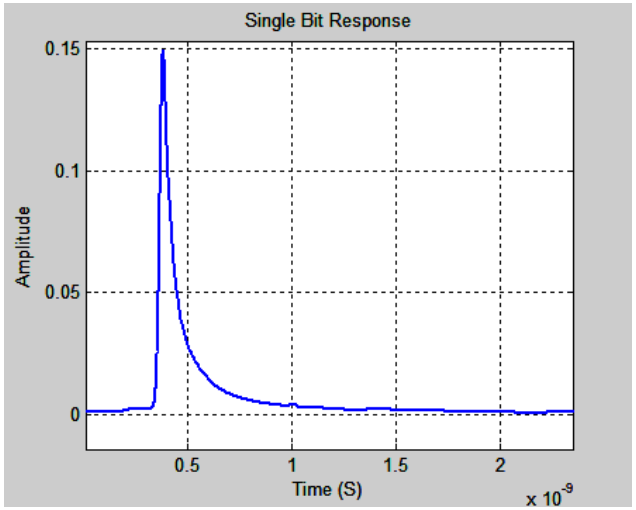
Operational control		
COM Pass threshold	3	dB
Include PCB	0	Value
g_DC_HP	[-9:1:-1]	
f_HP_PZ	1.328E+00	GHz

This table is only for feasibility. A lot more work will be required.

PHY Simulation Example Setup for Consideration

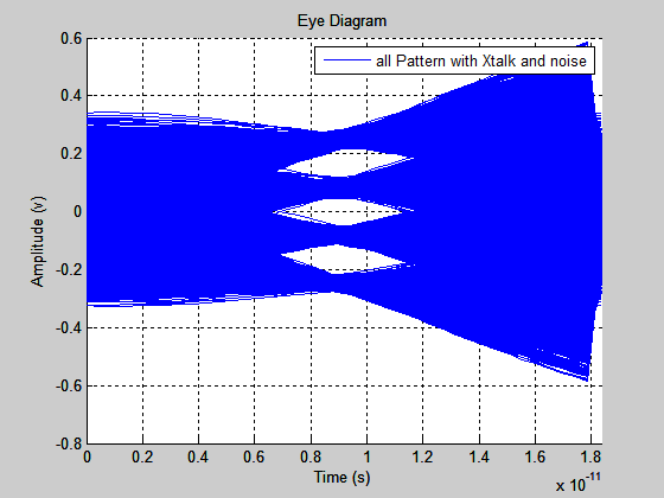
- Insertion loss for 2 m cable backplane is -31. 92 dB @ 26.6 GHz, ICR is 20.86 dB @ 26.6 GHz.
- A low loss package model included
- TX SNDR: 34 dB
- Jitter: RJ 0.01 UI rms, even/odd: 0.02 UI p2p.
- Device noise and distortion are modeled.





PHY Simulation Shows Promising Results

- ❑ BER is about 6.2E-8.
- ❑ TX FIR: 3 pre cursors, 25 post cursors, tail taps are very small.
- ❑ RX: CTLE + DFE.



Of course follow-on work will happen.

Preliminary Work Before Study Group and Task Force Gets into High Gear

- Package – tough decisions
  - 25-35 % of a channel insertion loss budget for 100 G PAM-4 based is not really acceptable
  - Consider manufacturing variations
    - http://www.ieee802.org/3/cd/public/adhoc/archive/hidaka_020117_3cd_adhoc.pdf
  - Consider PHY types for package S –M –L ?
- Equalization – Needs to consider more
  - Pre-cursors
  - Post-cursors
  - Continuous Time
  - Other approaches for reference equalizers
- COM
  - Reference equalization may tax the quick run time of a COM computation
  - New methods may need to be considered
- Noise sources
  - Signal isolation
    - Tx to Rx and port separation needs to support 0.7mV or less noise
  - Bounded vs Gaussian noise assumptions
- Lower impedance targets
  - A lot of prior work suggest margin improvements are possible

Summary

- A 100 Gb/s backplane channel shown
- Rudimentary computations and simulation suggest operation is in sight
- A list of early actions suggest efficiency improvements for project
  - Perhaps before the CFI?
  - Use NEA to facilitate?