

# Interconnect for 100G serial I/O ports



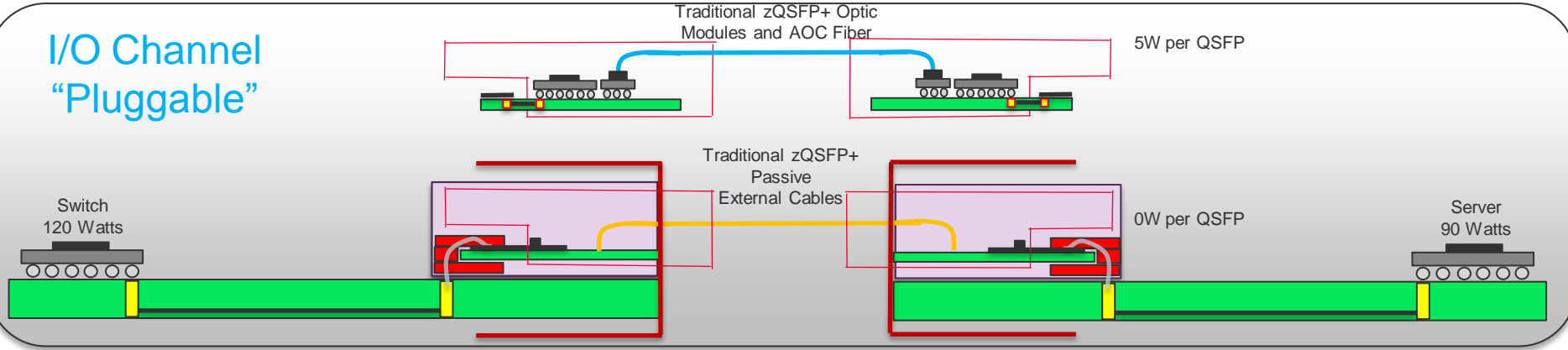
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# Today @ 25Gbps lanes

I/O Channel  
“Pluggable”



# PAM4 Channel Link Budget (ball to ball)

## Traditional 56 Gbps, $f_0=14$ GHz

Parameter	Loss
External cable loss (5m) (26 AWG)	16 dB
2 Host PCB trace (9" Megtron 6)	2 x 7.3 dB
2 Connectors	2 x 1.2 dB
2 Module PCB & capacitor & termination	2 x 1.5 dB
<b>Total channel loss</b>	<b>36 dB</b>

## Traditional 112 Gbps, $f_0=28$ GHz

Parameter	Loss
External cable loss (2m) (26 AWG foam)	13 dB
2 Host PCB trace (9" Isola Tachyon)	2 x 13.5 dB
2 Connectors	2 x 1.4 dB
2 Module PCB & capacitor	2 x 2 dB
<b>Total channel loss</b>	<b>46.8 dB</b>

- Current 25G-generation CDR/DFE/DSPs provide -36 dB loss compensation @ 14 GHz
- The traditional PCB channel is broken at 28 GHz

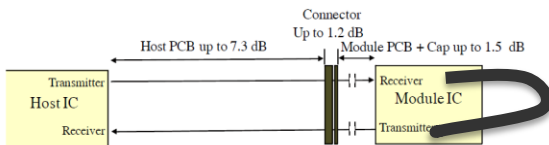
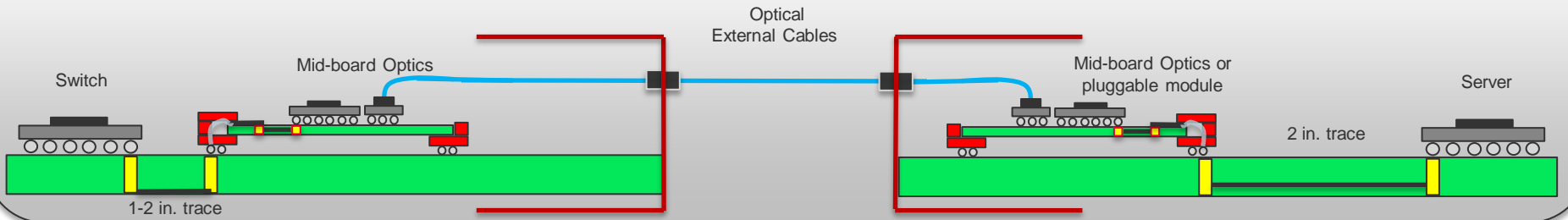


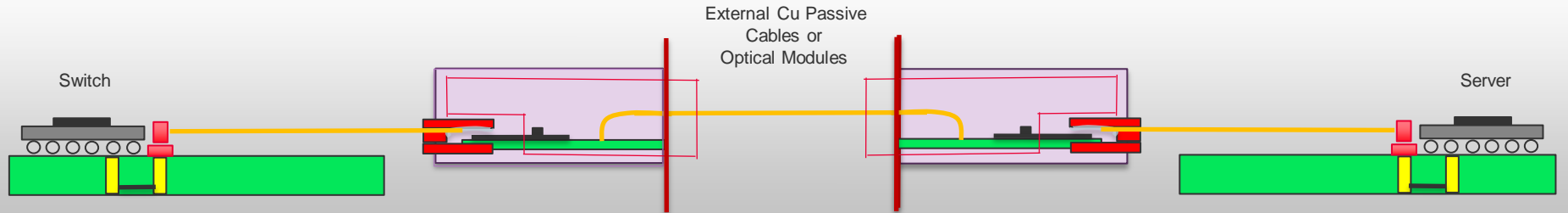
Figure 13-20. CEI-28G-VSR full Channel Reference Model

# Options for 100 Gbps lanes

## “Mid-board Optics”



## Pluggable optics and passive copper cables



# QSFP BiPass to NearStack “VSR” Cable



Shown here is the 56G PAM4 design

## Key Benefits:

- › **Lower System-Level Costs:**
  - › Eliminate the need for costly PCB materials (Nelco, Megtron, Tachyon, etc)
  - › Eliminate the use of additional DFE or retimer chips to drive long traces
  - › Improved thermal performance with 1x1 cages (air-cooled)
- › **Architectural Flexibility:**
  - › Freedom to locate ASIC anywhere (eg. further from backplane)
  - › Enable lower power ASIC
  - › Extended reach from ASIC to I/O
  - › Enable longer external copper I/O cables
  - › Cool the ports and the ASIC better
- › **New ways to handle power integrity to large ASICs**

# PAM4 Channel Link Budget

## Traditional PCB (112 Gbps, $f_0=28$ GHz)

Parameter	Loss
External cable loss (2m) (26 AWG foam)	13 dB
2 Host PCB trace (9" Isola Isola Tachyon)	2 x 13.5 dB
2 Connectors (port)	2 x 1.4 dB
2 Module PCB & capacitor & termination	2 x 2 dB
<b>Total channel loss</b>	<b>46.8 dB</b>

## 112G BiPass Cables 112 Gbps, $f_0=28$ GHz

Parameter	Loss
External cable loss (2m) (26 AWG foam)	13 dB
2 BiPass cables (10")(30 AWG) incl both connectors	2 x 3.1 dB
2 Module PCB & capacitor & termination	2 x 2 dB
2 Host PCB trace (ASIC side) (2" Isola Tachyon)	1.5 x 3 dB
<b>Total channel loss</b>	<b>27.7 dB</b>

- BiPass to NearStack assemblies are close to the -25 dB loss goal
- But will they help us deal with noise?
- And will they help us with cooling?

# PAM4 “VSR” Budget

## Traditional PCB (112 Gbps, $f_0=28$ GHz)

Parameter	Loss
Package	3 dB ???
ASIC via	0.5 dB
Host PCB trace (9" Isola Tachyon)	13.5 dB
Connector	1.4 dB
<b>Total channel loss</b>	<b>~15.4 to 18.4 dB</b>

## 112G BiPass Cables 112 Gbps, $f_0=28$ GHz

Parameter	Loss
Package	3 dB ???
ASIC via	0.5 dB
Host PCB trace (ASIC side) (2" Isola Tachyon)	6 dB
BiPass cables (10")(30 AWG) incl both connectors	3.1 dB
<b>Total channel loss</b>	<b>~9.6 to 12.6 dB</b>

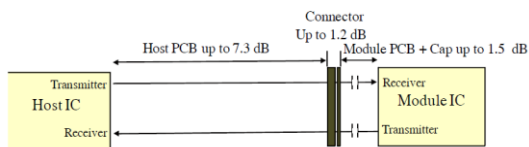


Figure 13-20. CEI-28G-VSR full Channel Reference Model

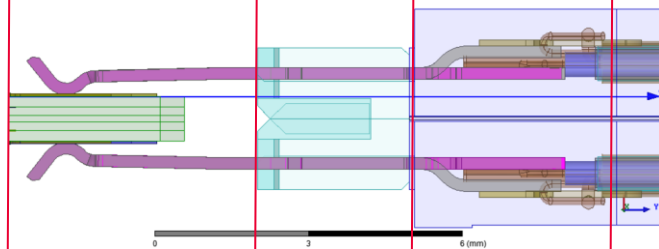
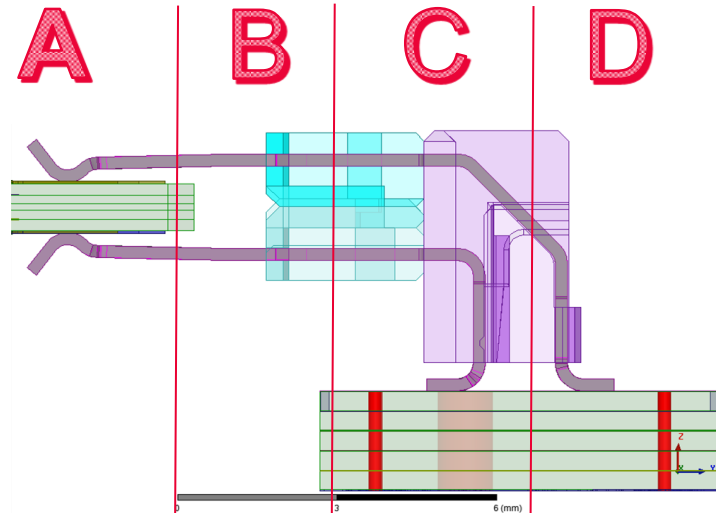
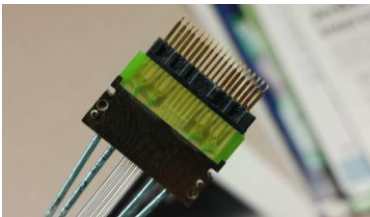
# BiPass compared to a standard SMT Connector

- A. The goal for the module/connector interface is to be backward compatible.
- B. Substantially the same
- C. The Twinax approach provides shorter electrical path lengths and more consistent signal integrity for upper/lower rows (and for upper/lower stacked connectors)
- D. The standard connector uses vias and PCB trace. The BiPass™ approach uses Twinax.

Standard SMT zQSFP

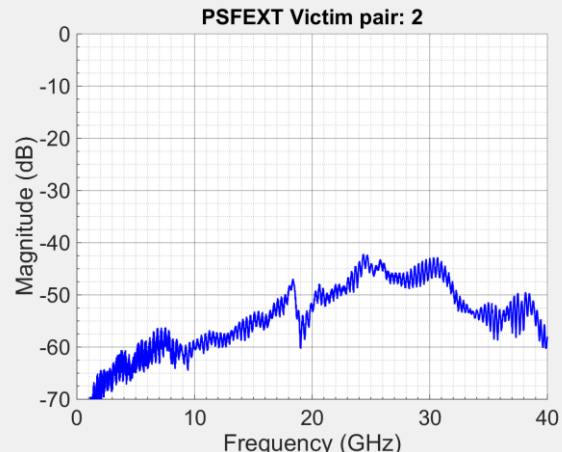
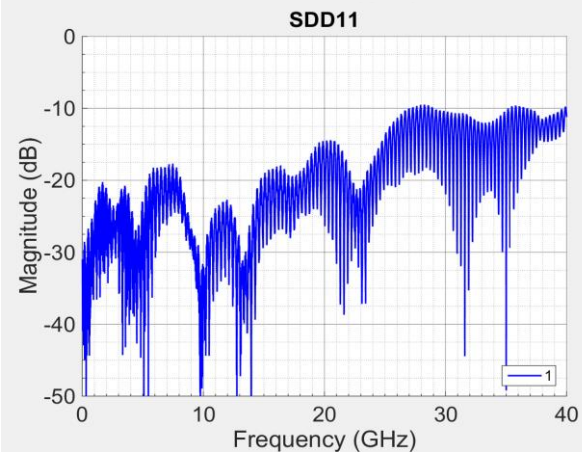
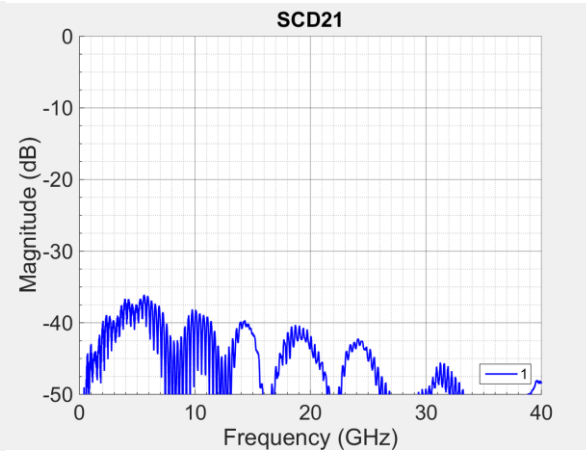
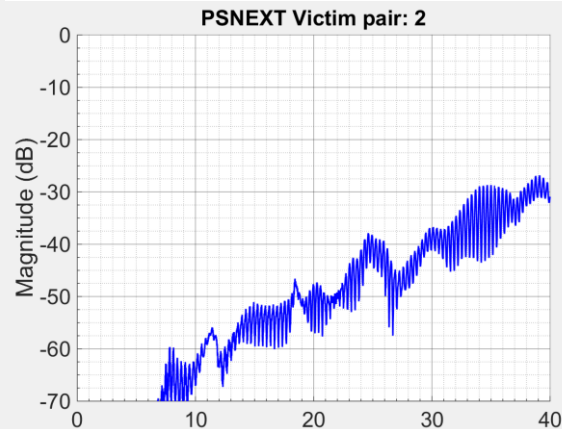


zQSFP Twinax BiPass





# QSFP112 BiPass Ball-to-ball Channel



- 2, 12" QSFP BiPass to NearStack 30 AWG cable
- 2m 26 AWG QSFP112 cables - backward compatible with QSFP
- 2" Isola Tachyon trace between Near Stack and ASIC

# Example I/O ports using Backplane Cables



- Open19 Architecture
- Improves SI versus traditional pluggable ports
  - Much lower loss
  - Much lower crosstalk
- Significantly higher port density
  - 2 x 96 diff pair ports inv1RU shown here
  - ~72 QSFP-DD ports (fully loaded)

# PAM4 Channel Link Budget

## 112G BiPass to front panel Cables 112 Gbps, $f_0=28$ GHz

Parameter	Loss
External cable loss (2m) (26 AWG foam)	13 dB
2 BiPass cables (10")(30 AWG) incl both connectors	2 x 3.1 dB
2 Module PCB & capacitor & termination	2 x 2 dB
2 Host PCB trace (ASIC side) (2" Isola Tachyon)	1.5 x 3 dB
<b>Total channel loss</b>	<b>27.7 dB</b>

## 112G BiPass to Backplane Cables 112 Gbps, $f_0=28$ GHz

Parameter	Loss
External cable loss (2m) (26 AWG foam)	13 dB
2 BiPass cables (10")(30 AWG) incl both connectors	2 x 4.6 dB
2 Module PCB & capacitor & termination	0
2 Host PCB trace (ASIC side) (2" Isola Tachyon)	1.5 x 3 dB
<b>Total channel loss</b>	<b>26.7 dB</b>



Thankyou

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