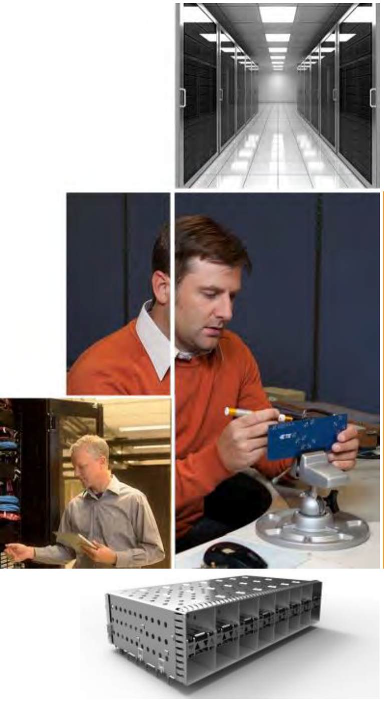

An Initial Investigation of a Serial “100”Gbps PAM4 VSR Electrical Channel

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TE Connectivity
May 24, 2017

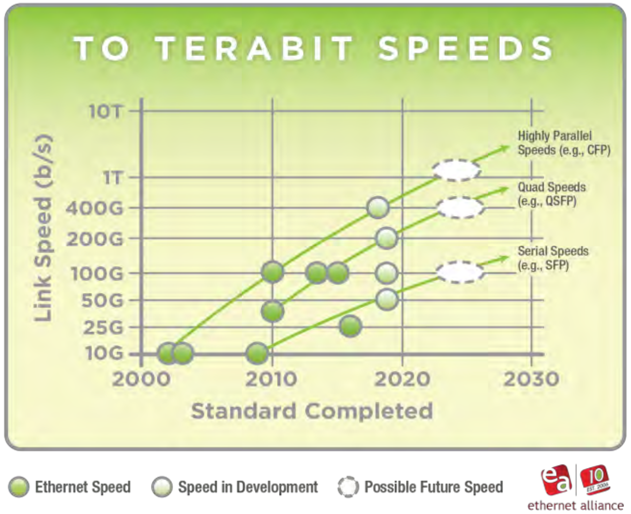
Agenda

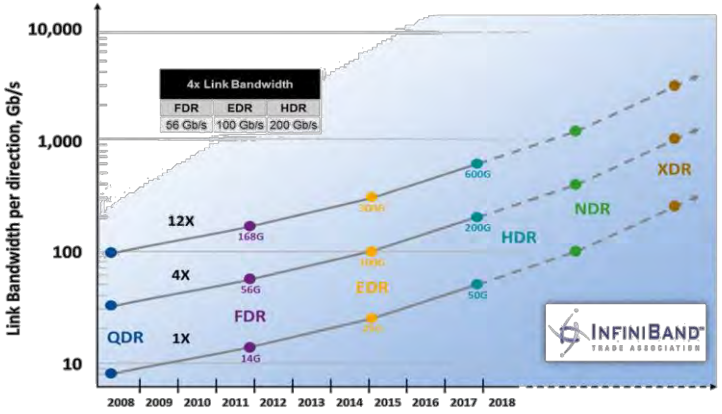
- Transmission over copper
- Channel description
- Existing 25G channel review
- Setting 100G targets
- 100G VSR channels
- Conclusions

Higher speed copper transmission

What are the limits of copper?

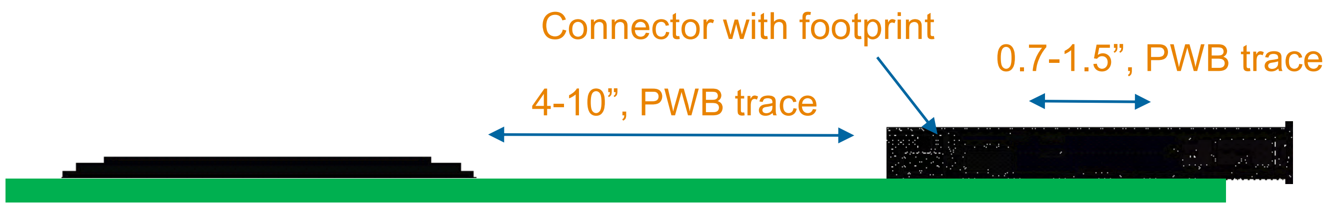
- Higher speed copper was predicted to be dead a decade ago– but this has also been the case for the last 30 years
- Copper keeps on pushing the frequency limits
- Copper vs optical – gap is closing as speeds increase
- Although optics offer reach and density, electrical still offers lower cost and power
- Equalization technology and modulation techniques continue to be improved
  - PAM4, ENRZ, Duobinary, etc.
- The economics at stake are huge, “Do you really want to bet against copper?”



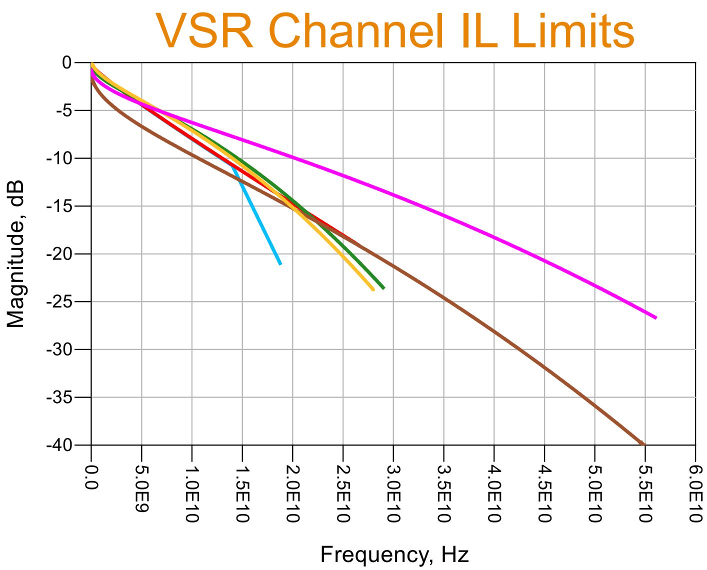


Channels Considered for this Discussion

VSR - Connecting Chips to Modules - Typical Reach up to 10”



Reminder of 25 & 50G Channel Requirements

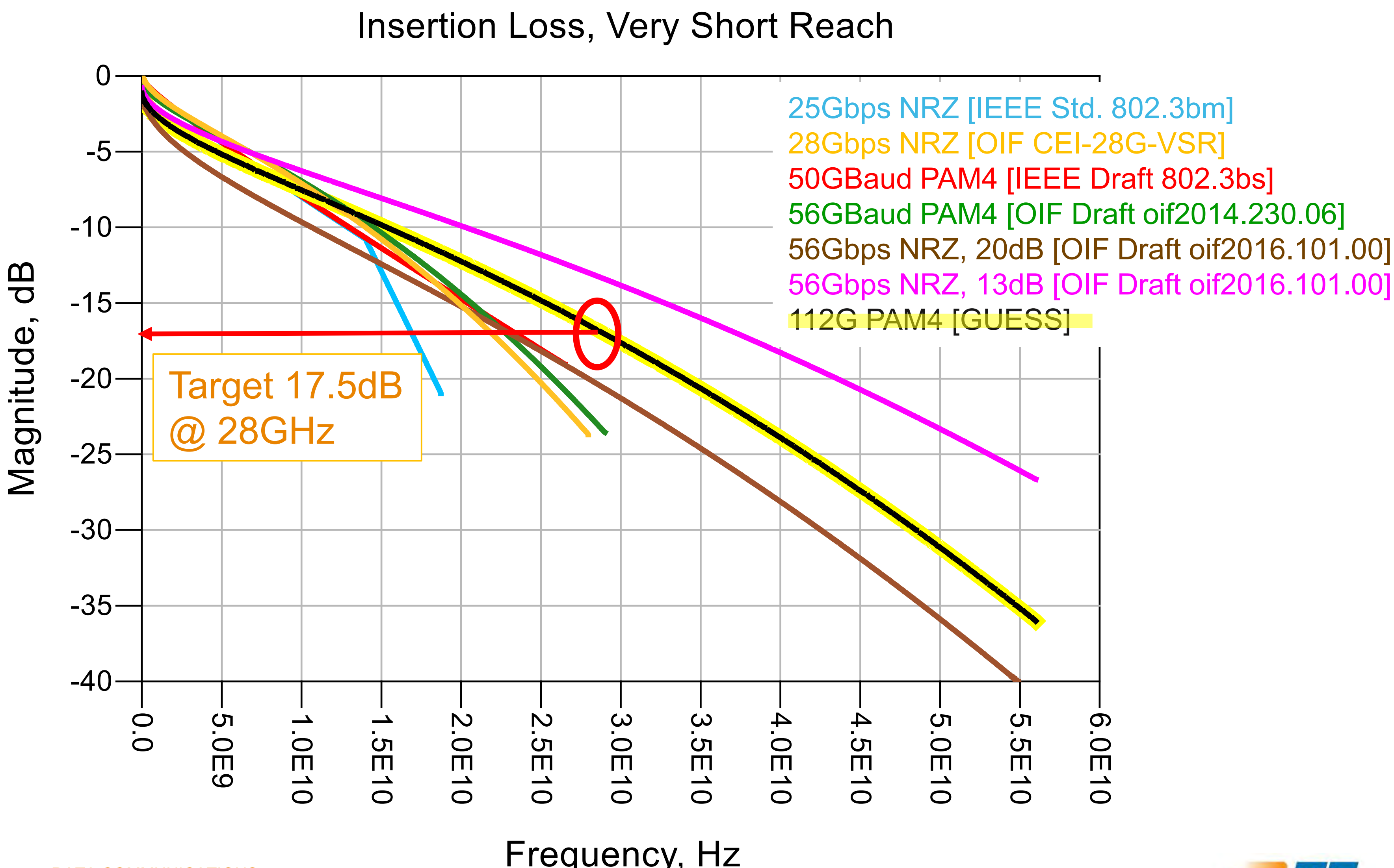


25Gbps NRZ [IEEE Std. 802.3bm]
28Gbps NRZ [OIF CEI-28G-VSR]
50GBaud PAM4 [IEEE Draft 802.3bs]
56GBaud PAM4 [OIF Draft oif2014.230.09]
56Gbps NRZ, 20dB [OIF Draft oif2016.101.00]
56Gbps NRZ, 13dB [OIF Draft oif2016.101.00]

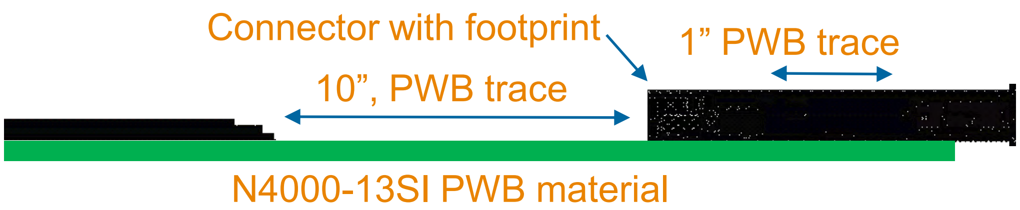
Assumptions to Determine 100G Target

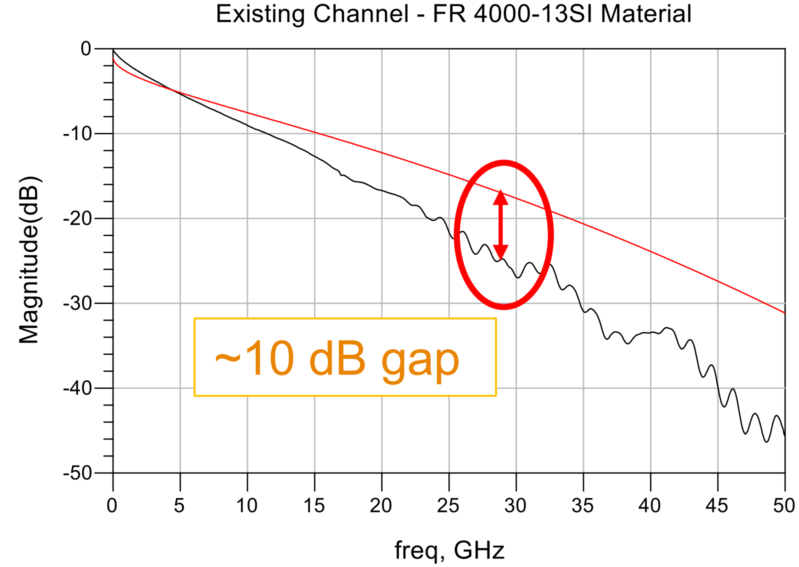
- Used 25G (published) and 50G (in development) OIF and IEEE industry standards as starting point
- Based on the shift towards PAM4 with the transition from 25G to 50G we can assume 100G will likely be PAM4
- Other encoding schemes were not considered but new emerging methods could enable next generation high speed links.
- For 100G the actual data rate will likely be 112Gbps with a Nyquist frequency around 28GHz (PAM4)
- The bandwidth of interest is assumed to be 10MHz – 56GHz
- The Insertion Loss/Return Loss requirements were extrapolated using a combination of,
    - Historical trends in data rate leaps, using current 50G targets as reference
    - Successful demonstrations of actual channels at 50G (PAM4 and NRZ)

Very Short Reach (Chip to Module) Limits



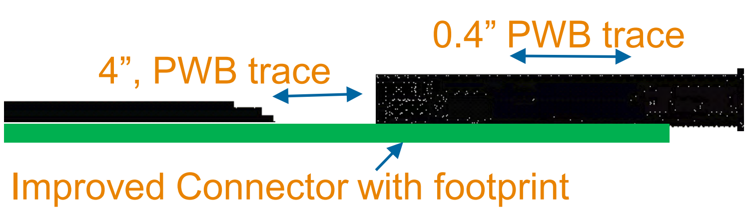
Existing VSR Channel vs New Limits



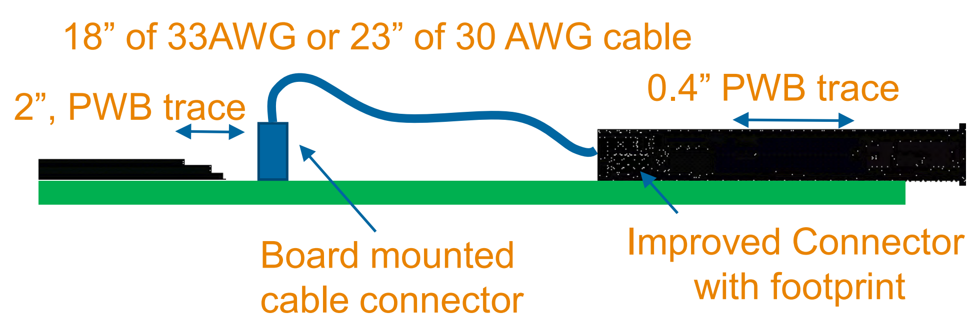


Two Possible Paths for Improvement

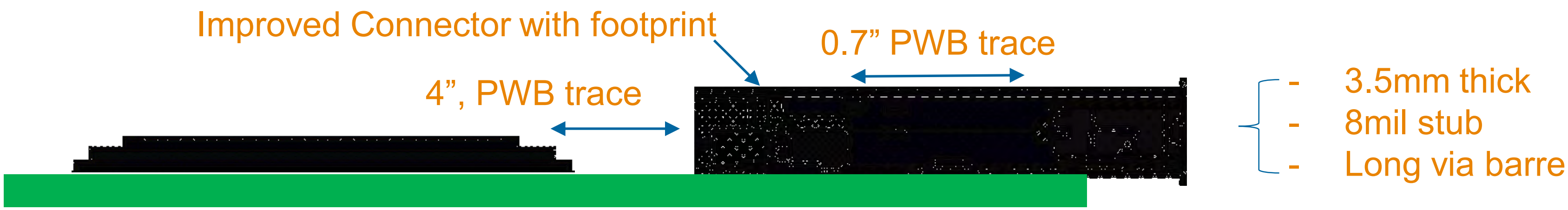
Reduce Channel Length

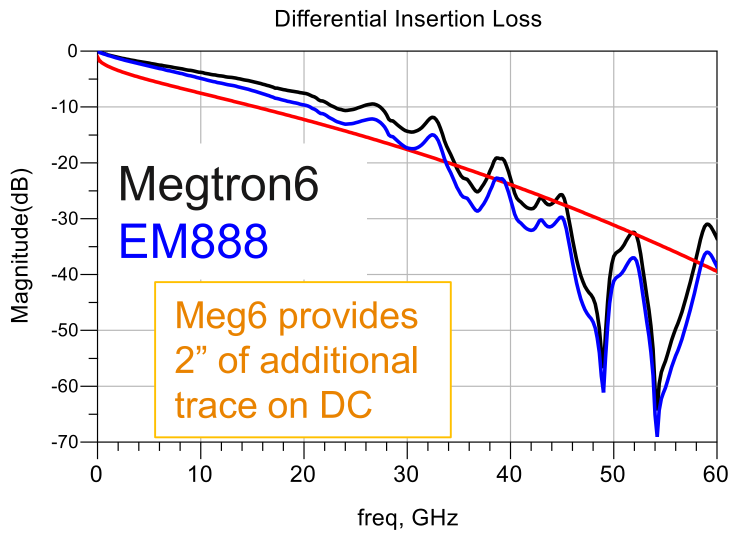


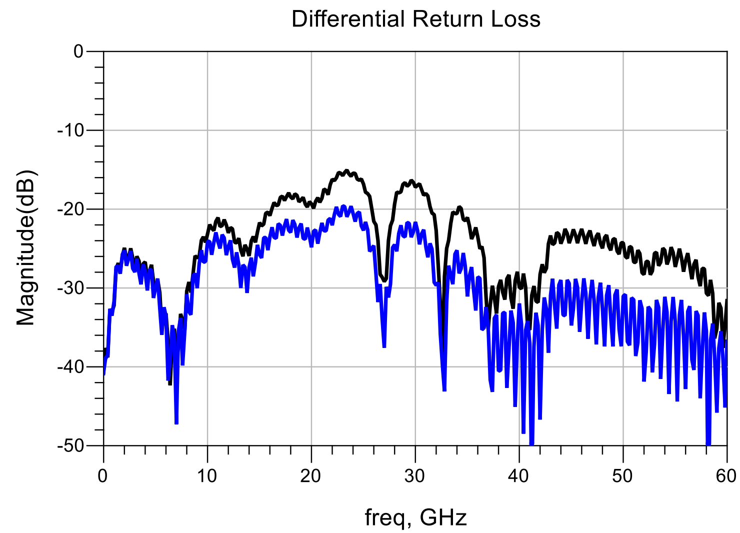
Use Lower Loss Channel



Shorter VSR Channels



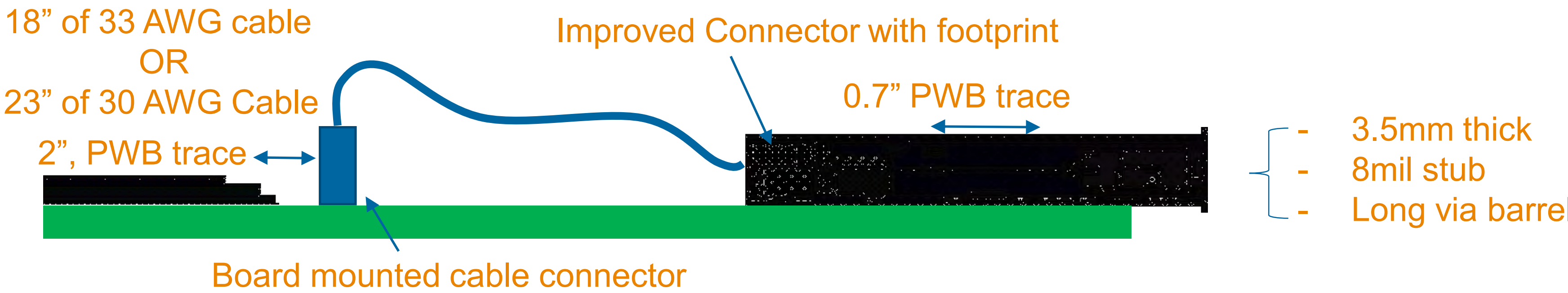


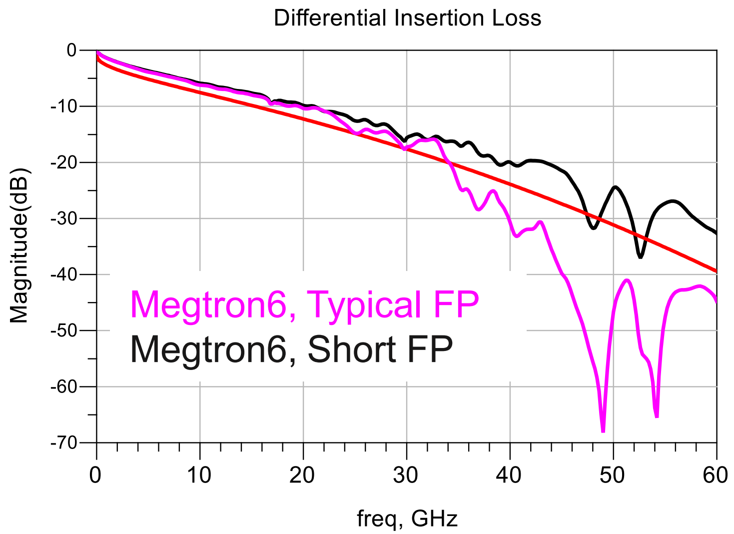


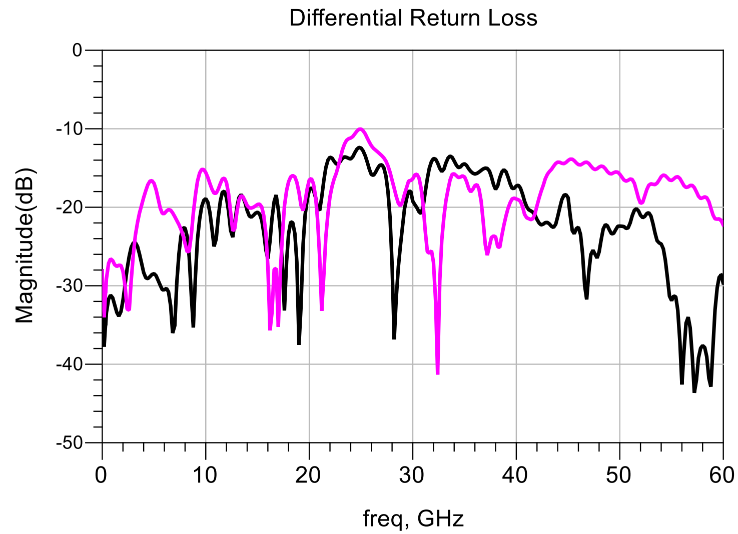
<u>Conclusions:</u>

- Passes up to the Nyquist frequency but may be impractical lengths
- Footprint is critical. FP causes significant degradation beyond 33GHz

Using Cables to Extend Channel Length







Conclusions:

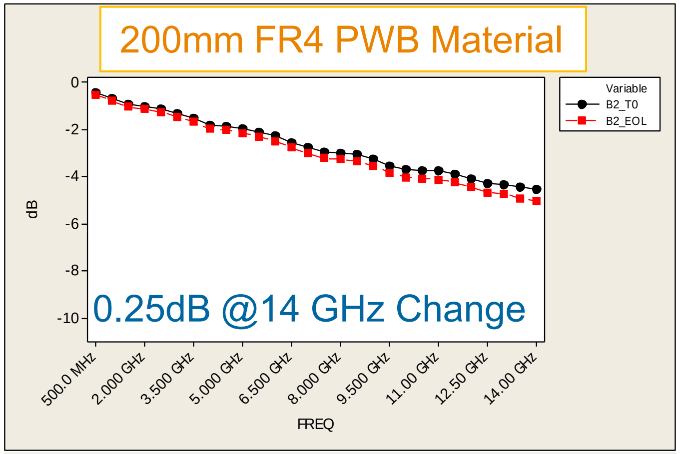
- Passes up to the Nyquist frequency with margin
- Utilizing cable provides extended reach and flexibility

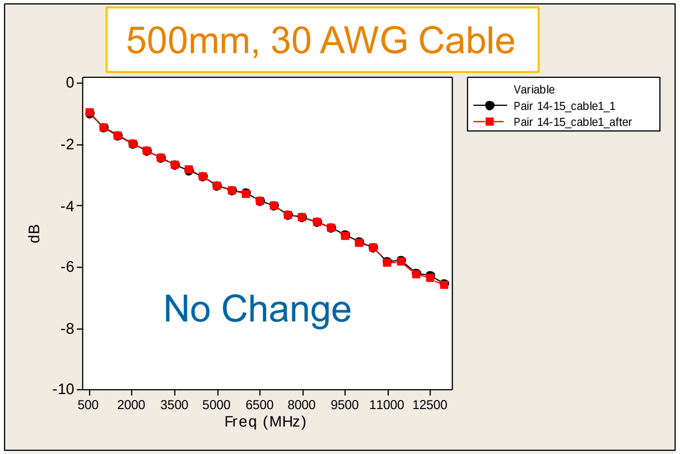
PCB vs. Cable Consistency Measurements

200mm PWB Megtron 6 traces vs. 500mm twinax cable assemblies

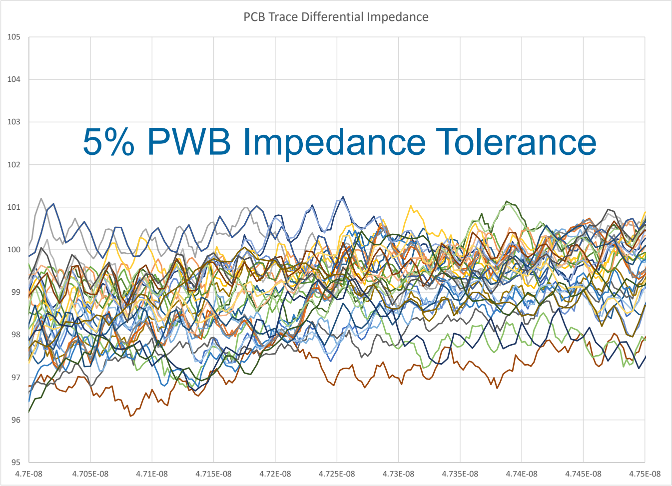
T_0 vs EoL: Temperature/Humidity cycling per EIA-364-31 Method III

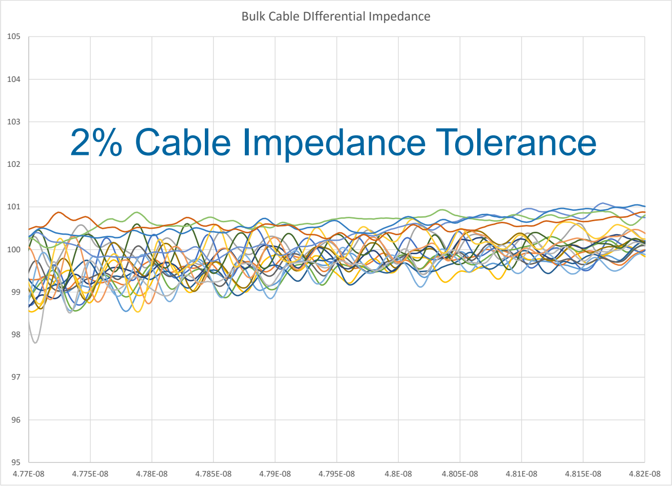
IL Variance During Temp/Humidity





Typical Impedance Variance

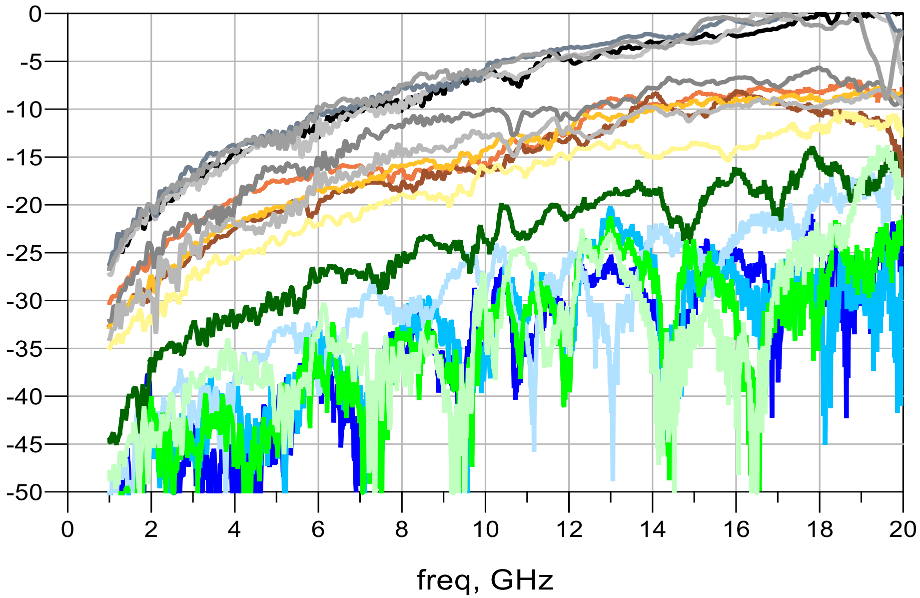




PCB & Cable Consistency Measurements

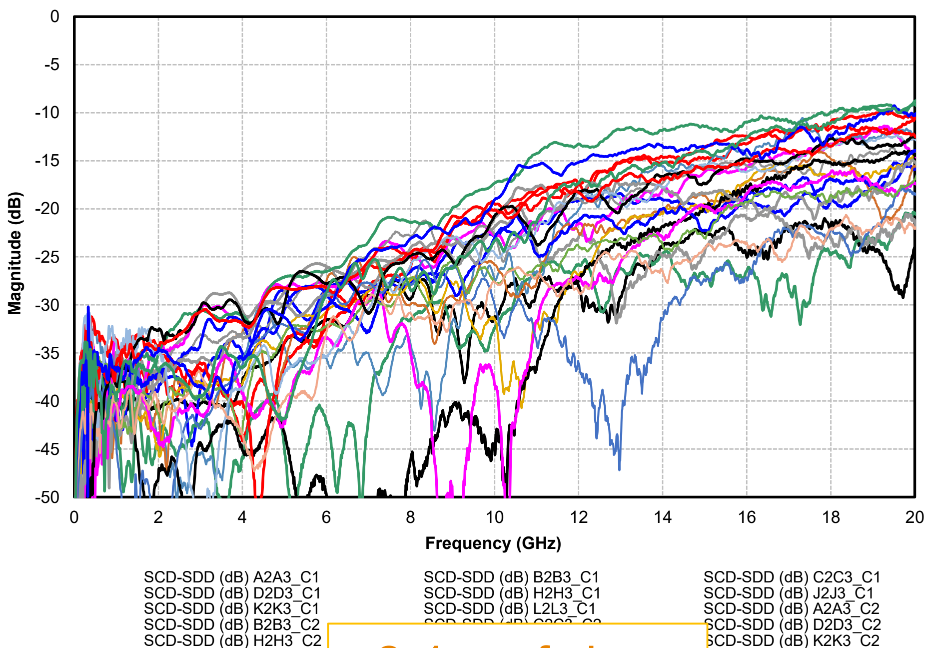
Mode Conversion (Skew) SCD21-SDD21 Measurements

27" PWB Megtron 6 traces vs. 1m twinax cable assemblies



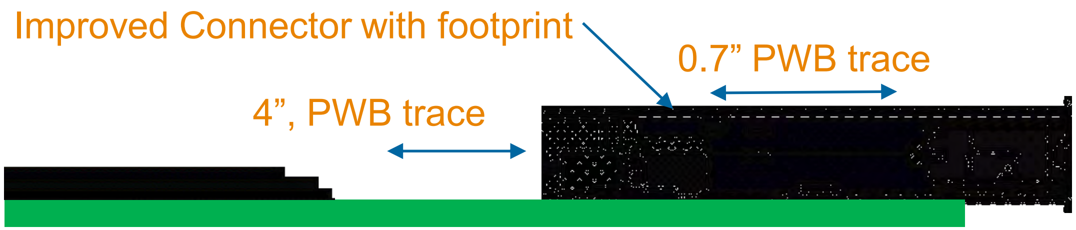
~6-8ps of skew

SCD21- SDD21All 3 Cables

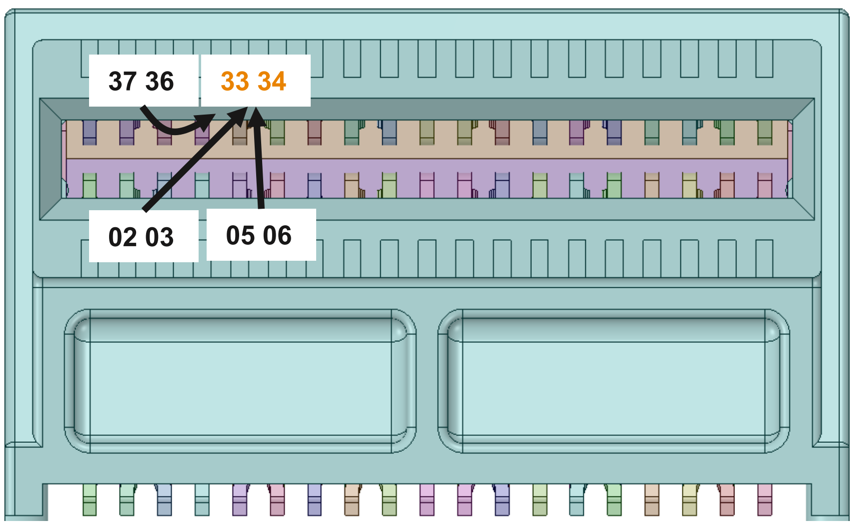


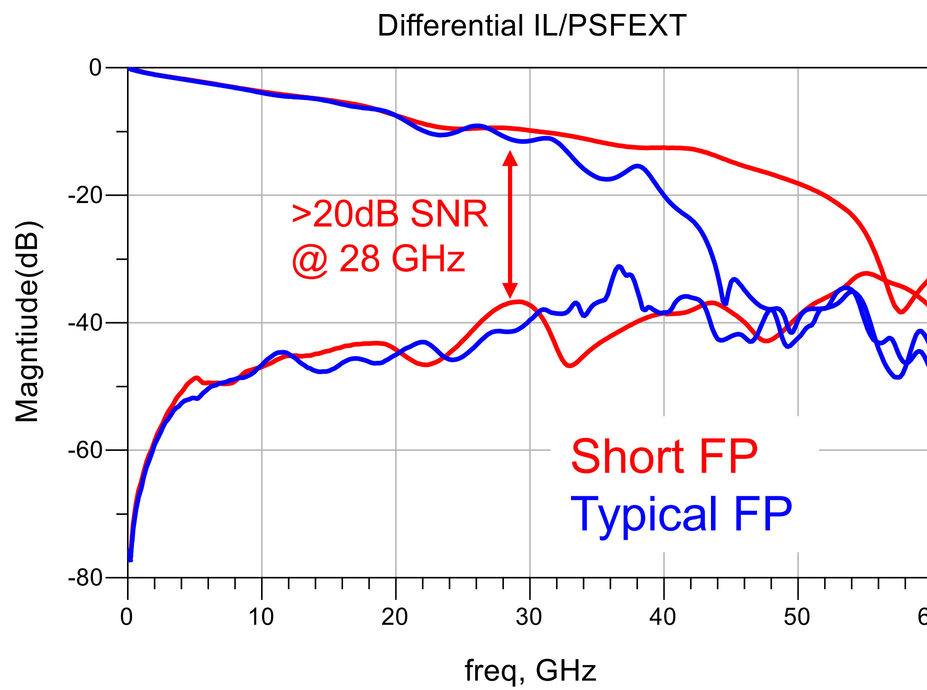
~2-4ps of skew

Typical Noise vs. IL in a Shorter VSR Channel

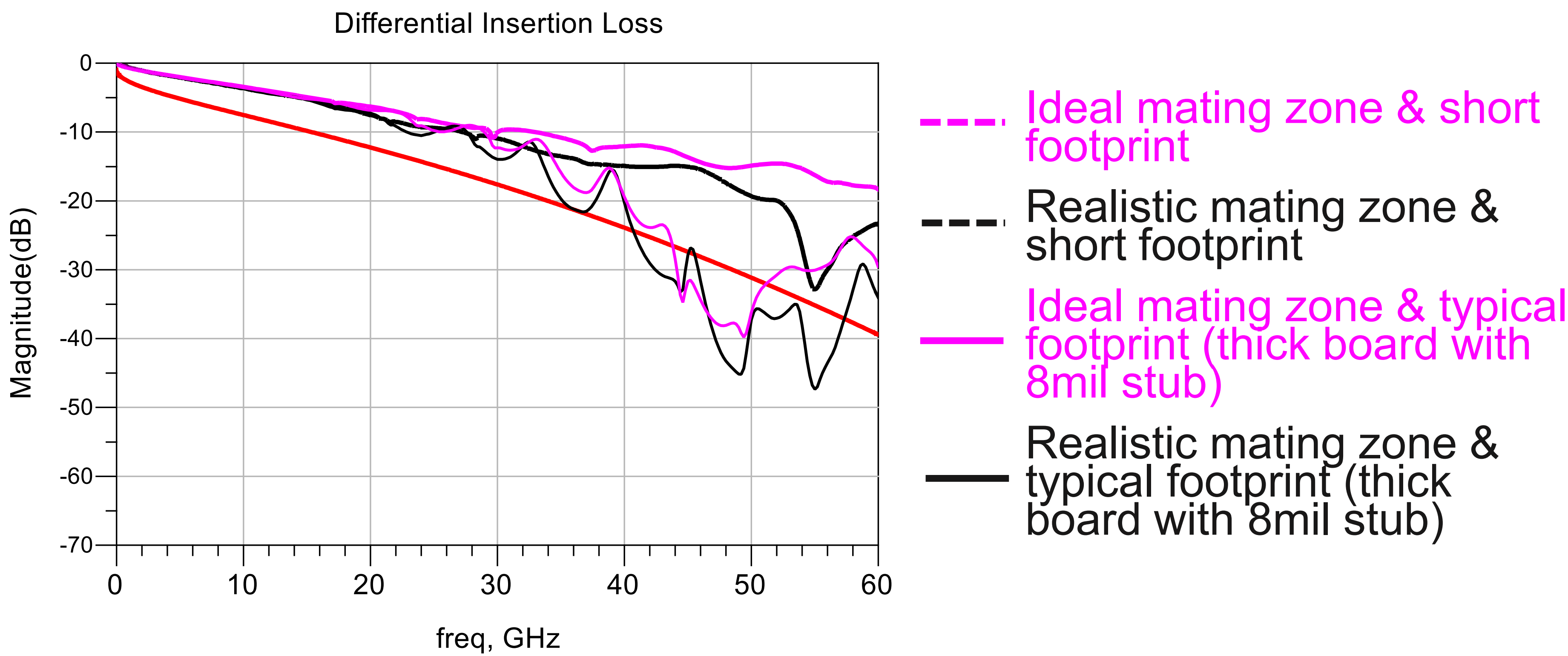


Typical FP	Short FP
- 3.5mm thick	- Micro-via
- 8mil stub	- No stub
- Long via barrel	- Short via barrel



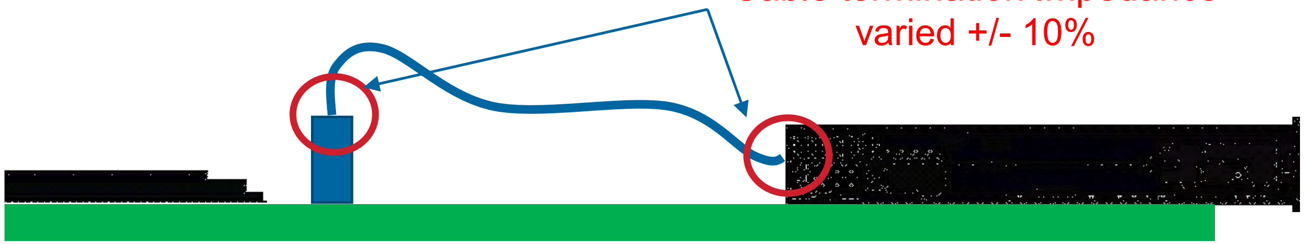


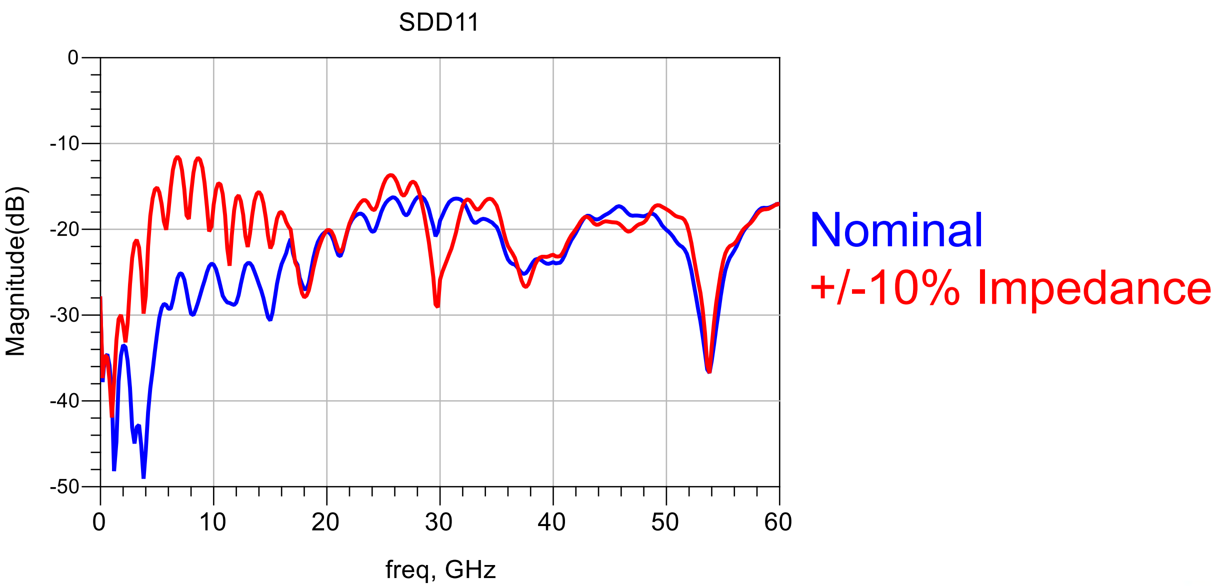
VSR Sensitivity to Connector Design



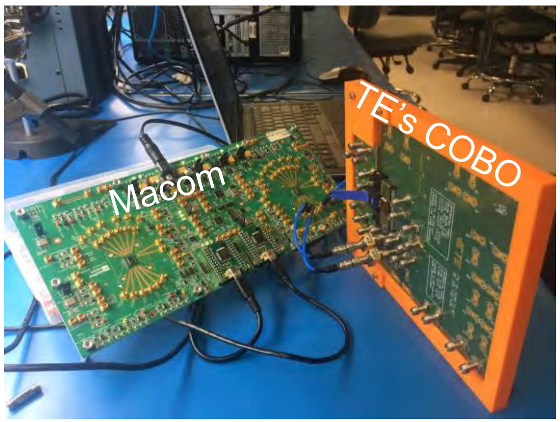
VSR Sensitivity to Cable Termination Variance

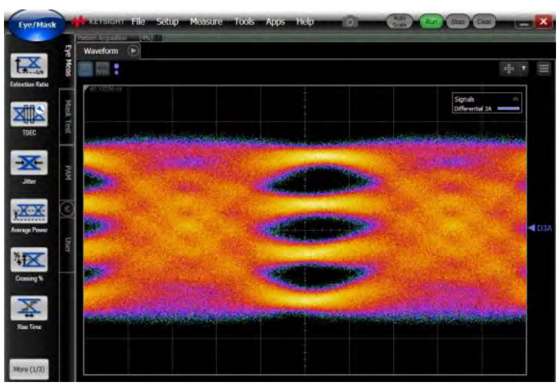
- Excess solder paste
- Inaccurate cable placement
- Stripping of signal insulation and shield
- Manufacturing control is critical





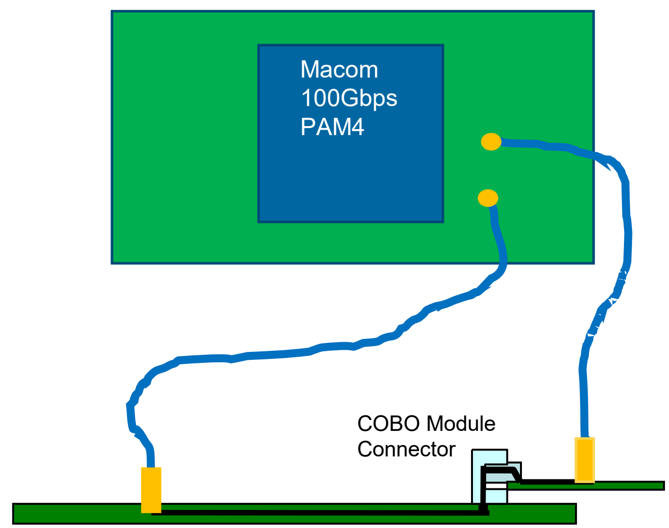
112 Gbps COBO Sliver Demo at DesignCon 2017





TE's COBO test board with Macom's serial 112Gbps silicon

10dB channel (7dB COBO channel plus 3 dB Macom test board)



Conclusions

Don't bet against 112Gbps copper for VSR channels

100G VSR channels are possible (multiple public demos)

New lower loss techniques should be implemented

Manufacturing consistency will be even more critical

Effects of footprints becoming as critical as the connector itself

Need better definition of silicon and package requirements