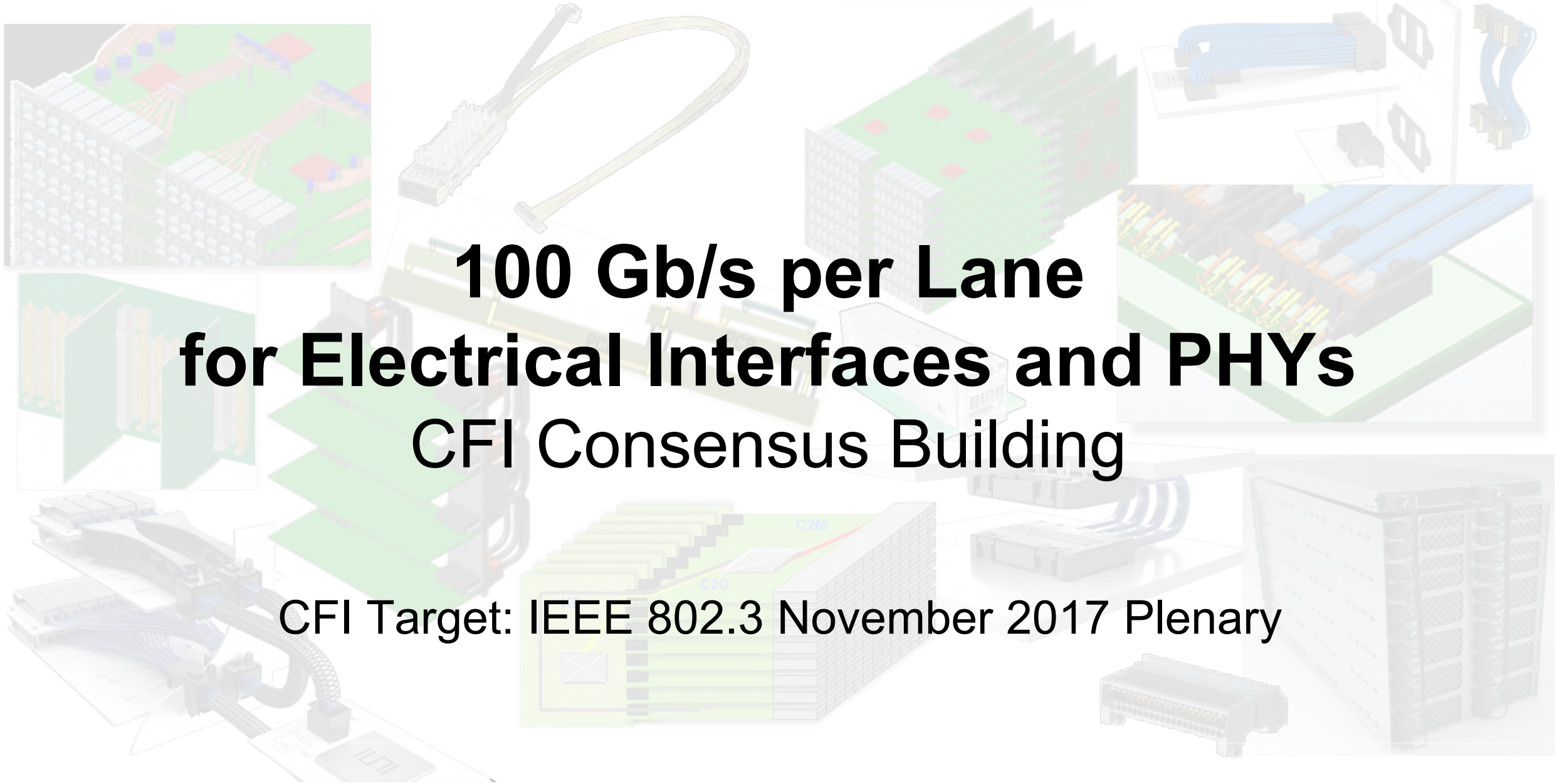


100 Gb/s per Lane for Electrical Interfaces and PHYs

CFI Consensus Building

CFI Target: IEEE 802.3 November 2017 Plenary

Objective

- Build consensus of starting a study group investigating a "100 Gb/s per lane for electrical interfaces and PHYs" project
- We do **not** need to:
  - Fully explore the problem
  - Debate strengths and weaknesses of solutions
  - Choose a solution
  - Create a PAR or 5 Criteria
  - Create a standard
- Anyone in the room may vote or speak

Introductions for today's presentation

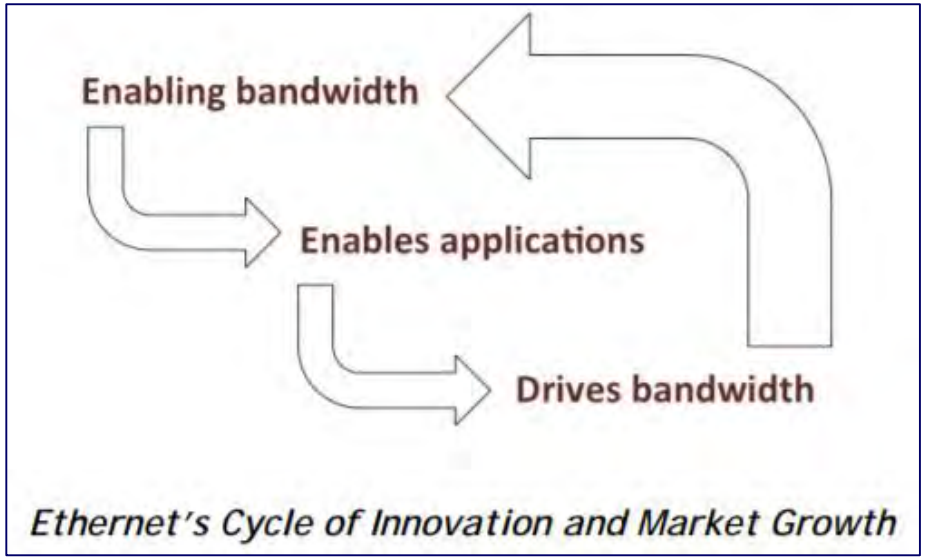
John D'Ambrosia, FutureWei Technologies & Beth Kochuparambil, Cisco Systems, Inc.	Intro
David O'felt, Juniper Networks	Market Drivers
Adam Healey, Broadcom	Technical Feasibility
Beth Kochuparambil, Cisco Systems, Inc.	Why Now? & Close

Motivation for 100 Gb/s per Lane

With next steps in Ethernet, comes the needed next step in interfaces.

- Faceplate density
- Chip breakout
- System throughput

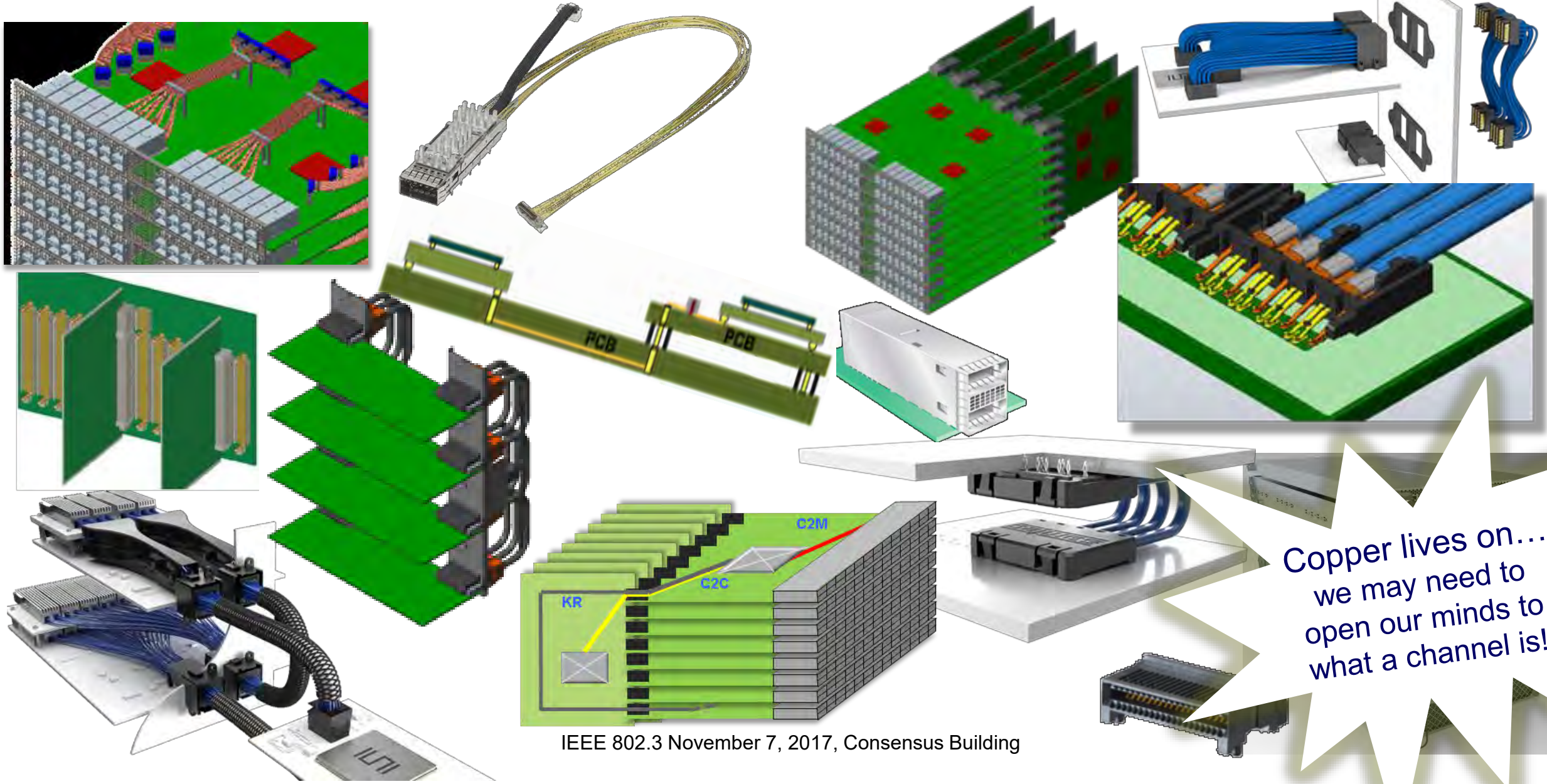
They are all tied together!



Ethernet's Cycle of Innovation and Market Growth

*Web-scale data centers and cloud based service are presented as leading applications

Electrical interfaces come in many shapes and sizes.



Tonight's Meeting

- To present the

  market ***NEED***,

  technical **Feasibility**,

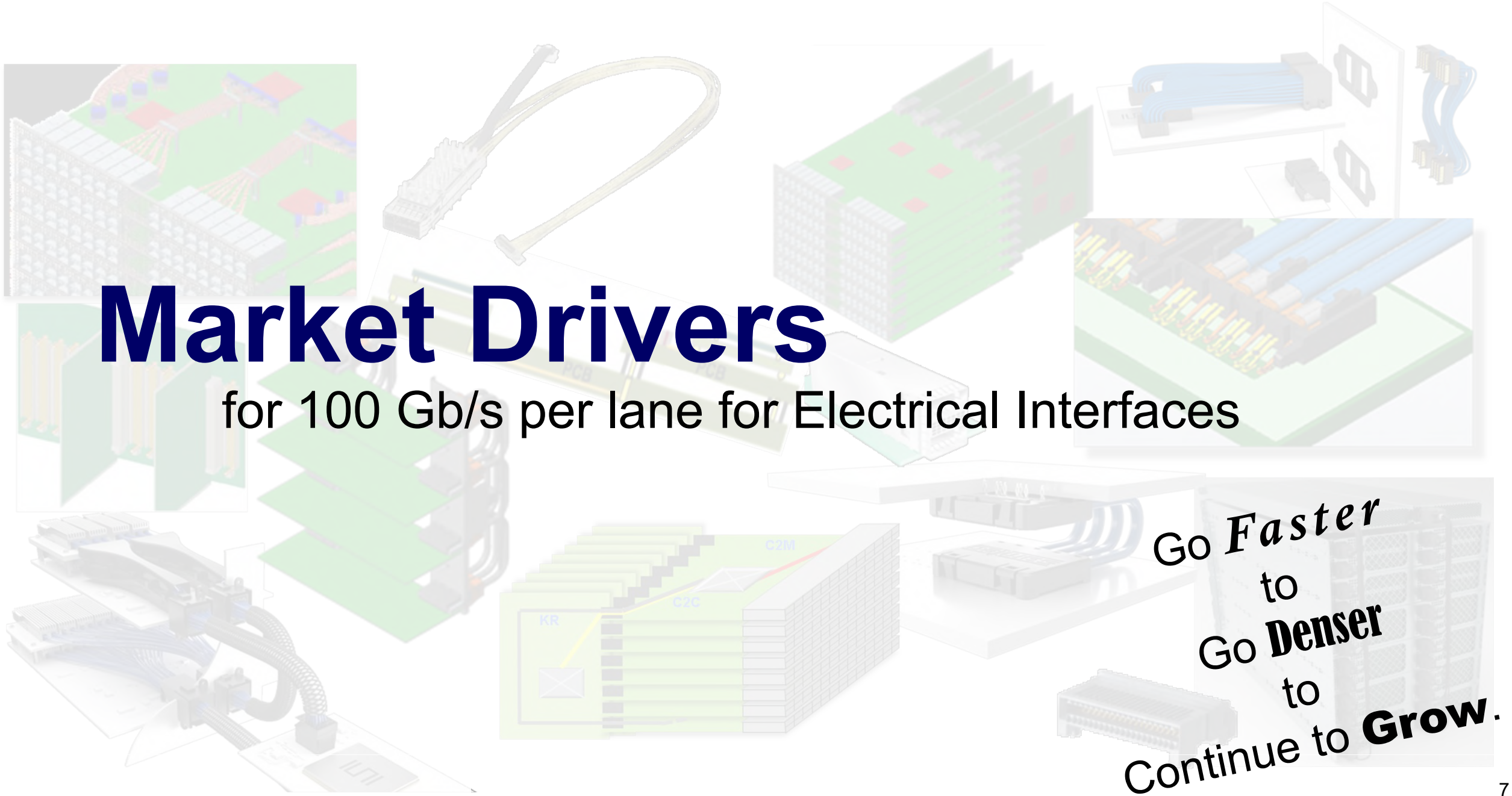
  and *Why Now??*

  of 100Gb/s per lane of electrical signaling.

- To gain consensus towards Thursday's motion to form a study group.
- We are NOT discussing specific implementations or objectives – these are just some of the reasons that we *need* a study group!

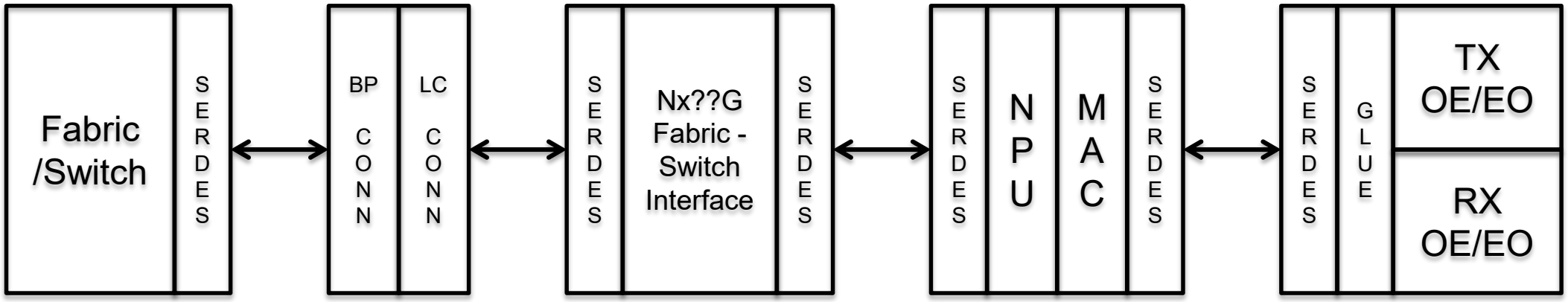
Market Drivers

for 100 Gb/s per lane for Electrical Interfaces

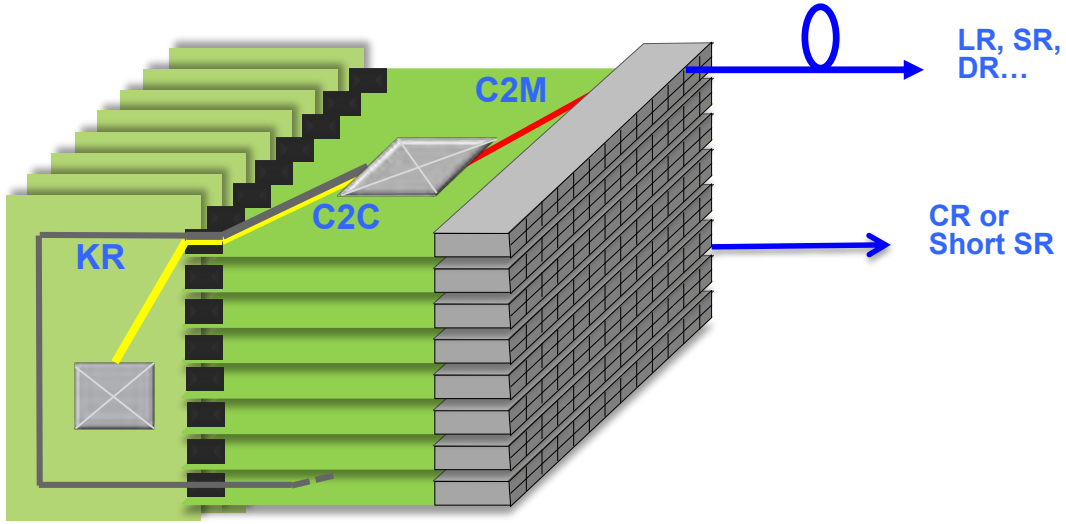


Go *Faster*
to
Go **Denser**
to
Continue to **Grow**.

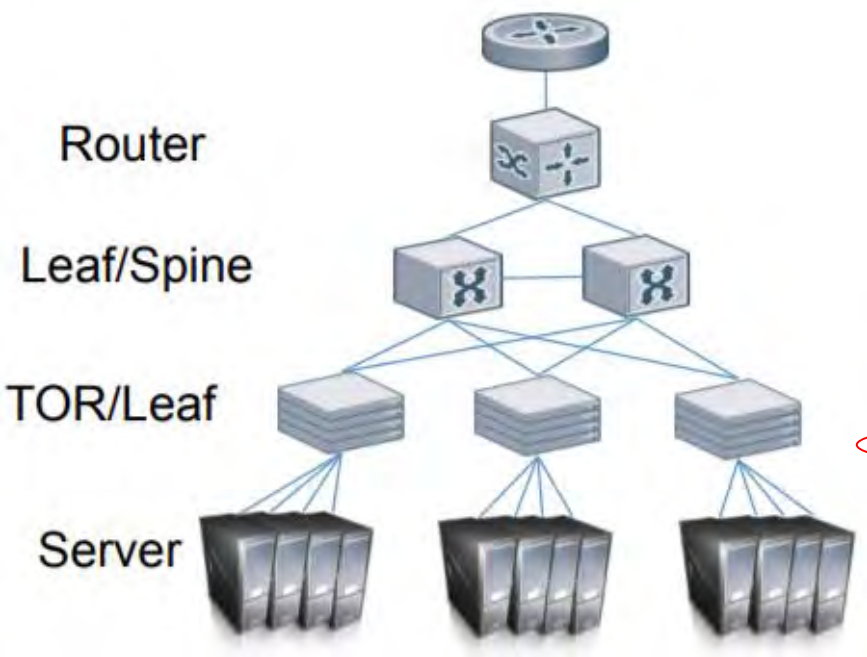
What Are We Talking About?



Consider how many instances of the interface can exist in the system…



Why Copper Cable??



Need to study
highly cost sensitive
and very short reach market.

Interconnection Volume

- Four sections per colo & multiple colos (≥ 4) per data center
- Volumes below are per section (except DCR to Metro)

A End	Z End	Volume	Reach (max)	Medium	Cost Sensitivity	Market Space
Server ǂ	TOR	10k – 100k	3 m	Copper	Extreme	
TOR	LEAF	1k – 10k	20 m	Fiber (AOC)	High	LAN
LEAF	SPINE	1k – 10k	400 m	SMF	High	
SPINE	DCR	100 – 1000	1,000 m	SMF	Medium	Campus
DCR	Metro	100 – 300	10 - 80 km	SMF	Low	WAN

ǂ Server-TOR links may be served by breakout cables

9 IEEE 802.3 400G Study Group - November 2013

Source: Brad Booth, Microsoft http://www.ieee802.org/3/400GSG/public/13_11/booth_400_01a_1113.pdf

*Note that data is from 2013, however data center architecture hasn't drastically changed in recent years

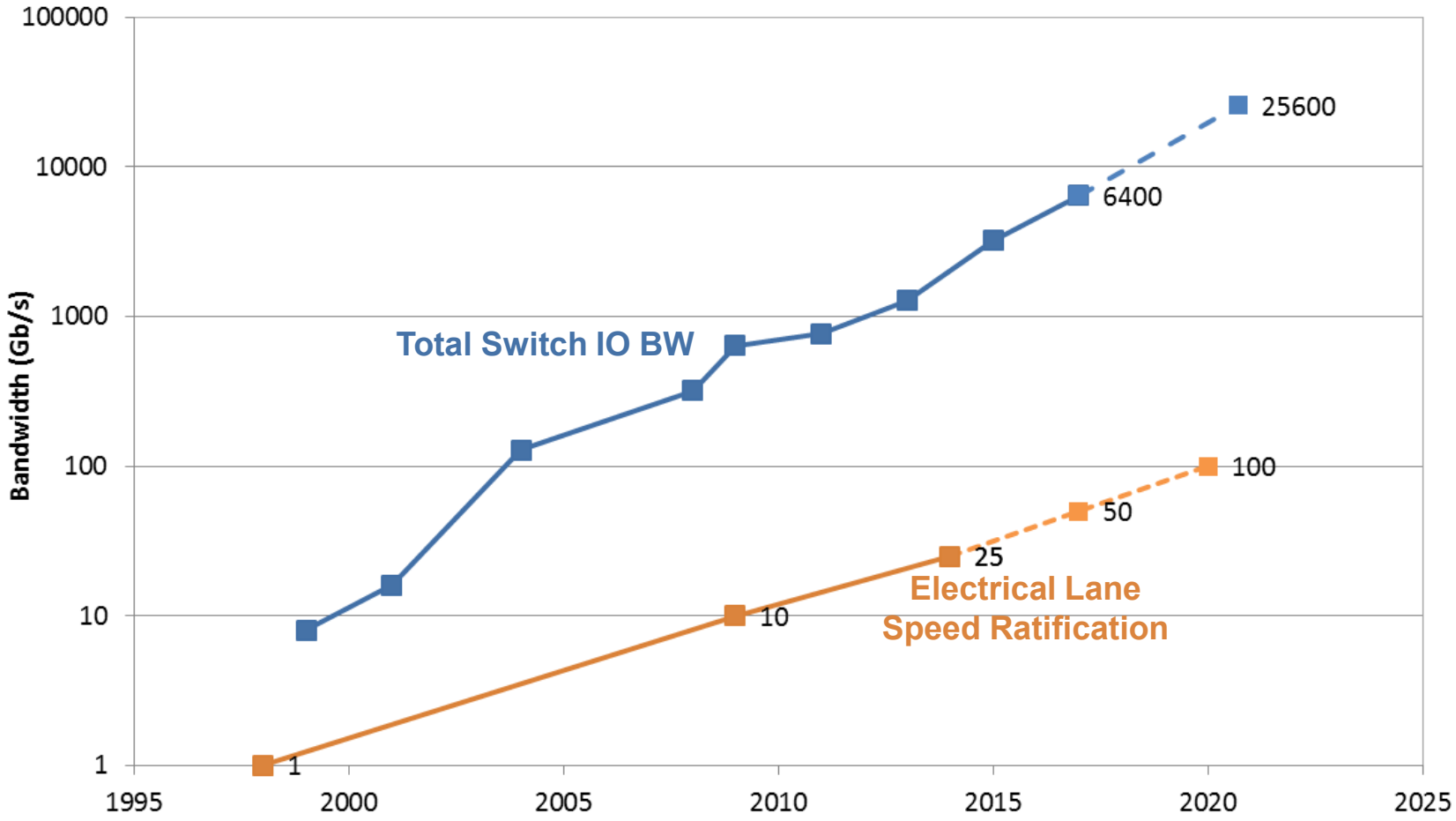
Faceplate Evolution

Increased faceplate density

Requires smaller form factors

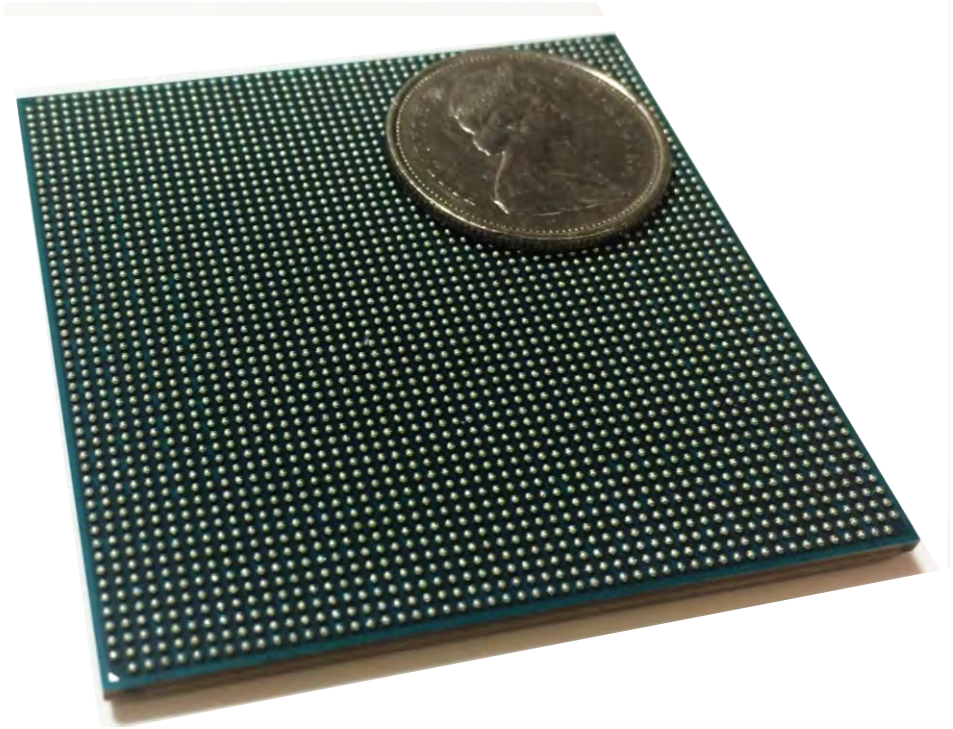
Enabled by faster AUIs
(per lane speed)

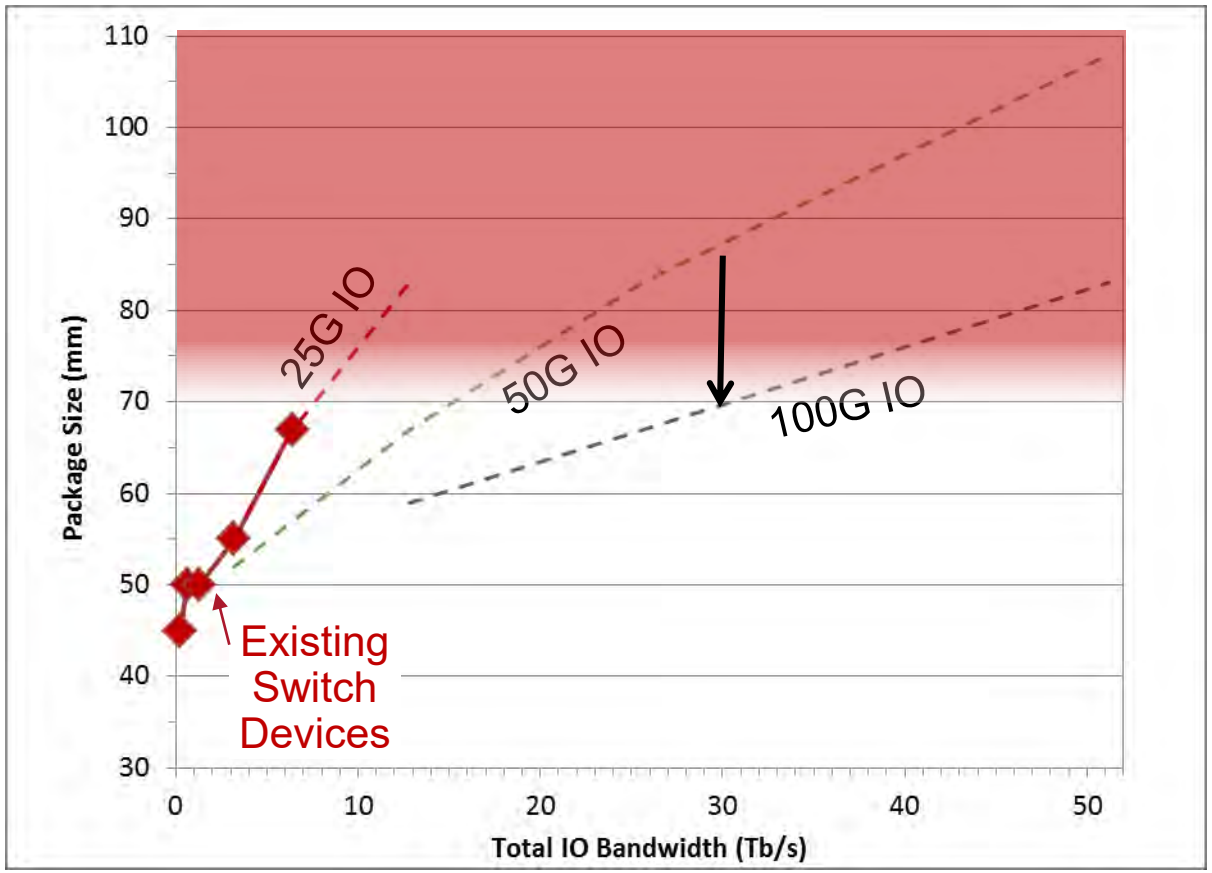
Historical Perspective Shows What's Coming



- Historical curve fit to highest rate switch products introduced to market (blue squares)
- Single ASIC IO capacity doubling every ~ 2 years

IO Escape forcing transition to higher lane speeds





- ~ 70mm package is a current BGA practical maximum (due to coplanarity / warpage)
- BGA devices with > 14Tb/s of aggregate bandwidth are forced to transition to lane rates beyond 50G

Backplane is easily system bottleneck

Finite space created by line card size and card pitch

Example: 52-55 diff. pairs per inch

Existing Systems

Defined backplane and pin count

No choice but to put more signal across the pin

New Systems

Can tune pitch and pin count

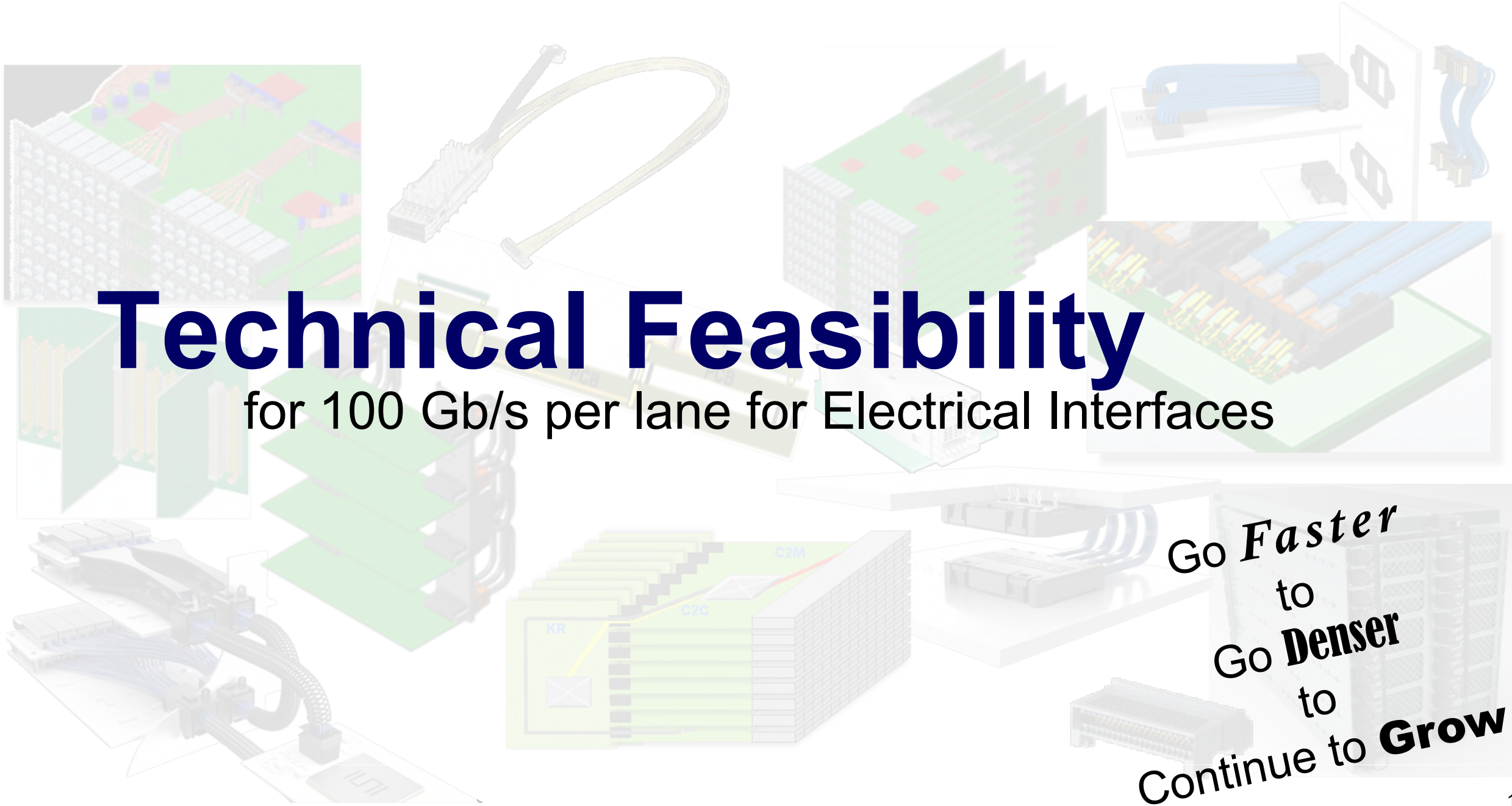
However, there is limited gain left in this mechanical density

backplane speed needs to scale for bandwidth to grow

The Current Ethernet Family (100 Gb/s and Above)

	Signaling (Gb/s)	Electrical Interface	Backplane	Twin-ax	MMF	500m SMF	2km SMF	10km SMF	40km SMF
100GBASE-	10	CAUI-10		CR10	SR10		10X10		
	25	CAUI-4 / 100GAUI-4	KR4	CR4	SR4	PSM4	CWDM4 CLR4	LR4	ER4
	50	100GAUI-2	KR2	CR2	SR2		-		
	100	?	?	?		DR			
200GBASE-	25	200GAUI-8							
	50	200GAUI-4	KR4	CR4	SR4	DR4	FR4	LR4	
	100	?	?	?					
400GBASE-	25	400GAUI-16			SR16				
	50	400GAUI-8					FR8	LR8	
	100	?	?	?		DR4			

Includes Ethernet standards in development
Underlined – indicates industry MSA or proprietary solutions
Blue – indicates the areas of interest for this CFI

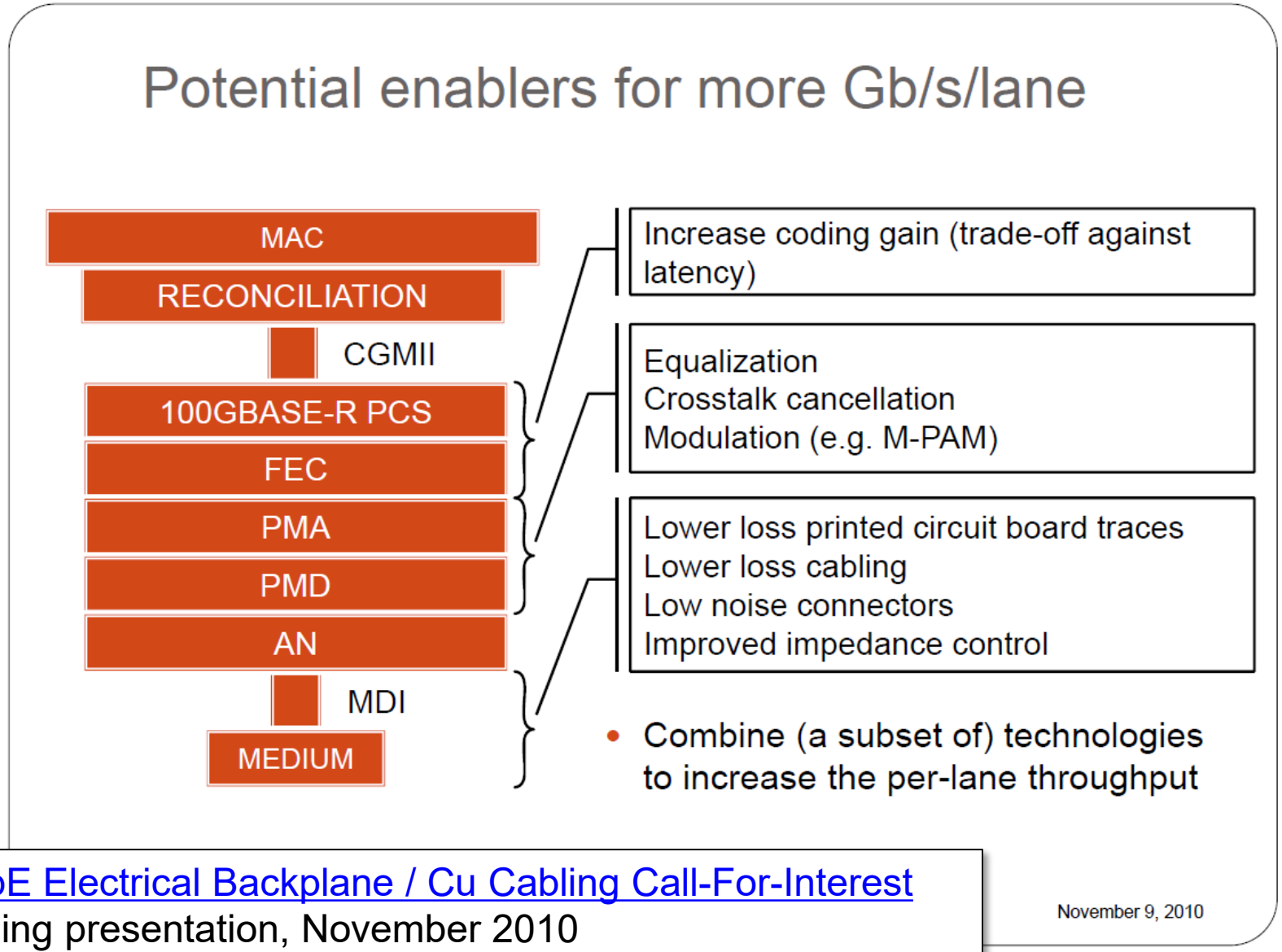


Technical Feasibility

for 100 Gb/s per lane for Electrical Interfaces

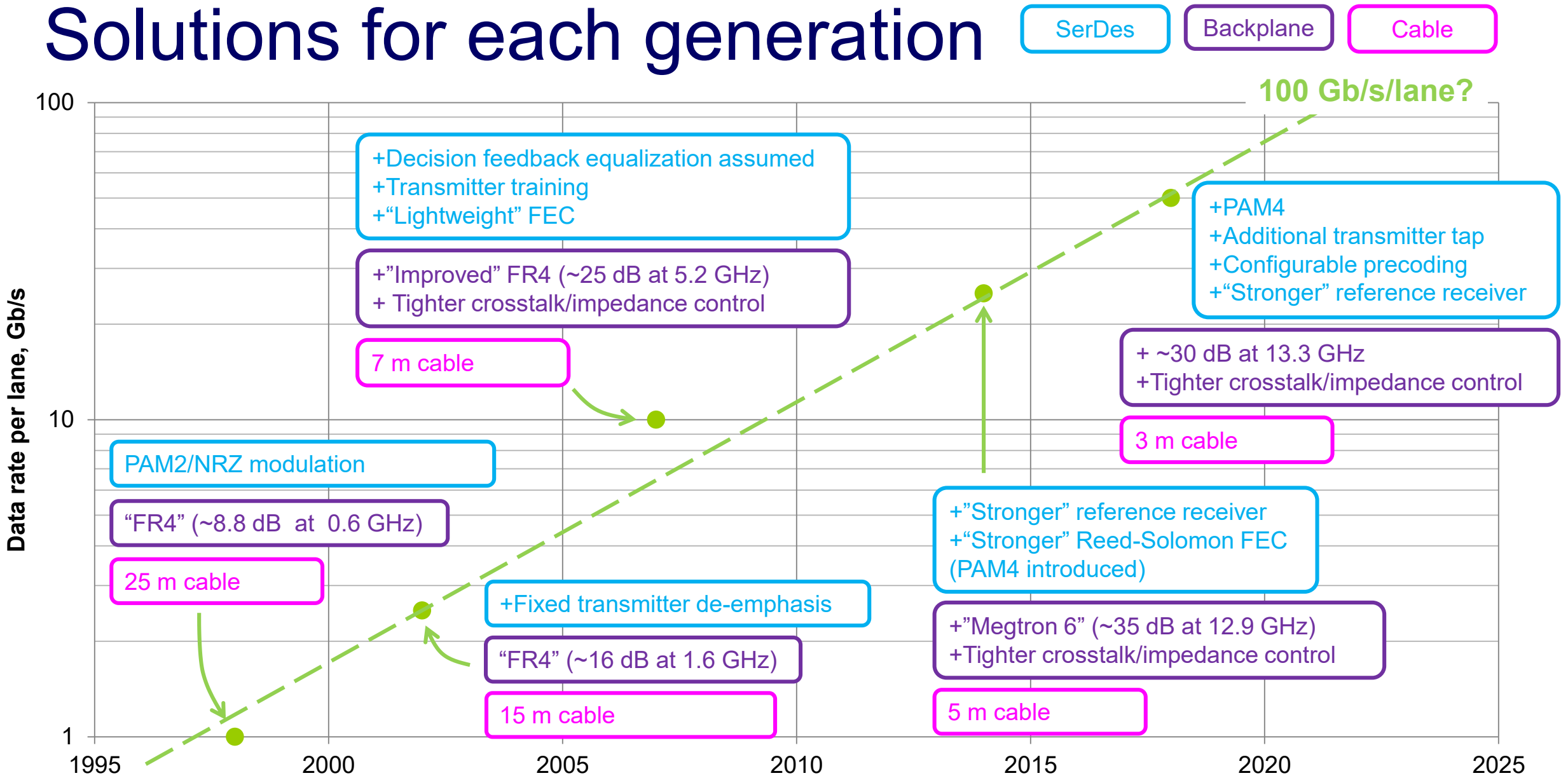
Go *Faster*
to
Go **Denser**
to
Continue to **Grow**.

It’s time to open the toolbox again…



From the [100GbE Electrical Backplane / Cu Cabling Call-For-Interest] consensus building presentation, November 2010

Solutions for each generation



* Dates are approximate

Different constraints for different applications

Chip-to-module

- What is the insertion loss range that supports useful applications?
- How can we “Coexist” with defined PHYs, including FEC & PCS?
- Consider improved PCB materials, PCB vs. cable, improvements in impedance/noise control

Chip-to-chip and “backplane”

- What are useful topologies? What implications are acceptable?
- Consider improved PCB materials, PCB vs. cable, improvements in impedance/noise control?

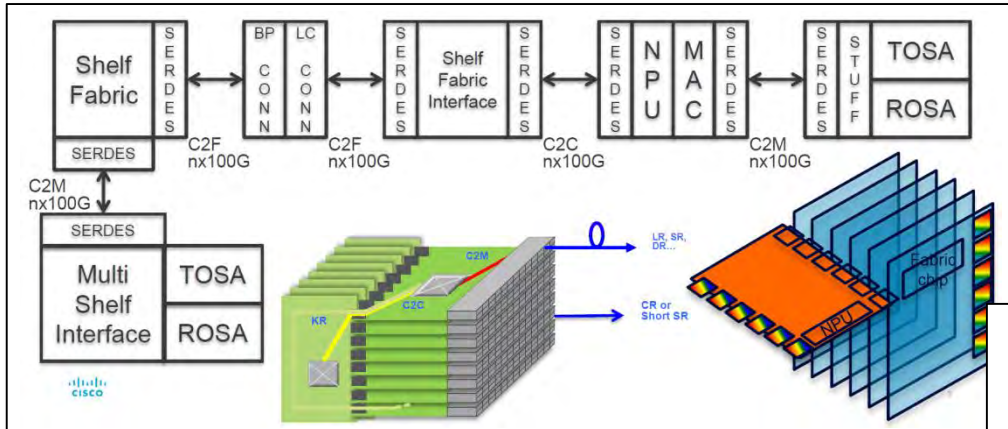
Cable

- What is the minimum useful reach?
- Consider “middle-of-rack” topologies?
- How can we “Coexist” with defined PHYs, including FEC & PCS?

Apply signal processing to meet the needs of each application

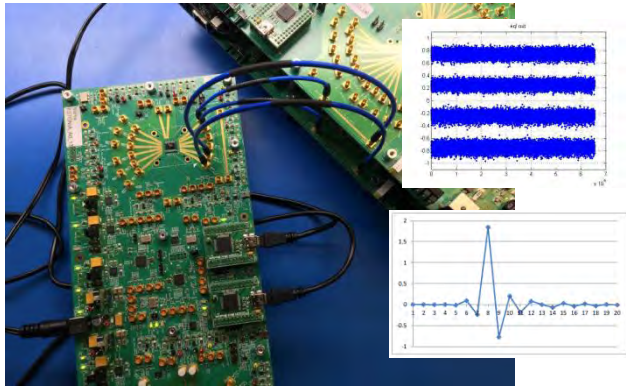
The discussion is already underway

From the proceedings of the IEEE 802.3 New Ethernet Applications ad hoc

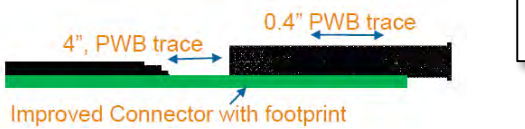


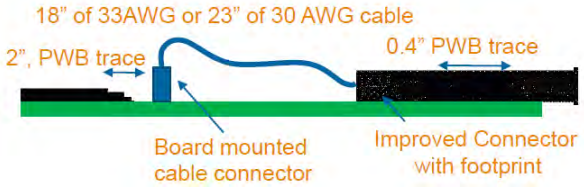
http://www.ieee802.org/3/ad_hoc/ngrates/public/17_05/goergen_nea_01_0517.pdf

System considerations
Channel options
Higher-speed SerDes

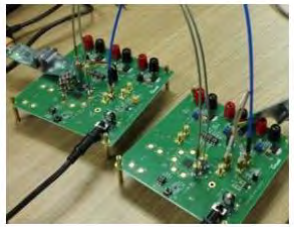


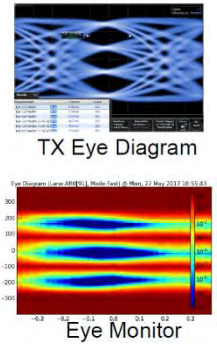
http://www.ieee802.org/3/ad_hoc/ngrates/public/17_05/palkert_nea_02_0517.pdf



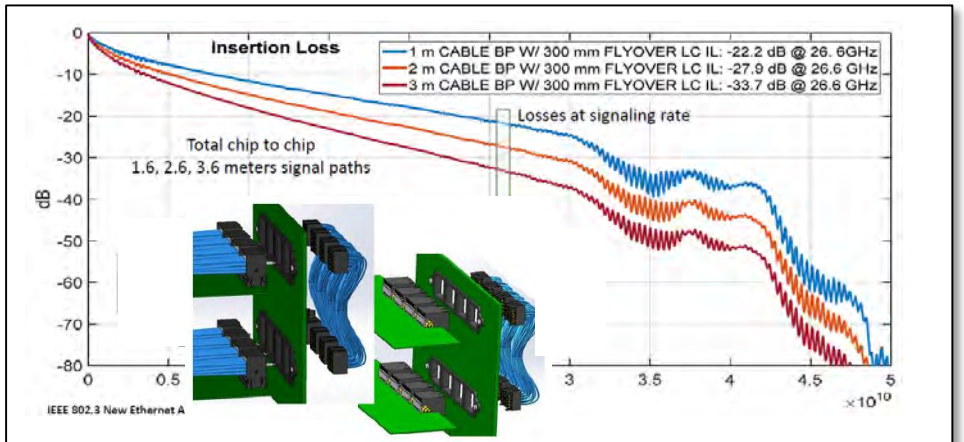


http://www.ieee802.org/3/ad_hoc/ngrates/public/17_05/tracy_nea_01_0517.pdf





http://www.ieee802.org/3/ad_hoc/ngrates/public/17_05/sun_nea_01a_0517.pdf



http://www.ieee802.org/3/ad_hoc/ngrates/public/17_05/mellitz_nea_01a_0517.pdf

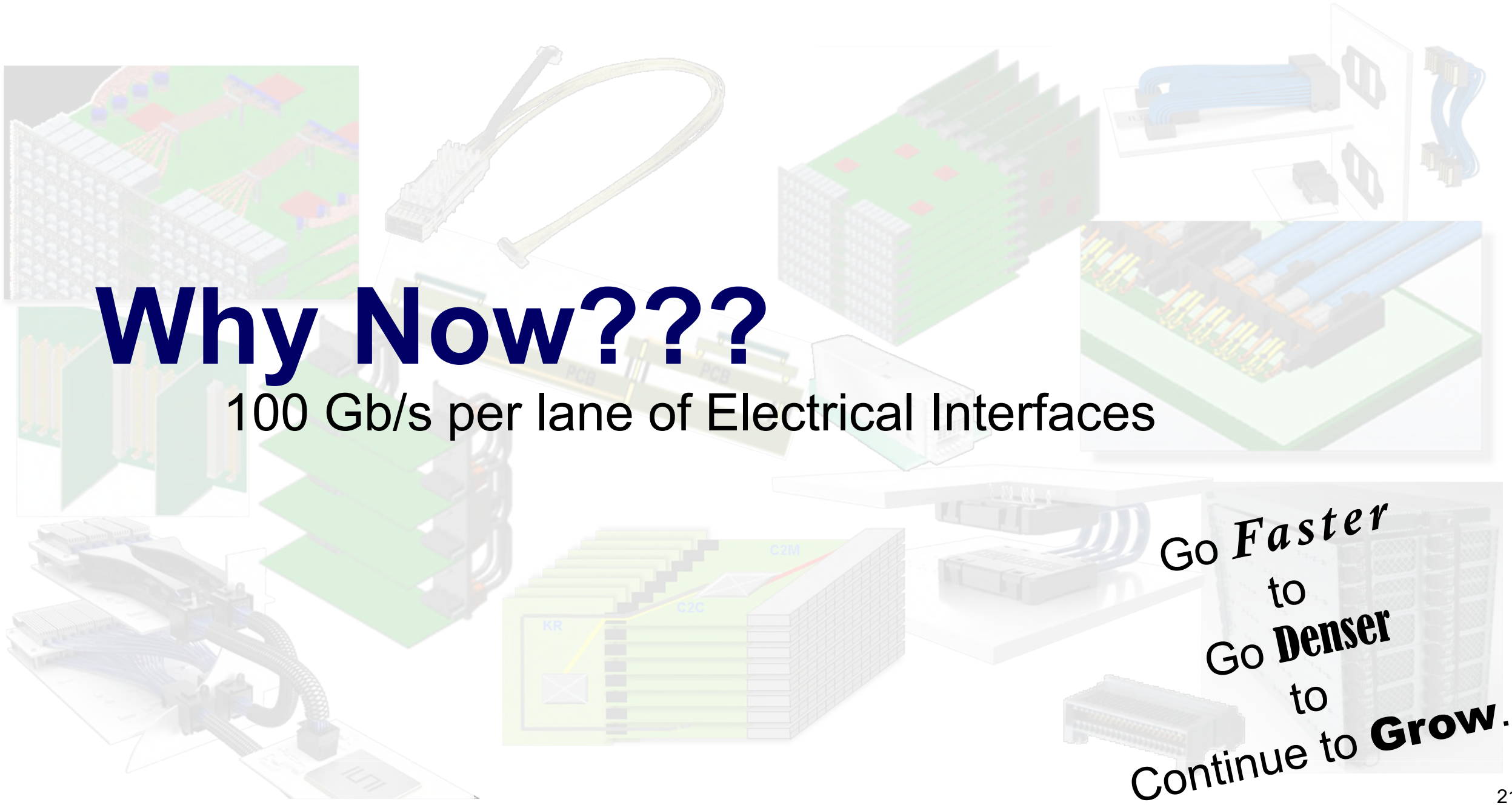
OIF has CEI 112G VSR and LR projects are already underway

Technical feasibility summary

- Rich signal integrity and signal processing toolbox that can be applied to the problem of “100 Gb/s per lane electrical signaling”
- We must be mindful of the different needs for different applications
- We have done this many times before
- The discussion is already underway

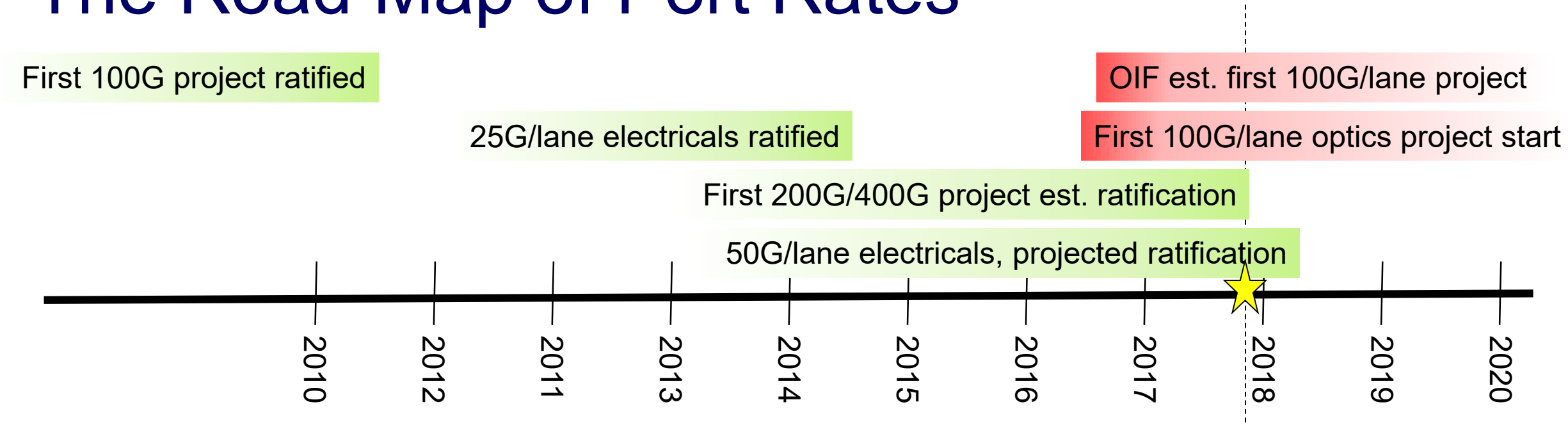
Why Now???

100 Gb/s per lane of Electrical Interfaces



Go *Faster*
to
Go **Denser**
to
Continue to **Grow**.

The Road Map of Port Rates



- 100G/200G/400G technology is already out
- 100G per lane optics has begun, more to come
- OIF is already working on this
- 100G per lane is coming...

→ IEEE needs to study and frame it NOW so the industry can plan Gb/s

Supporters (more to come)

- Yang Zhiwei, ZTE
- Mark Gustlin, Xilinx
- Paul Brooks, Viavi Solutions
- Nathan Tracy, TTM Technologies
- Toshiaki Sakai, Socionext
- Mabud Choudhury, OFS
- Tom Palkert, Molex/Macom
- Matt Brown, Macom
- Dale Murray, Lightcounting
- Steve Sekel, Keysight Technologies
- David Ofelt, Juniper
- Rick Rabinovich, IXIA
- Scott Schube, Intel
- Adee Ran, Intel
- Kent Lusted, Intel
- Hai-Feng Liu, Intel
- Mike Li, Intel
- Howard Heck, Intel
- David Chalupsky, Intel
- Ted Sprague, Infinera
- Andre Szczepanek, HSZ Consulting
- Yasuo Hidaka, Fujitsu Lab of America
- Vipul Bhatt, Finisar
- Phil Sun, Credo Semiconductor
- Joel Goergen, Cisco Systems
- Mark Nowell, Cisco Systems
- Jane Lim, Cisco Systems
- Mike Dudek, Cavium
- Rob Stone, Broadcom
- Raj Hegde, Broadcom
- Adam Healey, Broadcom
- Henry Chen, Broadcom
- Ramin Farjad, Aquantia
- Andy Zambell, Amphenol ICC

Summary

- 100 Gb/s is the next step on “Follow the SerDes” and continues existing market trends
- We’ve moved to the “unknown” before and the industry flourished.
- Technical details need to be rebalanced for the next speed.
- Impact of 100 Gb/s Electrical Signaling is wide across the Ethernet Family
- Let’s form a Study Group!!

Thank You!

Go *Faster*
to
Go **Denser**
to
Continue to **Grow**.