CMOS technology timelines

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Introduction

- A key component in supporting higher Ethernet and lane rates is the CMOS technology used on the PHY devices.
- This presentation provides a comparison of the timeline for CMOS technologies and Ethernet lane rates.
- The following presentation provides the Ethernet electrical lane rate timeline.
  - https://www.ieee802.org/3/ad_hoc/ngrates/public/calls/20_0604/brown_nea_01a_200604.pdf

CMOS Technology

- The key parameter for comparison of CMOS technologies is the node label, e.g., 10 nm, 7 nm, 5 nm.
  - The power and density scale approximately in relation to the node label magnitude.
- The supported (production) node label ranges from 10 nm in 2017 to 2.1 nm in 2025 based on the following sources:
  - “International Roadmap for Devices and Systems, 2020 Edition, Executive Summary”
  - “International Roadmap for Devices and Systems, 2018 Edition, Executive Summary”
  - Available here: https://irds.ieee.org/

CMOS Roadmap (IRDS 2020)

Table ES2 Overall Roadmap Technology Characteristics

2020 IRDS Executive Summary Drivers-ORTC								
YEAR OF PRODUCTION	2019	2020	2022	2025	2028	2031	2032	2034
Logic device technology naming [4] NEW node definition	G54M38	G48M36	G45M24	G45M20	G40M16	G38M16T2	G38M16T3	G38M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0nm-eq"	"1.0nm-eq"	"0.7nm-eq"
Logic device structure options	FinFET	FinFET	FinFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA	LGAA-3D VGAA
LOGIC CELL AND FUNCTIONAL FABRIC TARGETS								
Average Cell Width Scaling Factor Multiplier	1	0.9	0.9	0.9	0.9	0.9	0.9	0.9
LOGIC DEVICE GROUND RULES								
MPU/SoC M0 1/2 Pitch (nm) [1,2]	18	15	12	10.5	8	8	8	8
Physical Gate Length for HP Logic (nm) [3]	20	18	16	14	12	12	12	12
Lateral GAA (nanosheet) Minimum Thickness (nm)				7	6	5	5	5
Minimum Device Width (FinFET fin, nanosheet, SRAM) or Diameter (nm)	9	7	6	7	6	6	6	6
LOGIC DEVICE Electrical								
Vdd (V)	0.75	0.7	0.7	0.65	0.65	0.6	0.6	0.6
DRAM TECHNOLOGY								
DRAM Min half pitch (nm) [1]	18	17.5	17	14	11	8.4	8.4	7.7
DRAM Min Half Pitch (Calculated Half pitch) (nm) [1]	20.5	17.5	18.5	15	12	10	10	8.5
DRAM Cell Size Factor: aF^2 [4]	6	6	4	4	4	4	4	4
DRAM Gb/1chip target	8	8	16	16	32	32	32	32
NAND Flash								
Flash 2D NAND Flash uncontacted poly 1/2 pitch – F (nm) 2D [1][2]	15	15	15	15	15	15	15	15
Flash Product highest density (independent of 2D or 3D)	512G	1T	1T	1.5T	3T	4T	4T	4T+
Flash Product Maximum bit/cell (2D_3D) [6]	2_4	2_4	2_4	2_4	2_4	2_4	2_4	2_4
Flash 3D NAND Maximum Number of Memory Layers [6]	48-65	64-96	96-128	128-192	256-384	384-512	384-512	512+

https://irds.ieee.org/

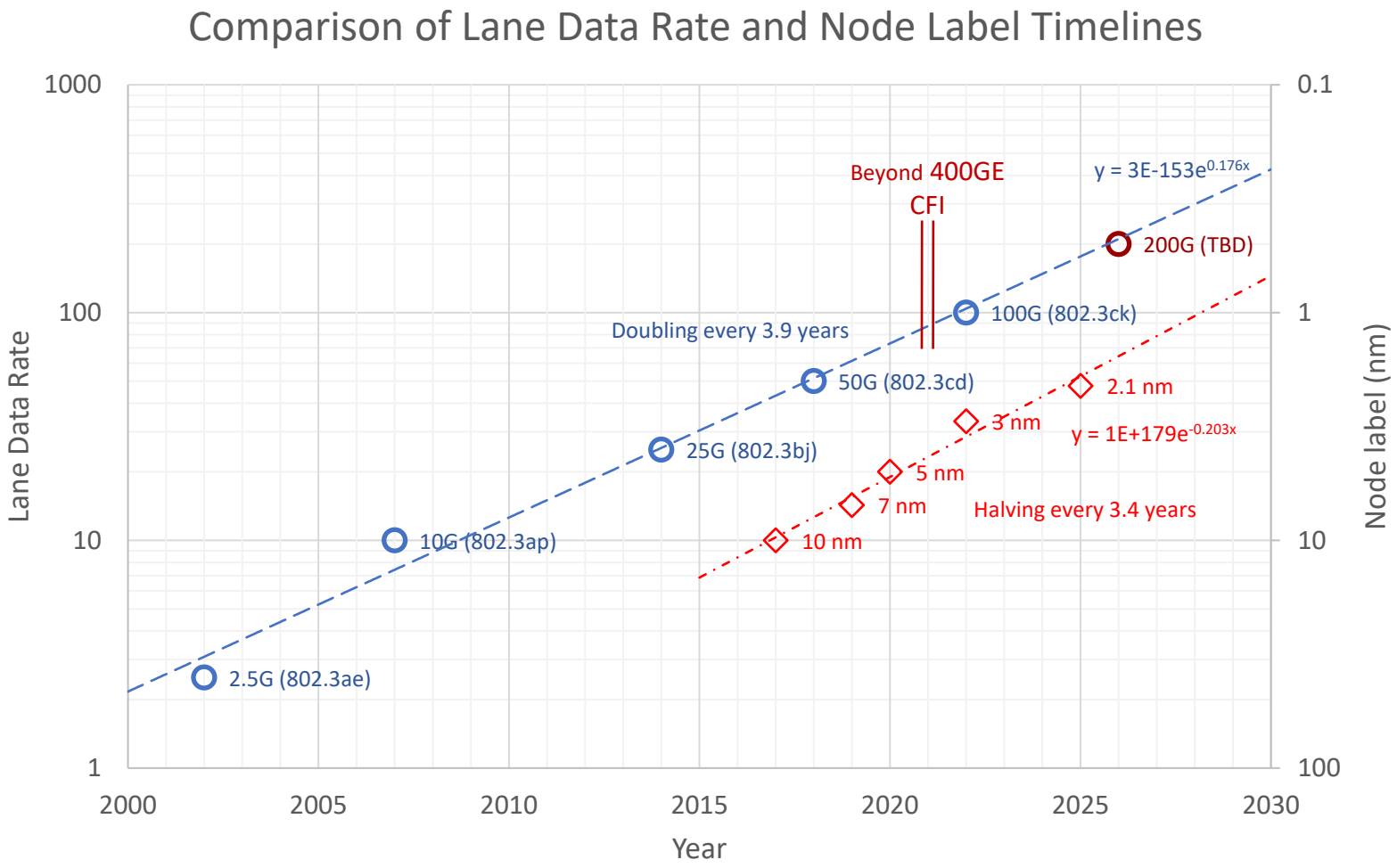
CMOS Roadmap (IRDS 2018)

Table ES2 Overall Roadmap Technology Characteristics

2017 IRDS Executive Summary - ORTC							
YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
Logic device technology naming	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14 T2	P32M14 T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA, 3DVLSI	VGAA, LGAA, 3DVLSI
LOGIC CELL AND FUNCTIONAL FABRIC TARGETS							
Average cell width scaling factor	1.00	0.90	0.90	0.90	0.90	0.90	0.90
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm) [1,2]	18	14	12	10.5	7.0	7.0	7.0
Physical gate length for HP Logic (nm) [3]	20	18	16	14	12	12	12
Lateral GAA (nanosheet) Minimum Width (nm)			7.0	7.0	6.0		
Minimum Device Width (fin, nanosheet) or Diameter (nm)	8	7.0	7.0	7.0	6.0	6.0	6.0
LOGIC DEVICE Electrical							
Vdd (V)	0.75	0.70	0.65	0.65	0.65	0.60	0.55
DRAM TECHNOLOGY							
DRAM ½ Pitch (nm) [1]	18	17.5	17	14	11	8.4	7.7
DRAM cell size factor: aF^2 [11]	6	6	4	4	4	4	4
DRAM bits/1chip target	8G	8G	16G	16G	32G	32G	32G
NAND Flash							
Flash ½ Pitch (nm) (un-contacted Poly)(F) (2D) [1]	15.0	15.0	15.0	15.0	15.0	15.0	15.0
Flash Product Highest Density (independent of 2D or 3D)	512G	1T	1T	1.5T	3T	4T	4T+
Flash 3D Maximum Number of Memory Layers [6]	64	96	128	192	384	512	>512

https://irds.ieee.org/

CMOS technology compared with lane data rate



The upper data (blue) shows evolution of electrical lane data rate over time.

The lower data (red) shows the evolution of node label over time.

Current designs for 100 Gb/s per lane are in 7 nm and are moving to 5 nm.

3 nm and 2.1 nm will be available when 200 Gb/s per lane is standardized.

The node label (halving every 3.4 years) is progressing faster than the electrical lane rate (doubling every 3.9 years).

Conclusion

- CMOS technology is closely tracking electrical lane data rates and should scale appropriately for 200 Gb/s per lane.

Thanks