PAM4 DSP Architecture Advances for Beyond 400GbE

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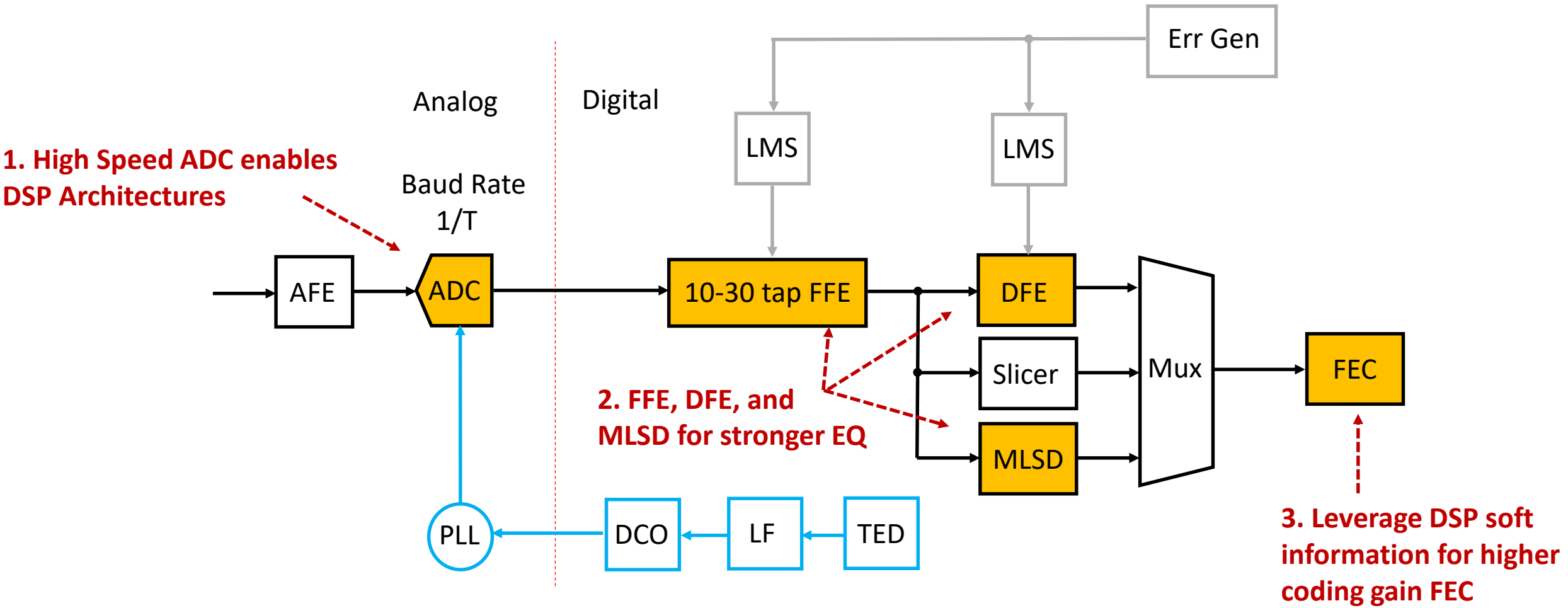
Summary

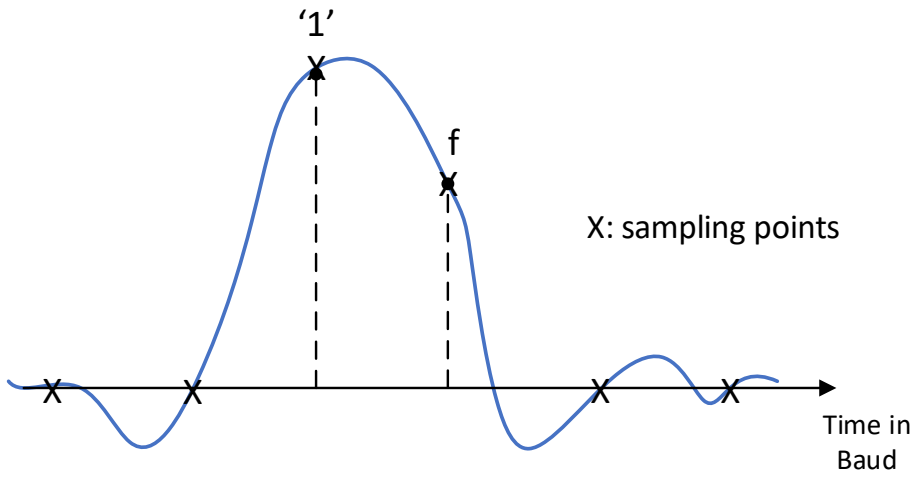
- 100G per Lambda/per Lane PAM4 Rx DSP Architectures
- Identify Potential DSP Building Blocks for Beyond 400GbE
- Low Power MLSD
- Soft FEC for Low Latency Higher Coding Gain
- Conclusions

100G PAM4 Rx DSP Architecture



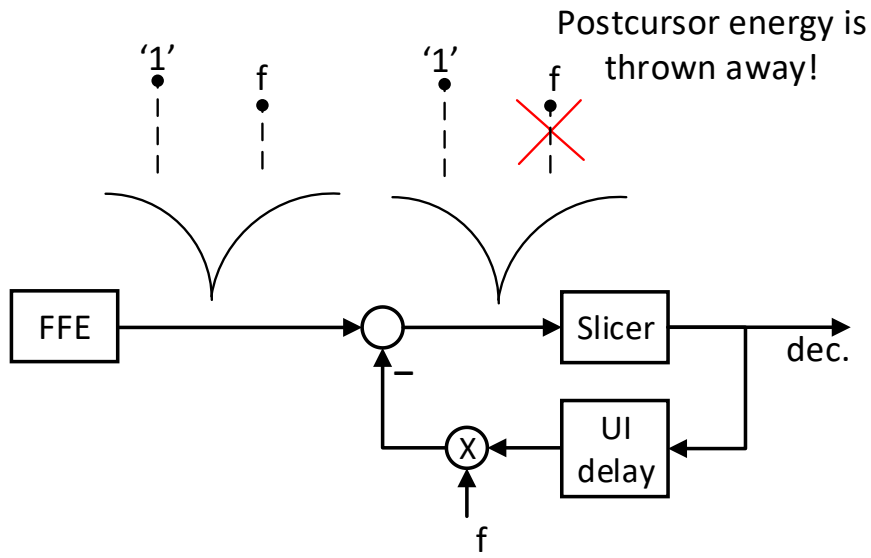
Maximum Likelihood Sequence Detection (MLSD)

- Fully equalizing postcursor tap (f) through the FFE is expensive in terms of noise enhancement →high SNR penalty vs channel IL



- Commonly a DFE is used to handle postcursor ISI:
  - Only channel energy at main tap is used for symbol detection
  - Postcursor energy is thrown away → suboptimal

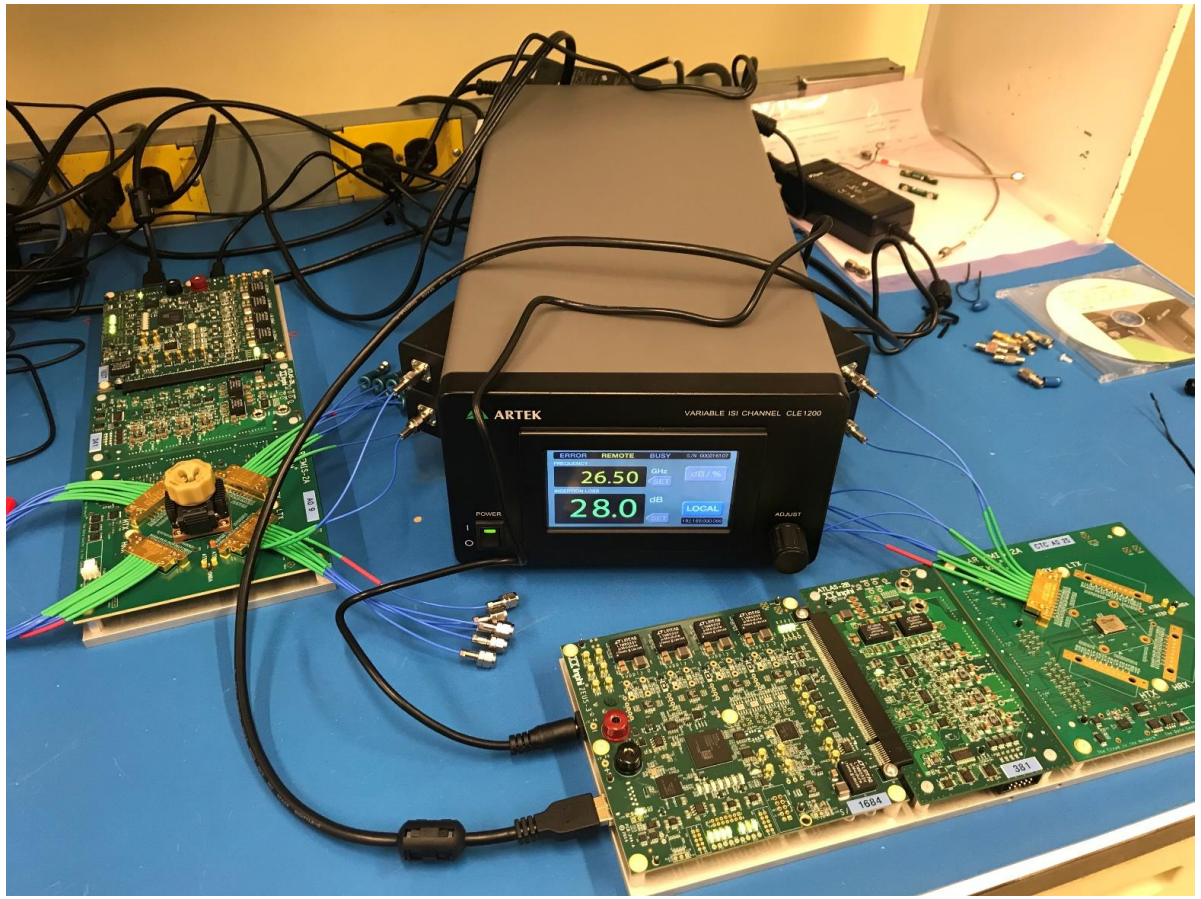
- Optimal detection has to use all signal energy. Both symbol k and symbol k+1 contains directly information on PAM symbol k, through main tap or postcursor tap
  - Such optimal detection is achieved by applying sequence detection seeking to find the Maximum Likelihood sequence



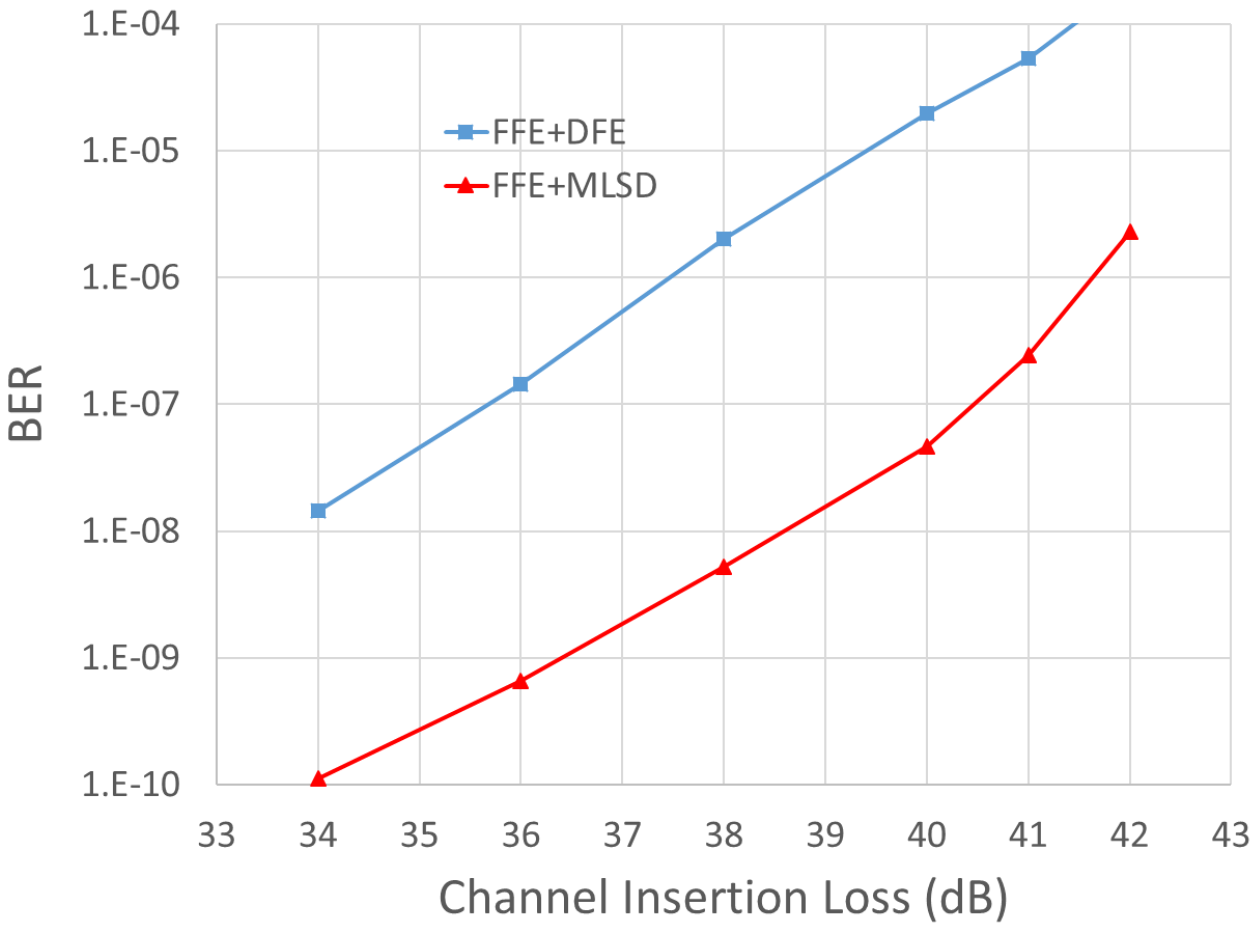
Reference: farhoodfar_3bj_01_0912

Measurement Results for 53Gbaud LR PAM4 SerDes

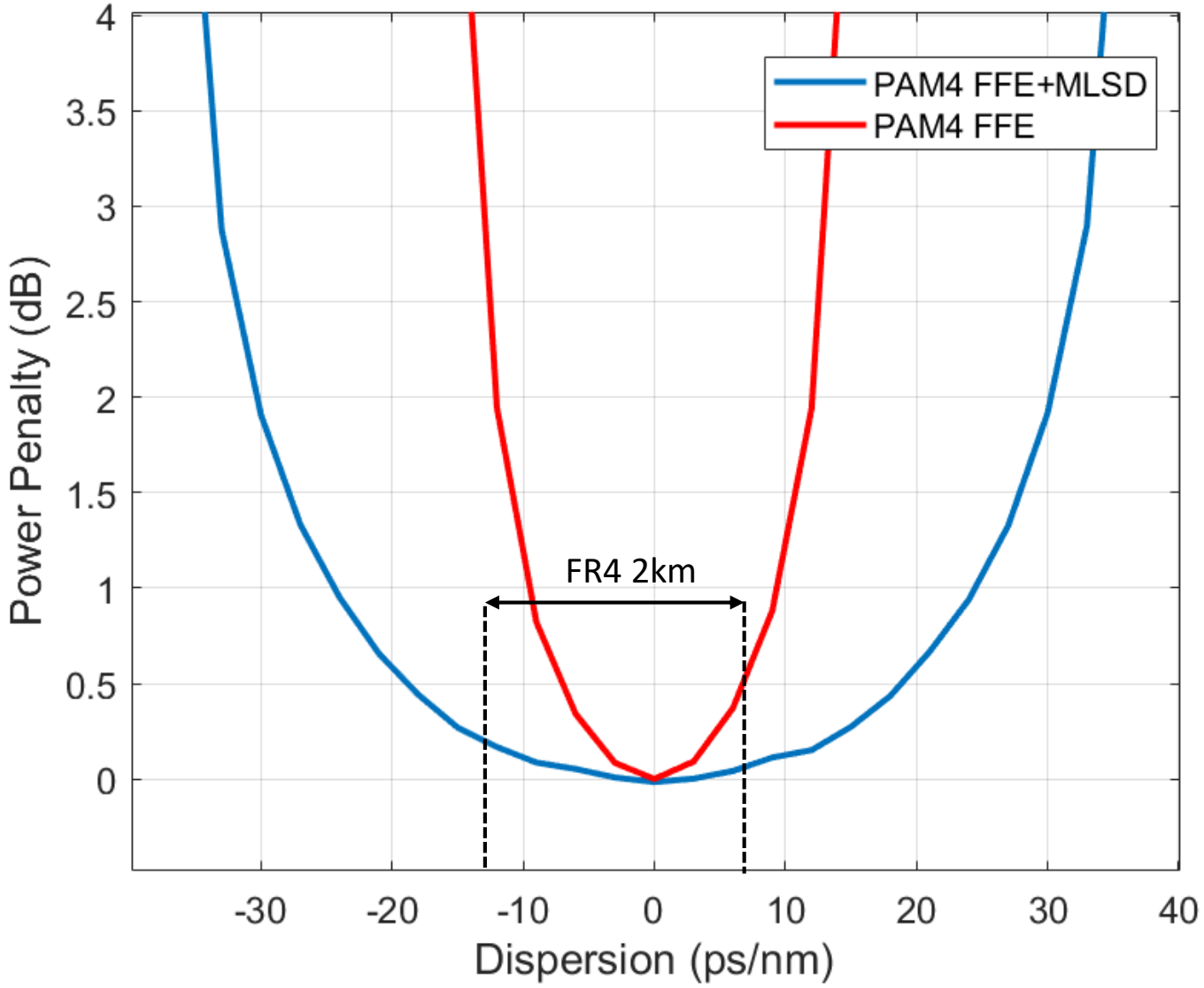
Variable IL measurement setup for 7nm SerDes test chip



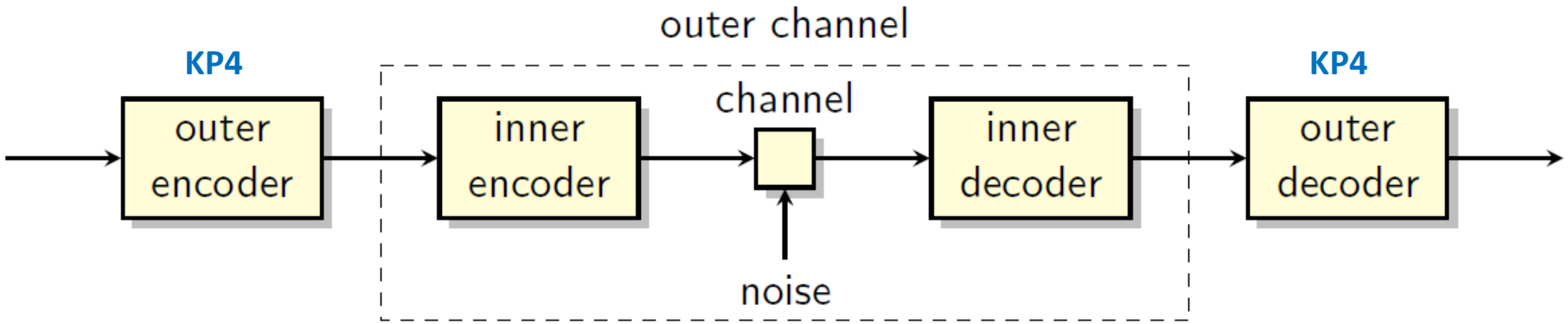
Measured BER vs. Channel IL



200G Dispersion Penalty Simulation Results: Looking Ahead to Beyond 400GbE



Concatenated Codes: ADC Enables Soft Decision Inner Code in the Module DSP

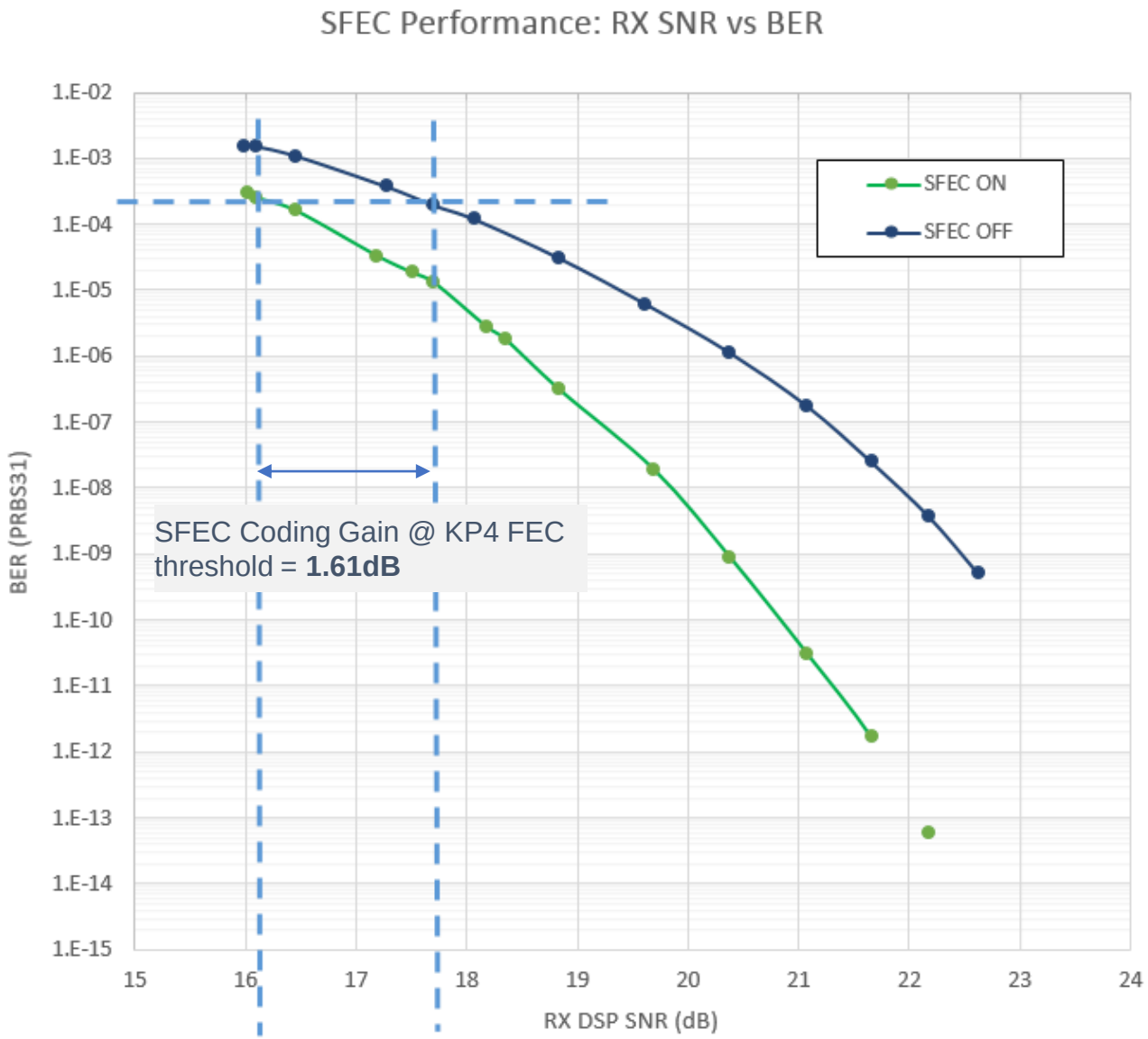


Concatenated codes: use two or more codes in tandem

- **inner code** (code closest to the channel) is well-tuned for the particular channel
- **outer code** "cleans up" the errors left by the inner code
- overall rate $R = R_{\text{inner}} \cdot R_{\text{outer}}$
- often the inner code can perform soft-decision decoding

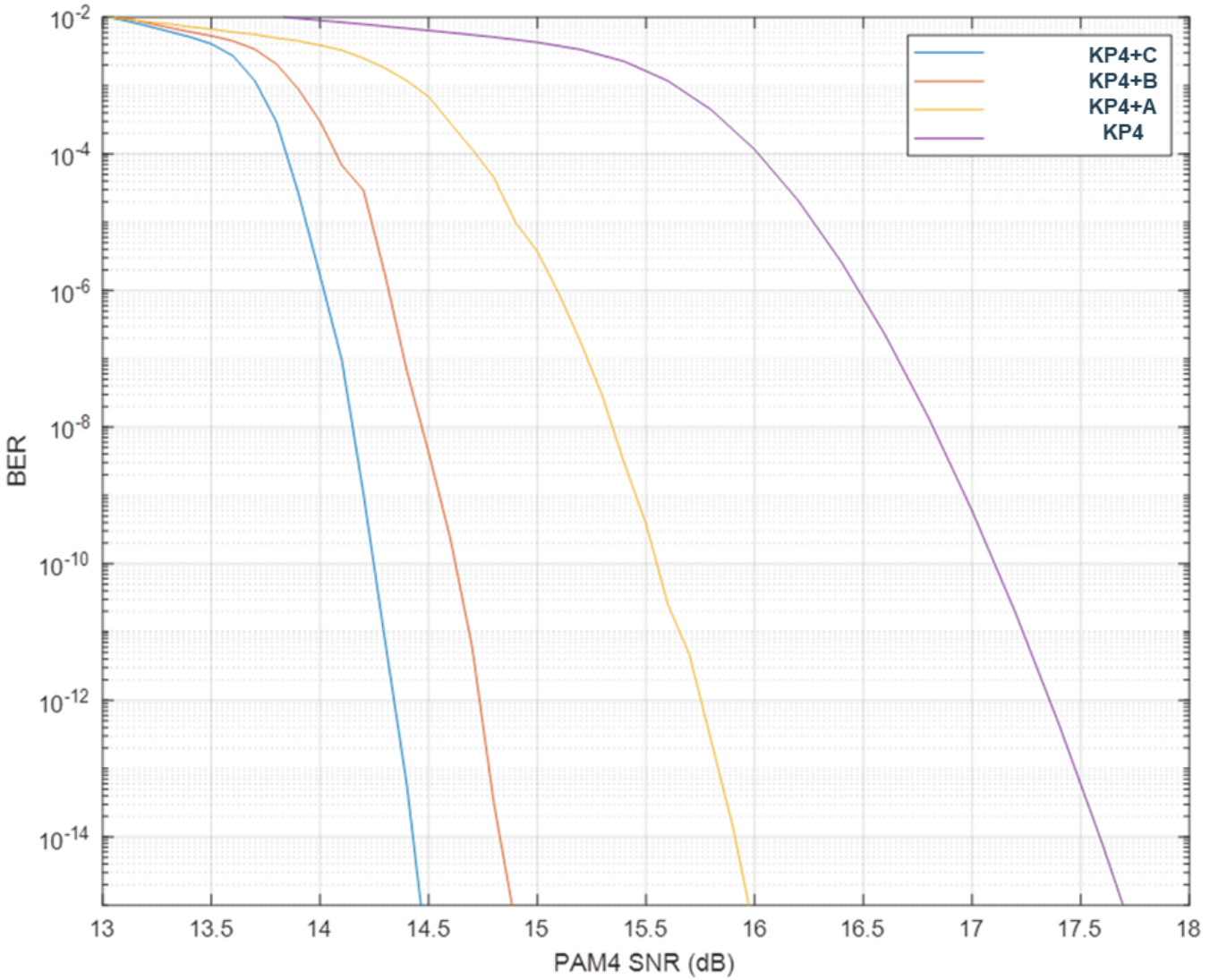
Source: Frank Kschischang, "Introduction to Forward Error Correction,"
OFC Short Course, 2018

Low Complexity/Low Latency Soft Decision FEC (SFEC) Measurement Results



SFEC latency < 1 ns
SFEC power 55-65 mW per 100G lane

Second Generation SFEC Simulation Results



Source: “Next Generation PON and Data Center Interconnect: Exploring Synergies on FEC,” IEEE Summer Topical, July, 2019

Conclusions

- We reviewed PAM4 DSP technology deployed today in 100G per lane electrical SerDes as well as 400G FR4/DR4/LR4 optical modules
- Rx DSP equalization capabilities far exceed the assumptions that went into PAM4 TDECQ reference equalizer; DSP based equalizers can include 10-30 tap FFE, 1-tap DFE, and MLSD
- Advancements in high speed ADC technology also open the way toward low latency higher gain soft decision FEC; such soft decision FECs are already in use for enhancing the reach and/or lowering optical module costs
- Beyond 400GbE project will be able to leverage these DSP advancements