Cl **33** *SC* **2.7** *P* **36** *L* **27** # 127

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *L1 adhoc*

The text:
"If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall assign the PD to Class 0 and a Type 2 PSE shall assign the PD to class 4." imposes an unnecessary design requirement. This text also enables dump-Type 2 PDs that do not support DLL classification.

A system that does not provide a proper class is:
a) Experiencing a temporary fault that will rectify itself.
OR
b) Noncompliant.

A compliant Type-2 PD has not achieved mutual identification and will remain in type-1 power mode. Therefore, requiring class-4 power serves no legitimate purpose.

A PSE that classifies a PD and gets an invalid results is not probable because this occurs only when class current exceeds 51 mA.

SuggestedRemedy

Require PSEs that performs classification, to either repeat the detection and classification steps, or repeat the classification step, until legal responses are achieved.

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **2.7.2a** *P* **37** *L* **52** # 129

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A** *L1 adhoc*

The same settling requirements for Type-1 classification should be imposed on Type-2 first class, classification. A Type 1 PD requires 5 ms to provide a valid class current (table 33-12, item 9). This comment also applies to p38 L24.

SuggestedRemedy

Have the L1 ad hoc review and correct this section.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The editor to apply the same transient settling timing to both 1-event and 2-event classifications. Page 37, line 43.

Cl **33** *SC* **2.7.2a** *P* **38** *L* **35** # 130

Schindler, Fred — Cisco Systems

Comment Type **ER** *Comment Status* **D** *L1 adhoc*

The text:
"… transition to the POWER_ON state without allowing the voltage at the PI to go below Vmark." Conflicts with text at L40: "… shall ensure the PI enters the Vreset range…" because Vmark > Vreset.

SuggestedRemedy

Have the L1 ad hoc provide text to correct this section.

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **2.7.2a** *P* **38** *L* **40** # 102

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *L1 adhoc*

Draft 1.0:

When PSE classify the PD after Icllas_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to adress this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset.

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **2.7.2a** *P* **38** *L* **40** # 83

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *L1 adhoc*

Draft 1.0:
If after Iclass_lim event the PSE classify the PD as class 4, why we need to be in Reset range?
It looks that the text "Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port." is not required.

SuggestedRemedy

Option a:
Classification ad hoc to explain why we need it.
If we don't need it, to delete it.

Option b:
Change the text to read:
"If PSE decides not to complete two event classification due to any reason, or decides to ignor classification results, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **57** *L* **38** # 255

Stanford, Clay — Linear Technology

Comment Type **E** *Comment Status* **D** *L1 adhoc*

Define Mark Event Voltage range. It will make text more clear.

Define Reset Voltage range. It will make text more clear.

Label Reset Threshold Vreset_th to be more consistant.

SuggestedRemedy

Table 33-11a

Item 2: Add "10" to max column.

Item 5: Change Symbol from Vreset to Vreset_th

Add new item 6, Classification Reset Voltage Vreset V 0(V) 2.8(V) See 33.3.4.2.1

Proposed Response *Response Status* **O**

see 256

Cl **33** *SC* **3.4.2** *P* **57** *L* **50** # 111

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **D** *L1 adhoc*

Draft 1.0:
PD don't have to present class 4 for infinite classification attempts.
Id adds thermal burden and costs.
In any case if system has problems it may initiate consecutive startups every Ted which is defined in Table 33-5 item 21.

SuggestedRemedy

To be added after line 50.
"PD may revert to IDLE state if PSE initiate more then 3 consecutive classification attempts within less then Ted as specified in Table 33-5."

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **3.4.2.1** *P* **57** *L* **53** # 256

Stanford, Clay — Linear Technology

Comment Type **E** *Comment Status* **D** *L1 adhoc*

Text will be more clear if we use Vmark range.

SuggestedRemedy

Line 53 IS:

When the voltage at the PI is between VMark min and VMark_th min, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Line 53 SHOULD BE:
When the voltage at the PI is IN THE RANGE OF Vmark, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Proposed Response *Response Status* **O**

see 255