Cl **33** *SC* **2.2** *P* **22** *L* **50** # 151

Pincu, David Microsemi Inc.

Comment Type **TR** *Comment Status* **D** *4P*

The standard should not preclude implementations that are using both alternative A and B due to the following reasons:

a) It is out of scope of the standard to limit implementations.

b) There are products in the market that are already utilizing the 2 x 2P topology.

c) There is a considerably large market for higher power then 25-30W at the PD.

d) we need to support installations where a 4 pair cable supports two PDs where each one of them is connected to a 2P system. This arrangement is allowed by the cabling standards and exists in many locations .The 4 pair cable is connected to two outlets each outlet connected to two pairs and supporting a different PD.The current text precludes using this arrangement .

SuggestedRemedy

Change from:

"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:

"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

a) It is out of scope of the standard to limit implementations. - The job of a standard is to limit implementations to ensure interoperability so limiting implementations is not out of scope for the standard - it IS the only job of the standard.

b) There are products in the market that are already utilizing the 2 x 2P topology. - That is not justification for a standard.

c) There is a considerably large market for higher power then 25-30W at the PD. - Show the market research and report the market size. Let the TF decide what defines a large market.

d) we need to support installations where a 4 pair cable supports two PDs where each one of them is connected to a 2P system. This arrangement is allowed by the cabling standards and exists in many locations .The 4 pair cable is connected to two outlets each outlet connected to two pairs and supporting a different PD.The current text precludes using this arrangement . - It is disallowed by the power section of 802.3 (Clause 33), need to check the validity under the rest of 802.3. I'm pretty sure Geoff always points out that while people do it, it is expressly not allowed under 802.3. Need to verify with Geoff.

Cl **33** *SC* **2.2** *P* **22** *L* **50** # 166

Feldman, Daniel — Microsemi

Comment Type **TR** *Comment Status* **X** *4P*

The text precludes powering a port using alternatives A and B at the same time. This has several problems.
a) Limits implementations that both make sense, create no harm and are already found in the market for both IEEE802.11n and IEEE802.16 applications
b) As seen by products in the market, as long as the power sharing is performed at the load, there is no need to specify anything on the standard, and even IEEE802.3af endspans and midspans can power 4-pairs PD's that requrie up to 26W today.
c) It is an economically feasible solution to reach power levels of 30W to 60W, as shownb in several presentations.
d) It is technically feasible as shown by the same presentations and by the PD's in the field..
e) There is a huge market for higher power then 30W over 2P, including IEEE802.16 Base Stations, Thin Clients, FTTx ONT's and Notebooks.
f) The cost of a 4-pairs solution is so reasonable that there are even IEEE802.11n Access Points in the market today (e.g. Trapeze Networks) that preferred to use 4-pairs for 20W applications, instead of using 2-pairs high current, since the customers infrastructure is preserved and thes e access points can be powered by existing Midsspans and switches.
g) Using 4-pairs can be a way to reduce heat dissipation on the cable for outdoors applciations. 4-pairs in general is greener than 2-pairs, as the power wasted at the cable is much smaller.
h) 4-pairs fully utilizaes the cabling infrastructure, diminishing the chances we will have to create a new task force in another 2-3 years to support more power.

SuggestedRemedy

Change from:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **W**

see 151, 100 - all redundant comments

Cl **33** *SC* **2.2** *P* **8** *L* **50** # 100

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *4P*

The standard should not preclude implementations that are using both alternative A and B due to the following reasons:
a) It is out of scope of the standard to limit implementations.
b) There are no interoperability issues if PD gets power from two 2 pairs power source. It is the load responsibility (PD) to meet the 2P specification for each 2P. Implementation methods are out of scope of the standard.
c) It is economically feasible as shown in numerous presentations
d) It is technically feasible as shown by the same presentations.
e) There are products in the market that already is using the 2 x 2P implementation e.g. High power Midspan that is using 2 x 2P and applications that are using 2P power coming from the Switch and additional power delivered from Midspan.
f) There is huge market for higher power then 30W over 2P.
g) There is no additional cost issue. The $/watt cost is even lower then in 2P system as shown in previous meeting presentations.
h) For outdoor applications, temperature rise issues of the cables when using 60degC cabling system grade can be solved if the same power is delivered over 2 x 2P which is an easy solution for outdoor applications.
i) Users will do it any way to utilize the full capability of the existing infrastructure.
J) In previous meeting switch and PHY vendors wanted the ability to use the same cable which consists of 4 pairs to support two PDs that each one of them is connected to a 2P system. The current text precludes using this feature.

SuggestedRemedy

Change from:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **O**

see 151

Cl **33** *SC* **2.3** *P* **23** *L* **20** # 183

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **D** *sd*

As defined, the same PSE cannot perform all the state machines listed in the figures simultaneously.

SuggestedRemedy

Either:
- Retain the original motivation for the state diagrams, which was to describe the high level behaviour as seen externally, by leaving the classification state as do_classification with the details defined in subsequent sections

OR

- Change the text to reflect the different combinations. Specifically, isert a copy of the table from diab_2_1007.pdf to precede this section and go through the various combinations and state diagrams that have to be implemented

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.3.3** *P* **24** *L* **15** # 226

Law, David — 3Com

Comment Type **TR** *Comment Status* **D** *sd*

Table 33-5, item 5 IInrush defines three different parameters:

[1] The minimum current the PSE shall supply (IInrush min). This is the minimum point at which the PSE can current limit and ensures a PD that is in excess of 180uF will be supplied with a minimum 400mA - the maximum a PD is allowed to draw (see 33-12, item 3, IInrush max)
[2] The maximum current the PSE is permitted to supply (IInrush max). This is the maximum value at which the PSE is permitted to supply and therefore is the maximum point at which a PSE must current limit when connected to a PD that is less than 180uF and therefore does not current limit.
[3] The range in between which a threshold has to be selected to define the threshold at which the timer ILIM runs (see Figure 33-7, I > IInrush). If this condition exists for more than 50 to 75ms the power has to be removed.

It is therefore permissible to set the current limit at 410mA as it is between the ranges set by [1] and [2] above yet set the TLIM threshold at 420mA. TLIM would therefore never trigger. In a sensible implementation one threshold will be selected and when current limiting TLIM will be running but there is nothing that requires this.

In addition subclause 33.2.3.3 defines constants but IInrush is a range, the constant in the IInrush threshold selected from that range.

SuggestedRemedy

[1] Change 'IInrush' to 'IInrush_threshold' in figure 33-7 and subclause 33.2.3.3.

[2] Change 'Current during inrush period of startup (see Table 33–5)' to read 'Startup inrush current limit (see Table 33–5)'.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.3.4** *P* **24** *L* **19** # 96

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *sd*

Draft 1.0:

We had allowed the PSE to turn power off if Vport is out of operating range per 33.2.8.1.
Therefore the state diagram in figures 33-6 and 33-7a should reflect is as well.

The way to do it is to create new variable which will be optional.
When the conditions of this variable are met, the PSE will remove power at any t<TLIM_MIN.

SuggestedRemedy

Remedy steps:
1) Add new variable option_vport_lim to 33.2.3.4. It will be an optional variable:

"option_vport_lim
This variable is indicating If PSE port voltage is out of operating range during normal operating mode.
Values:
False: Vport is within the Vport normal operating range as defined by table 33-5.
True: Vport is above or below normal Vport operating range as defined by table 33-5."

2) Change state diagram (figure 33-6 and 33-7a) per the attached drawing by changing the inputs to ERROR_DELAY_SHORT state coming from POWER_ON state, from:
tlim_timer_done

to:
Tlim_timer_done + !tlim_timer_done*option_vport_lim*power_applied)

Effect on legacy equipment: None since the variable is optional.

Proposed Response *Response Status* **W**

state diagram bucket

Cl **33** *SC* **2.3.4** *P* **24** *L* **20** # 184

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **D** *sd*

Please remove the dll_comm_established from this state machine. This should be taken care of by the classification sections. The physical layer classification simply have to initiate the ednvironment for the DLL to start. Behaviour once the DLL starts can then be defined in the DLL machine.

SuggestedRemedy

Please remove the dll_comm_established from this state machine. The functionality associated with this can be addressed by the classification sections as we did in 802.3-2005.

Proposed Response *Response Status* **W**

state diagram bucket

Cl **33** *SC* **2.3.4** *P* **25** *L* **30** # 238

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *sd*

Variable pse_available_power needs to be expanded to cover both Type 1 and Type 2 PSEs.

Follow style of page 27, line 35, creating pse_available_power2.

SuggestedRemedy

Add new variable pse_availablepower2

pse_available_power2
This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.
Values: 0: Class 1
1: Class 2
2: Class 0, Class 3
3: Class 4

SHOULD BE:

Proposed Response *Response Status* **W**

state diagram bucket

Cl **33** *SC* **2.3.4** *P* **25** *L* **45** # 239

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *sd*

I think variable pse_skips_event3 can be deleted.

SuggestedRemedy

Delete pse_skips_event3 variable and description.

Proposed Response *Response Status* **W**

state diagram bucket

Cl **33** *SC* **2.3.7** *P* **30** *L* **1** # 241

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *sd*

I submit redlines the the state diagrams.

SuggestedRemedy

Implement redlines.

Proposed Response *Response Status* **W**

state diagram bucket

comment editor did not receive redlines drawings.

Cl **33** *SC* **2.5** *P* **33** *L* **5** # 13

LANDRY, MATTHEW SILICON LABS

Comment Type **TR** *Comment Status* **D** *baseline*

A PSE performing detection should be able to provide two characteristics.

(1) Probing into a short circuit won't destroy the PSE or the source of the short.

(2) Two PSEs probing the same link segment should not result in a 25kohm differential impedance.

The probing voltage (Vvalid and Voc) and short circuit current limit defined in Table 33-2 accomplish (1). A simple shall statement can accomplish (2).

Instead we have some schematics (Figs 33-8 and 33-9) and a normative statement requiring conformance to them. This sure sounds like mandating an implementation -- and unnecessarily at that.

SuggestedRemedy

Strike Figs 33-8 and 33-9 or add a NOTE mentioning that they are informative only.

Strike Thevenin shall statement on line 45.

Add the following shall: A PSE shall present a non-valid signature as defined in Table 33-9 in all detection states.

Note that current PSEs conforming to the Thevenin circuits currently mandated will still satisfy this new shall.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.5.1** *P* **33** *L* **51** # 124

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *baseline*

The existing section on PD detection requires specific design requirements that are not necessary to ensure interoperability. Other detection methods have been disclosed: http://www.ieee802.org/3/poep_study/public/sep05/naegeli_1_0905.pdf
The IEEE specification should ensure requirements for interoperability are in place.

This comment also affects text in section 33.3.3, p54, L18.

SuggestedRemedy

Reference the PD model shown in figure 33-10, and require that the PSE detect values of Rpd_d for all permissible values of Cpd_d as specified in table 33-2.

Remove the text requiring two values but continue to provide guidance for designs that use the two probe method.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7** *P* **36** *L* **27** # 127

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *L1 adhoc*

The text:
"If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall assign the PD to Class 0 and a Type 2 PSE shall assign the PD to class 4." imposes an unnecessary design requirement. This text also enables dump-Type 2 PDs that do not support DLL classification.

A system that does not provide a proper class is:
a) Experiencing a temporary fault that will rectify itself.
OR
b) Noncompliant.

A compliant Type-2 PD has not achieved mutual identification and will remain in type-1 power mode. Therefore, requiring class-4 power serves no legitimate purpose.

A PSE that classifies a PD and gets an invalid results is not probable because this occurs only when class current exceeds 51 mA.

SuggestedRemedy

Require PSEs that performs classification, to either repeat the detection and classification steps, or repeat the classification step, until legal responses are achieved.

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **2.7.2a** *P* **38** *L* **35** # 130

Schindler, Fred — Cisco Systems

Comment Type **ER** *Comment Status* **D** *L1 adhoc*

The text:
"… transition to the POWER_ON state without allowing the voltage at the PI to go below Vmark." Conflicts with text at L40: "… shall ensure the PI enters the Vreset range…" because Vmark > Vreset.

SuggestedRemedy

Have the L1 ad hoc provide text to correct this section.

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **2.7.2a** *P* **38** *L* **40** # 102

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *L1 adhoc*

Draft 1.0:

When PSE classify the PD after Icllas_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to adress this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset.

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **2.7.2a** *P* **38** *L* **40** # 83

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *L1 adhoc*

Draft 1.0:
If after Iclass_lim event the PSE classify the PD as class 4, why we need to be in Reset range?
It looks that the text "Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port." is not required.

SuggestedRemedy

Option a:
Classification ad hoc to explain why we need it.
If we don't need it, to delete it.

Option b:
Change the text to read:
"If PSE decides not to complete two event classification due to any reason, or decides to ignor classification results, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **38** *L* **48** # 173

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **D** *editorial*

As per comments 225 and 161, this text needs to be restructured so that we can write PICs around it. The way it stands, it says you shall implement this and you may then omit. This is hard to write text around. I believe that the editor is trying to describe a state machine.

SuggestedRemedy

Please replace this paragraph with a state machine

Proposed Response *Response Status* **O**

also see 196, 272

Cl **33** *SC* **2.8** *P* **40** *L* **23** # 134

Schindler, Fred — Cisco Systems

Comment Type **E** *Comment Status* **D** *editorial*

Consider using "k" or something other than "V" to convey that a constant is being used.

SuggestedRemedy

Suggest using "KTran_lo."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8** *P* **40** *L* **35** # 81

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Iport_max is shown with the value Icable as a MINIMUM required maximum port current. However, Icable is defined as 720 mA in 33.1.4, and 720 mA is the very top of the allowed current range in Figure 33-9a (formerly SOA curve). So it doesn't seem logical that Icable can be a MINIMUM value for anything including Iport_max for Type 2 PSE's.

SuggestedRemedy

Icable needs to be clearly defined as EITHER the maximum continous current (Iport) that can ever exist on a single pair OR if it is to be equated with 803.3af value of Iport_max (MIN) (=350 mA), then it cannot be considered the maximum continous current allowed on a pair as implied by Figure 33-9a.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8** *P* **40** *L* **4** # 131

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *editorial*

Combine the two sentences added so that the required intent is conveyed within one sentence.

SuggestedRemedy

Use the sentence: "When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the electrical requirements of a Type 1 PSE, and may choose to meet the electrical requirements of a Type 2 PSE for table 33-5 items 4, 8, and 10."

Proposed Response *Response Status* **O**

This is an editorial comment. Technically, what changes from the edit? Propose to accept…

Cl **33** *SC* **2.8** *P* **41** *L* **7** # 9

LANDRY, MATTHEW — SILICON LABS

Comment Type **T** *Comment Status* **D** *Vport adhoc*

ICUT is optional. ICUT min should be the maximum current the PD can draw at a given port voltage (PClass/VPort). It is.

To maintain the use of the TCUT timer, the maximum ICUT should be less than or equal to the current limit. This is almost true for Type 1. We have a TBD for Type 2.

We need to specify an ICUT max that meets the criteria above.

SuggestedRemedy

Change ICUT max to ILIM.

This will open up the ICUT space a little wider for Type 1 PSEs (e.g. if ILIM is 425mA, then ICUT could be 424mA), but will also properly let the SOA curve guide ICUT for all future PSEs.

Note that it does not break compliance of current PSEs, and still supports both current limited and energy limited PSEs.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.1** *P* **41** *L* **52** # 246

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The statement:

"A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the VPort specification"

is very broad and doesn't reflect the intent. Add text to clarify.

SuggestedRemedy

IS:
A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the VPort specification.

SHOULD BE: (CAPS INDICATE ADDITION)
A PSE in the POWER_ON state may remove power from the PI IF THE PI voltage no longer meets the VPort specification DUE TO EXCESSIVE PORT LOADING FROM A NON-COMPLIANT PD OR PORT FAULT CONDITION.

Proposed Response *Response Status* **O**

what is allowed by the present text that we want to prevent? Lacking specific examples, I'm inclined to reject.

Cl **33** *SC* **2.8.14** *P* **45** *L* **41** # 5

LANDRY, MATTHEW — SILICON LABS

Comment Type **E** *Comment Status* **D** *editorial*

Is this a proper use of the 'CAUTION' statement?

SuggestedRemedy

If not, change it to a NOTE.

Proposed Response *Response Status* **O**

see 29

Cl **33** *SC* **2.8.2a** *P* **42** *L* **12** # 132

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The PD is restricted to a current slew rate of 15 mA/us maximum. A single PSE port can provide a 35 mA/us demand rate but multiple ports transitioning at this rate may be unrealistic.

SuggestedRemedy

Change PSE requirements in this section of "35 mA/us max." to "at least 15 mA/us."

Proposed Response *Response Status* **O**

defer to vport

Cl **33** *SC* **2.8.2a** *P* **42** *L* **17** # 135

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *editorial*

The sentence structure does not convey the intent for PSE transient behavior and what action to take when a short circuit condition exists.

SuggestedRemedy

Modify the existing sentence to: "A Type 2 PSE shall maintain an output voltage of no less than VTran_lo below Vport min for transient conditions lasting more than 30 uS and less than 250 us, and meet the requirements of section 33.2.8.8.

Proposed Response *Response Status* **O**

comment recommends adding this:

"and meet the requirements of section 33.2.8.8"

to the end of the existing sentence.

See 247

Cl **33** *SC* **2.8.2B** *P* **42** *L* **17** # 247

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Paragraph could be written more clearly to better express intent.

SuggestedRemedy

IS:
A Type 2 PSE shall maintain an output voltage no less than VTran_lo below VPort min for transient conditions lasting more than 30us and less than 250us.

Transients less than 30us in duration may cause the voltage at the PI to fall more than VTran_lo . The minimum PD input capacitance ensures the PD will operate for any input voltage transient lasting less than 30us. Transients lasting more than 250us shall meet the static VPort specification.

SHOULD BE:

Brief decaying voltage transients less than 30us in duration should not effect PD operation due to storage capacity present in the PD and as such are not limited.

For decaying voltage transients lasting 30 to 250us, a Type 2 PSE shall maintain an output voltage no less that VTran_low bleow Vport_min.

Transients lasting more than 250us shall meet the static VPort specification.

Proposed Response *Response Status* **O**

see 135

Cl **33** *SC* **2.8.4** *P* **42** *L* **35** # 137

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The value for Ipeak is incorrect.

SuggestedRemedy

The correct value for Ipeak = (Vpse - SQRT(Vpse^2 - 4RchPpd_port_peak))/(2Rch).
More details can be found in a presentation that will be provided during the Atlanta Plenary meeting.

Proposed Response *Response Status* **W**

defer to Vport adhoc
see 114

Cl **33** *SC* **2.8.4** *P* **42** *L* **38** # 227

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Please provide definitions for the variables used in this equation.

SuggestedRemedy

Suggest that this text be changed to read:

The PSE shall support an AC current of Ipeak minimum for 50 ms minimum and 5 % duty cycle minimum.

Ipeak = (400 / 350) × (PPort / VPort)

Where:

IPeak is the peak output current.
PPort is the minimum continuous output power (see Table 33-5, item 14).
VPort is the minimum static output voltage (see Table 33-5, item 1).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.
NOTE: Yair has comment that could remove this section.

Defer to Vport adhoc

Cl **33** *SC* **2.8.4** *P* **42** *L* **38** # 80

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **D** *Vport adhoc*

It is no longer clear that 33.2.8.4 requires Vport to fall into the valid Vport range during a transient load condition (Ipeak). Without this clarification, 3.2.8.4 could come into conflict with 33.2.8.1 which allows power to be removed when Vport drops below Vport_Min. Additionally, there is nothing in 33.2.8.2 (Vport Regulation) that assures a valid Vport level given Ipeak as defined in 33.2.8.4. Additionally, "transient current waveforms" or "peak current waveforms" may be a better term than "AC current waveforms" in line 38 since "AC" in the spec is generally associated with MPS technique rather than overload currents.

SuggestedRemedy

One solution: Title 3.2.8.4

PSE maximum continuous and peak output current in normal powering mode at or above minimum output voltage

Separately modify line 38 to use "...peak current waveform..."

Proposed Response *Response Status* **O**

defer to vport

Cl **33** *SC* **2.8.4** *P* **42** *L* **38** # 114

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

1. The editor was not authorized to make the changes in this clause due to the fact that the remedy suggested by the ad-hoc was not concluded and adopted.

2. In addition, the new text makes legacy PSE non compliant due to the fact that the peak power for type PSE is not function of (Pport/Vport)*(0.4/0.35) for class 1 and 2. It is correct only for class 0,3.

3. The peak current is already defined in Table 33-12 item 12 (Ed note: Item 4) and we don't need to define it again for the PSE due to the simple physical fact the PSE output current is equal to the PD input current..

SuggestedRemedy

Option 1: (Not recommended)
Restore the old text.

Option 2: (Recommended)

Replace the text in line 38 from:
"The PSE shall support the following AC current waveform parameters:
Ipeak = (400 / 350) ª (PPort / VPort) minimum for 50 ms minimum and 5 % duty cycle minimum."

To:
"The PSE shall support the following the maximum peak current as defined by Table 33-12 item 4 for 50 ms minimum and 5 % duty cycle minimum."

Note to the group:
1. The peak current already defined in table 33-12 item 4. No need to repeat it again.
2. The peak current numbers should be defined in one place i.e. in the PD side due to the fact that it is defined by the load and the PSE has only to support it.
3. The peak current with option b remedy is function of (0.4/0.35)*Port/Vport only for Type 2 PD due to the fact that we don't have to take in account previous legacy definitions.
For type 1 class 1 and 2 PDs, the constant power model contains some margin from reasons that was explained in my presentation (that was not presented yet) which is located at the web site of the October 2007 meeting).
3. For class 0,3 the peak current is a constant and not a function of Vport.
(The average current was described as a function of Pport/Vport.)
Taking all this data in account, leads to the suggested remedy of option b.

Proposed Response *Response Status* **W**

defer to Vport Adhoc
see 137

Cl **33** *SC* **2.8.4** *P* **42** *L* **39** # 79

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The formula as written is confusing and should be corrected to avoid breaking 802.3af specification where any PD is allowed to draw 400 mA for 50 msec.

SuggestedRemedy

Ipeak = (400 / 350) x (Port / Vport_Min) for 50 msec minimum and 5% duty cycle minimum.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Defer to Vport adhoc
The remedy recomends changing Vport to Vport_min in the formula.

Cl **33** *SC* **2.8.5** *P* **43** *L* **16** # 104

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **D** *annex*

Draft 1.0:
In many ocasions the normative text send the reader to see figures 33C.4 and 33C.6 which contains valuble data.
These drawings should be at the normative text as it was in early drafts of 802.3af and were moved to the informative section due to editing considerations.

SuggestedRemedy

Move figures 33C.4 and 33C.6 (after updating them per my previous comment) to the normative section at the location where they are mentioned for the first time.

Proposed Response *Response Status* **O**

opposite comment of Fred 138 which asks to delete reference to these figures

Cl **33** *SC* **2.8.5** *P* **43** *L* **23** # 136

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *editorial*

The text: "In a PSE that supports a classification function … may optionally be" provides a formula for ICUT. This ICUT formula is valid whether classification is performed or not.

SuggestedRemedy

Replace this text with: "In a PSE, the minimum value of ICUT may optionally be"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.6** *P* **43** *L* **30** # 56

Vetteth, Anoop Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

the denominator of the equation should be Vport and not Vportmin. The minimum value of Icut should be equal to the value of Iport_max as defined in 33.2.8.4

SuggestedRemedy

Change the denominator of the equation to Vport

Proposed Response *Response Status* **O**

defer to Vport

Cl **33** *SC* **2.8.6** *P* **43** *L* **31** # 249

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Icut is being re-defined to allow current to be limited to PD power rating.

In equation, I think the intent is for the PSE to use the actual port voltage to calculate the allowed current.

Therefore, Vport_min should be Vport-operation, or Vport-actual.

SuggestedRemedy

Proposed Response *Response Status* **O**

see 56

Cl **33** *SC* **2.8.8** *P* **44** *L* **5** # 138

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **D** *annex*

The reference to "Figure 33C.4 and Figure 33C.6" are no longer correct. The information provided in Figure 33-9a supersedes them.

SuggestedRemedy

Remove reference to "Figure 33C.4 and Figure 33C.6."

Proposed Response *Response Status* **O**

opposite comment of Yair 104 which asks to pull these into the normative text.

Cl **33** *SC* **2.9** *P* **45** *L* **51** # 140

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **D** *editorial*

The text, "The PSE may manage …. the attached PD.", removed from the legacy standard is still valid.

SuggestedRemedy

Restore the text.

Proposed Response *Response Status* **O**

this is baseline text we pulled out after D0.9. comment 148 from D0.9 struck it.
D0.9 Comment 148:
The text states that '.. and the mechanism for obtaining that additional information, is beyond the scope of this standard ..'. I do not believe that is true anymore due to the link layer classification protocol.
Remedy:
Reword to acknoledge link layer classification.
Response:
ACCEPT IN PRINCIPLE.

Delete 2nd paragraph of 33.2.9

not much help here…

Cl **33** *SC* **3.1** *P* **49** *L* **41** # 115

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *4P*

Draft 1.0:

The note in line 42 precludes the following applications:
1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD.

2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or power application.

The standard should not preclude implementations that are using standard compliant 2P system.

Theoretically a PD can get N x 2P power sources while each of the 2P system is well defined by the standard and the standard should not preclude it since it is implementation issue and it is not a source of interoperability issues.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:
"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode are not precluded by this standard as long as the requirements of this standard are kept for each mode."

Other equivalent wording is possible.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This comment is word for word identical to 152 - handle it there.
Turning in multiple comments that are TEXTUALLY IDENTICAL accomplishes nothing, in fact it wastes my valuable time. It does not make the issue appear more important nor do I think it fools the TF into thinking that more people want a specific feature.
I volunteer to do this job not because I enjoy it. I want to see this standard finish up in a decent amount of time and a comment editor helps push that recircs out faster. Please respect my time and resist ganging up on comments.

Cl **33** *SC* **3.1** *P* **49** *L* **41** # 152

Pincu, David — Microsemi Inc.

Comment Type **TR** *Comment Status* **D** *4P*

The note in line 42 precludes the following applications:

1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD.

2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or higher power application.

The standard should not preclude implementations that are using standard compliant cabling systems.

Theoretically a PD can get N x 2P power sources while each of the 2P system is well defined by the standard and the standard should not preclude it since it is implementation issue and it is not a source of interoperability issues.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode are not precluded by this standard as long as the requirements of this standard are kept for each mode."

Other equivalent wording is possible.

Proposed Response *Response Status* **O**

"1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD."

This is a job for Geoff.

"2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or higher power application. The standard should not preclude implementations that are using standard compliant cabling systems. "

The job of a standard is to preclude implementations to ensure interoperability. In this case, there is a huge interoperability issue (not to mention a stringent design requirement) on the PD to accept power at disparate voltages from the two different 2P systems. As a PD designer, I want no part of the added cost and complexity from enabling this. I also don't believe that interoerability has been proven.
This issue has been popping up repeatedly in each draft. I suggest we make a motion and vote so we can resolve this and move on toward TF draft.

Cl **33** *SC* **3.1** *P* **49** *L* **42** # 91

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *4P*

The standard allow using for each pair up to Icable.
This Note prevents using all 4 pairs in a way that the total current will be Icable.
The end result would be less power on the cables, less power consumption on PSE.
If Icable meet the spec. of 2P then I<Icable certaily meets the same specification so preventing feeding the current all over the 4 pairs doesnt make sense.
This is implementation and we are not authrized to preclude implementations that meet the numbers and state machines of this standard.

SuggestedRemedy

Delete:
"PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

Proposed Response *Response Status* **O**

As stated many times already, standards are exactly about limiting implementations to ensure interoperability. See 151 or 100 or 166 or 156 for my diatribe against this argument. As for changing the text, I suggest we put up a motion and vote on it then accept the result and move forward.

Cl **33** *SC* **3.1a** *P* **50** *L* **5** # 199

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **D** *editorial*

This section does not accurately reflect the decisions we made in October. Specifically, it mandates that a Type PD implement classification, which breaks 802.3-2005. Moreover, it rules out certain combinations that the table in diab_2_1007.pdf allows, like classifying a Type 2 PD using one event classification and DLL.

It is very difficult to retain this wording here as it is without getting into classification.

SuggestedRemedy

Rewrite this section as follows:

PDs can be categorized as either Type 1 or Type 2 (refer to 1.4). PDs may also implement Physical Layer Classification and/or Data Link Layer Classification. Permutations allowed by the standard are covered in section 33.3.4.

A Type 2 PD is required to achieve mutual identification with a Type 2 PSE as described in section 33.4. A Type 2 PD that does not achieve mutual identification shall conform to Type 1 PD power restrictions. Such a PD shall provide the user with local external notification that it is underpowered. The external notification mechanism is left to the implementor.

Proposed Response *Response Status* **O**

The new text is missing the shall that mandates the Type 2 PD to implement 2-event and DLL. For sure this is still a requirement. 202 points to 33.3.4 - the shalls are there. Maybe this text needs to have all shalls removed and be informative.

Cl **33** *SC* **3.2.3** *P* **52** *L* **12** # 251

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *sd*

An entry was lost in the state diagram by error. It was in the .af spec.

SuggestedRemedy

Add to REQUESTING_POWER BLOCK

present_pd_siganture <= TRUE

Proposed Response *Response Status* **O**

This block is a holder for Figure 33-12a. Concievably this block could be deleted and replaced with 33-12a in which place your requested text would not exist.

Cl **33** *SC* **3.2.3** *P* **52** *L* **15** # 200

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **D** *sd*

Is there a priority issue with the exit conditions out of the REQUESTING_POWER state? Specifically, what happens if both exit conditions are asserted simultaneously?

SuggestedRemedy

There are 2 variables that govern the exit conditions in this state. This has 4 combinations. Please either draw in all 4 arrows OR show what happens if both variables are asserted

Proposed Response *Response Status* **O**

for sure the state diagrams still need work. Which one takes priority?

Cl **33** *SC* **3.2.3** *P* **53** *L* **4** # 252

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *sd*

See Clay's redlines regarding state diagram.

SuggestedRemedy

Update state diagram.

Proposed Response *Response Status* **O**

awaiting redline drawings.

Cl **33** *SC* **3.3** *P* **54** *L* **23** # 253

Stanford, Clay Linear Technology

Comment Type **E** *Comment Status* **D** *editorial*

The parameter name was changed from VI to slope.

Table 33-8 still uses V-I slope.

Pick a consistent name.

SuggestedRemedy

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4** *P* **56** *L* **2** # 168

Diab, Wael Broadcom

Comment Type **T** *Comment Status* **D** *editorial*

Please insert a copy of the Table and associated text from diab_2_1007.pdf in this section with introductory text, prior to the text present as the table covers both PSE and PD implementations.

SuggestedRemedy

Please insert a copy of the Table and associated text from diab_2_1007.pdf at the begining of this section with the following introductory text:

"An 802.3at PD implementing classification shall meet one of the permutaiuons lsted in Table 33-2a"

Proposed Response *Response Status* **O**

set to T by CE.

Cl **33** *SC* **3.4.1** *P* **56** *L* **32** # 12

LANDRY, MATTHEW SILICON LABS

Comment Type **T** *Comment Status* **D** *baseline*

The Usage column in Table 33-10 adds no value.

SuggestedRemedy

Remove it.

Proposed Response *Response Status* **O**

see 141, wants to modify rightmost column

Cl **33** *SC* **3.4.1** *P* **56** *L* **34** # 141

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *baseline*

Table 33-10 is not clear. Why is a range of maximum stated? Maximum is a single value per class. Some people assume the lower bound is a minimum power requirement and this is incorrect. The minimum power required to maintain PSE powering is covered in 33.3.6.

SuggestedRemedy

Only state the maximum class power allowed. Replace the third column with:
Maximum power used by the PD (W)
12.95
3.84
6.49
12.95
TBD

Proposed Response *Response Status* **O**

see 12, wants to remove usage column

Cl **33** *SC* **3.4.2** *P* **57** *L* **38** # 255

Stanford, Clay — Linear Technology

Comment Type **E** *Comment Status* **D** *L1 adhoc*

Define Mark Event Voltage range. It will make text more clear.

Define Reset Voltage range. It will make text more clear.

Label Reset Threshold Vreset_th to be more consistant.

SuggestedRemedy

Table 33-11a

Item 2: Add "10" to max column.

Item 5: Change Symbol from Vreset to Vreset_th

Add new item 6, Classification Reset Voltage Vreset V 0(V) 2.8(V) See 33.3.4.2.1

Proposed Response *Response Status* **O**

see 256

Cl **33** *SC* **3.4.2** *P* **57** *L* **50** # 111

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **D** *L1 adhoc*

Draft 1.0:
PD don't have to present class 4 for infinite classification attempts.
Id adds thermal burden and costs.
In any case if system has problems it may initiate consecutive startups every Ted which is defined in Table 33-5 item 21.

SuggestedRemedy

To be added after line 50.
"PD may revert to IDLE state if PSE initiate more then 3 consecutive classification attempts within less then Ted as specified in Table 33-5."

Proposed Response *Response Status* **O**

defer to L1

Cl **33** *SC* **3.4.2.1** *P* **57** *L* **53** # 256

Stanford, Clay — Linear Technology

Comment Type **E** *Comment Status* **D** *L1 adhoc*

Text will be more clear if we use Vmark range.

SuggestedRemedy

Line 53 IS:

When the voltage at the PI is between VMark min and VMark_th min, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Line 53 SHOULD BE:
When the voltage at the PI is IN THE RANGE OF Vmark, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Proposed Response *Response Status* **O**

see 255

Cl **33** *SC* **3.5** *P* **59** *L* **22** # 32

LANDRY, MATTHEW SILICON LABS

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Table 33-12 item 2 describes max static power. This can be expressed in terms of current and Vport.

SuggestedRemedy

Replace Type 1 max PPort with 0.35*VPort min. Replace Type 2 max with ICable*VPort min.

These equations presume that VPort mins are updated to 37V and 41V, respectively.

Proposed Response *Response Status* **O**

defer to Vport

Cl **33** *SC* **3.5** *P* **59** *L* **38** # 36

LANDRY, MATTHEW SILICON LABS

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Item 5 is really doing nothing more than telling the reader that IPort should scale with VPort.

They reader should already know this, as PPort max is a max power. Clearly if VPort moves, IPort has to move.

That being said, how is item 5 at all helpful?

SuggestedRemedy

(1) Strike item 5.

or

(2) Remove the multiple lines, and replace item 5 with:
Item: 5
Parameter: Input current (DC or RMS)
Symbol: IPort
Unit: A
Min:
Max: PPort max / VPort
PD Type: 1,2
Addl Info: See 33.3.5.4

Proposed Response *Response Status* **O**

defer to Vport

Cl **33** *SC* **3.5.1** *P* **60** *L* **31** # 105

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Draft D1.0:
Table 33-12 item 1 (Vport) may lead to confusion in the future regarding to how it was derived.
The facts are:
a) Vport minimum for type 1 was derived at peak input power (0.4A) and not at steady state current (0.35A).
(44v-20 ohms * 0.4A=36V.)
(44v-20 ohms * 0.35A=37V.)
The same concept is relevant to Type 2 PSE.
We need to clarify it in the text of 33.3.5.1

SuggestedRemedy

Change line 31 from:

"The specification for VPort in Table 33-12 is for the input voltage range after startup, and it includes loss in the cabling plant."

to:
"The specification for VPort in Table 33-12 is for the input voltage range after startup, and it includes loss in the cabling plant at PD maximum peak load current, as defined by table 33-12 item 4.
PD input voltage at maximum average current is given in Table 33-12 item 5."

Proposed Response *Response Status* **O**

see 31, 259 which suggest changing item in table to 37V.

Cl **33** *SC* **3.5.2** *P* **60** *L* **41** # 118

Vetteth, Anoop Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

This section does not referecnce the power negotiated by the PD over Physical Layer Classification or DLL Classification

SuggestedRemedy

Start the section with a paragraph that references the classified power
Suggestion:
Pport_max is the maximum permissible power negotiated over physical layer classification (per table 33-10) or data link layer classification (as defined in section 33.6a.2.2). Data link layer classification takes precedence over physical layer classification

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **60** *L* **47** # 34

LANDRY, MATTHEW SILICON LABS

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The equation and instructions for measuring PPort seem unnecessary. The power limit applies regardless of the PSE voltage and cable impedance.

The sudden appearance of a resistive approximation of the cable plant really adds nothing for the reader. Stating that the power limit applies over the specified input voltage range is simply redundant. Telling the reader that power equals voltage times current is a bit patronizing.

SuggestedRemedy

Replace 33.3.5.2 with the following:

33.3.5.2 Input average power

The specification for PPort in Table 33-12 (item 2) shall apply for the input power averaged using any sliding window with a 1s width.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **61** *L* **3** # 162

Jones, Chad Cisco

Comment Type **T** *Comment Status* **D** *editorial*

"NOTE—Duty cycle shall be calculated using any sliding window with a 1 s width."
This note contains a shall and the note is in the wrong place.
There is no mention of duty cycle in 33.3.5.2 where it is located.
Lastly can we spell out second?

SuggestedRemedy

change it to "Duty cycle is calculated using any sliding window with a 1 second width."
move it to section 33.3.5.4 just after the first paragraph.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **61** *L* **17** # 143

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The value of Iport_max created by the formula-using PD Pport_max-does not match the value provided in table 33-12. For example, class 0 PD power is 12.95 W maximum and 12.95W/36V = 360 mA, not the 400 mA shown in table 33-12, item 4.

SuggestedRemedy

The PD formula provides the correct answers when the PSE Pport_max values are scaled by 400/350 for the system classified power. A presentation will be provided at the Atlanta Plenary to cover the details.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **61** *L* **36** # 33

LANDRY, MATTHEW SILICON LABS

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The equations use absolute numbers for the port power. They should be variables, which has the added benefit of needing only one equation.

SuggestedRemedy

Replace equation with:
IPort_max = PPort_max / VPort
where
IPort_max is the max DC and RMS input current
PPort_max is the maximum power as defined in Table 33-12 item 2
VPort is the static input voltage

Remove reference to Type 1 PDs, and remove second equation entirely.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Defer to Vport adhoc

Cl **33** *SC* **3.5.4a** *P* **62** *L* # 59

Vetteth, Anoop Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Figure 3-12b and 3-12c
This is PD section and hence the SOA curve for the PSE is irrelevant.

PD_Toverload was defined in the presentation. The maximum value of PD_Toverload is PSE_Tcutmin. Hence PD_Toverload is not relevant anymore.

SuggestedRemedy

Remove the SOA curve for the PSE from both the figures.

Remove PD_Toverload and make the overload max duration to PSE_Tcutmin

Explain the mask in text using inequalities.

Proposed Response *Response Status* **O**

defer to Vport

Cl **33** *SC* **3.5.4a** *P* **62** *L* **48** # 165

Jones, Chad Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

"During transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for up to 10 ms." This is a PSE design requirement (though it does not carry a shall, it is information that a PSE designer should know) and it is located in the PD section. I can't find the corresponding information in 33.2.

SuggestedRemedy

Find an appropriate place in 33.2 to add this information, perhaps 33.2.8.2b.

Proposed Response *Response Status* **O**

defer to vport

Cl **33** *SC* **32** *P* **18** *L* **32** # 85

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *midspan*

Draft 1.0:
The note here is redundant due to the fact that the Midspan is required to meet 33.4.8 requirements in page 72.

SuggestedRemedy

Remove Note in lines 32-34

Proposed Response *Response Status* **O**

see 232

Cl **33** *SC* **33.2.1** *P* **18** *L* **32** # 232

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *midspan*

This note states that 'Midspans implementing Alternative A are not allowed to interfere with the data performance of a 100BASE-TX link. While true it is also true that Midspans implementing Alternative B are also not allowed to interfere with the data performance of a 100BASE-TX link, nor for that matter are Midspans in general allowed to interfere with the data performance of the link. This note however makes that fact unclear by specifically mentioning on 100BASE-TX.

The note then goes on to state 'Refer to Clause 25 for 100BASE-TX compatibility requirements.' If Clause 25 is examined, and in particular its requirement to comply with TP-PMD, two sets of requirements will be found. Set [1] is the channel requirements and set [2] is the MDI requirements. Now I believe that the channel requirements will be met by the conformance requirements found in subclause 33.4.8 'Midspan PSE device additional requirements' and its subclauses so set [1] is covered.

This leaves set [2] and since they are related to the MDI they would not normally apply to the midspan PI. I do believe however in the case of 100BASE-TX there is a requirement that need to be carried over to the PI. This requirement is found in ANSI X3.263-1995 (TP-PMD) subclause 9.1.7 'Worst case droop of transformer' which states:

Baseline Wander tracking by the receiver is dependent on the worst case droop that can be produced by a transmitter. Droop is directly related to the Open Circuit Inductance (OCL) which varies with temperature, manufacturing tolerance, and bias current.
Worst case Baseline Wander Frames vary the transformer bias which causes the droop to change with data content. This variation must be accounted for by the receiver to track the Baseline Wander over long frames. Variation in inductance caused by bias of the transformer can be on the order of 2:1.
The minimum inductance measured at the transmit pins of the AOI shall be greater than or equal to 350 uH with any DC bias current between 0 mA and +8 mA injected as shown in figure 13.

I understand that if a similar inductance is not provided at the output, that is transmit, side of both the data pairs through a Midspan, data corruption can occur due to baseline wander. Since this is a note it does not make this 350uH requirement mandatory, which it has to be.

So in summary:

[a] The note is misleading as it seems to imply that the requirement for no interference only applies to Alternative A 100BASE-TX Midspans.
[b] There is no need to reference the entire Clause 25 as most of the requirements there are also found in subclause 33.4.8
[c] There is one normative requirement which should be carried across to Midspans that support 100BASE-TX, the 350uH requirement. This however is not made mandatory for 100BASE-TX Midspans since this is only a note.

SuggestedRemedy

Add the following new subclause under 33.4.8:

33.4.8.2 Worst case droop of transformer

The Midspan shall meet the inductance requirements of ANSI X3.263-1995 (TP-PMD) subclause 9.1.7 at the pins of the PI used as 100BASE-T transmit pins with the additional requirement that the minimum inductance be meet with any DC bias current between 0 mA and TBD mA.

Editors note to be removed before publication
The need for the additional requirement and related DC bias current range are the subject of discussion in the 350uH adhoc.

Proposed Response *Response Status* **O**

see 85

Cl **33** *SC* **33.2.2** *P* **22** *L* **49** # 156

Dupuis, Joe Hubbell

Comment Type **TR** *Comment Status* **X** *4P*

a) It is out of scope of the standard to limit implementations.
b) There are products in the market that already use the 2 x 2P implementation.
c) There is a market need for >30W.

SuggestedRemedy

Delete "While a PSE may be capable of both
Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same
link segment simultaneously."

Proposed Response *Response Status* **W**

see 151, 100, 166 identical "out of scope of the standard to limit implementations."
argument. The job of a standard is to limit implementations to ensure interoperability.
Everything is a compromise.
Products in the market don't define market need nor do they ensure the need to enable in a standard.

Cl **33** *SC* **33.2.3.7** *P* **29** *L* **16** # 225

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *sd*

Need to define that 'I' used in Figure 33-7 is in fact Iport. This is confirmed in subclause 33.2.8.6 that states that 'If IPort in Table 33-5 exceeds ICUT for longer than Tovld.

SuggestedRemedy

Either:

Add the following to subclause 33.2.3.4:

I
A variable indicating the value of the current being sourced from the PI (IPort).

Or:

Add the following to subclause 33.2.3.4:

IPort
Output current (see 33.2.8.6)

Change I to read IPort is all instances in Figure 33-7.

Add a definition of IPort to 33.2.8.6.

Proposed Response *Response Status* **O**

Cl **33** *SC* **33-7** *P* **29** *L* **20** # 109

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **D** *sd*

Draft 1:
1. Figur 33-7 specifying the behavior of startup mode in addition to overload, short and MPS.
2. The behavior of short and startup are different in many aspects while it was similar in terms of ILIM and TLIM for type 1 legacy PSE.
Now we have to separate the behavioral state diagram to reflect current changes in type 1 and type 2 PSE.
We have to specify Tinrush, Iinrush for startup and ILIM/TLIM for short circuit.
I believe that this differentiation will help to make clearer standards.

SuggestedRemedy

Steps:
1. Replace figure 33-7 with the attached modification.
Changes are: Startup and short circuit behavior has separate drawing and the same behavior of the old drawing.
1.1 Add to 33.2.3.5:
"tinrush_timer
A timer used to monitor the duration of the inrush condition, See Tinrush in 33-5."
2. Update table 33-5 accordingly.
Add item 5a to table 33-5: Tinrush min=50msec, Tinrush_max=75msec (as was before with TLIM). Add to its "additional information" column "see 33.2.8.5"
3. In 33.2.8.5 add:
"a) for minimum of Tinrush. (The deletion of it was an error. we decided that startup in type 2 is similar to legacy PSE!).

Proposed Response *Response Status* **O**

attached figure is "Updated figure 33-7.pdf"

Cl **33** *SC* **4.8** *P* **72** *L* **52** # 220

Law, David 3Com

Comment Type **T** *Comment Status* **D** *midspan*

This subclause states that 'A Midspan PSE inserted into a channel shall provide continuity for the signal pairs.'. I'm not too sure what the term 'continuity' is mean to mean here - if it is an uninterrupted connection I don't think that is true anymore in the case of a Alternative B midspan which will have to use some form of DC blocking to ensure that power can only be sourced in one direction. That of course is covered on the next line which states 'Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.'.

SuggestedRemedy

I suspect that the best approach is simply to delete the text 'A Midspan PSE inserted into a channel shall provide continuity for the signal pairs.' now that Alternative B Midspans are permitted. The line before it still requires that the channel characteristics be maintained.

Proposed Response *Response Status* **O**

It is intended to point out that they must provide continuity for the data. Perhaps this is obvious and we should delete the text.
This is baseline text…

Cl **33** *SC* **4.8.1.4** *P* **74** *L* **14** # 233

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *cable*

ISO/IEC 11801 defines components as Categories and channels as Classes. Hence to form, for example, a Class E channel, Category 6 components such as connectors and jumpers have to be used. Now in the case of ISO/IEC 11801:2002 the specification for Category 5 and Class D were updated from that found in ISO/IEC 11801:1995. Hence a ISO/IEC 11801:2002 Category 5 jumper is equivalent to a TIA/EIA 568 Category 5e jumper.

SuggestedRemedy

Change '.. ISO/IEC 11801:1995 ..' to read '.. ISO/IEC 11801:2002 ..'.

Proposed Response *Response Status* **O**

see 203

Cl **33** *SC* **6a.4.1** *P* **87** *L* **22** # 213

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **D** *L2 adhoc*

This paragrpah does not accurately reflect the resolution to comment #268. It relfects part of the resolution to the comment. It does not address the second timeout aspect.

SuggestedRemedy

Please append the following sentence:

Upon a further timeout of TBD msec where the loss of DLL communication persists, the PSE may remove power from the PD.

Proposed Response *Response Status* **O**

defer to L2

Cl **33** *SC* **figure 33-12b** *P* **62** *L* **31** # 94

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

It can be understood from the drawing the PSE may remove power at I=0.9999999999*(0.4/0.35)*(Pport/Vport) and t=49.99999999msec which is incorect.
PSE must not remove power at this region due to the fact that PD allowed to take peak current up to this point.
It is ILIM_MIN.

SuggestedRemedy

1. Move the solid hirizontal line from PD_Tovld to Tcut_min.
2. Delete PD_Toverload due to the fact that it doesnt add additional information.
3. Add "PSE shall not remove power" below the PD max. operating current curve.

4. See figure 33-12c and add the "PSE shall not remove power" below the PD max. operating current curve.
The rest is OK.

Proposed Response *Response Status* **O**

referred to Vport ahdoc to review and resolve.

parts 3 & 4, comment 59 refers to removing PSE requirement in the PD section.

Cl **33** *SC* **Figure 33-4** *P* **19** *L* **54** # 155

Sanita', Gianluca Nokia Siemens Networ

Comment Type **E** *Comment Status* **D** *midspan*

Missing Midspam PSE, Altenative A.
It seems that this is not allowed from the standard.

SuggestedRemedy

Insert Midspam PSE, Alternative A figure

Proposed Response *Response Status* **O**

presently 10/100Mb alt A midspans are disallowed. With the allowance of 1000Mb alt A midspans that could conceivably be used in a 10 or 100Mb link, this needs reviewed. CE feels it needs allowed and yet another informative drawing added.

Cl **33** *SC* **Figure 33-7a** *P* **30** *L* **54** # 186

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **D** *sd*

Figure 33-7a is really not necessary. I think that Figure 33-6 is a behavioral machine. Meaning that the details of classification can be described in the relevant physical classification section (one event or two event) followed by DLL if appropriate.

SuggestedRemedy

Please delete Figure 33-7a and retain do_classification.

Proposed Response *Response Status* **O**

Cl **33** *SC* **figure 33-9a** *P* **44** *L* **39** # 90

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Draft 1.0:

The title of figure 33-9a is "PI operating current template"
It is only defines the maximum current.
In addition it contains error: The current after 75msec is Icable*0.4/0.35 and not 720mA.

SuggestedRemedy

Option A: (Recomended)

Delete figure 33-9a and use only figures 33-12b and figures 33-12c due to the fact that they contains PSE and PD data and hence figure 33-9a is redundant.

Option B:

Fix error in figure 33-9a and change title to read:
"Figure 33-9a - PSE PI maximum operating current vs. Time"

Proposed Response *Response Status* **O**

third time commentor pointed out Icable*.4/.35…

defer to Vport adhoc to determine correct title of Figure.

Cl **33** *SC* **Table 33-12** *P* **59** *L* **17** # 95

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Draft D1.0:

Table 33-12 items 1:
It is 39.71V and not 40V (50-12.5 OHMS x 0.72A*0.4A/0.35A=39.71V).

SuggestedRemedy

Table 33-12 item 1 for type 2 PD:
Change PD minimum operating voltage to 39.71V.

Proposed Response *Response Status* **O**

see 31, recommended 41V…

defer to Vport