Cl **00** *SC* **00** *P* *L* # 31195

Thompson, Geoff Nortel

Comment Type **TR** *Comment Status* **R**

PD equipment that is covered in the Code of Conduct on Energy Consumption of Broadband Equipment (from the EUROPEAN COMMISSION DIRECTORATE-GENERAL, JOINT RESEARCH CENTRE, Institute for the Environment and Sustainability, Renewable Energies Unit) will need to stay within the bounds of Type 1 power limits.

SuggestedRemedy

Remove all specifications for Type 2 devices and reformulate the standard to only support devices which meet the EC Code of Conduct on Energy Consumption of Broadband Equipment.

Response *Response Status* **U**

REJECT.

Although some Ethernet equipment is covered under the Code of Conduct on Energy Consumption of Broadband Equipment, it is by no means comprehensive and many types of Ethernet equipment fall outside of the scope of that specific Code of Conduct. For example, equipment covered by the Code of Conduct on Data Centres, published by the same body is not expected to be covered by the Broadband Code of Conduct.

Furthermore, if the commenter examines the Code of Conduct on Energy Consumption of Broadband Equipment he will find that power delivered by the PSE is specifically excluded by section A.5 ("Power delivered to other equipment (e.g. over USB or PoE) shall not be included in power consumption assessment").

Lastly, the Code of Conduct on Energy Consumption of Broadband Equipment specifies ONU equipment that exceeds 12.95W (e.g. 10Gb/s point-to-point or point-to-multipoint interfaces). It may be expected that some implementations of such devices will include power supplied over Ethernet from the home gateway device to the optical interface at the demarcation point. As such, this is a prime application of PoE that helps justify the broad market potential for the project.

Cl **00** *SC* **00** *P* *L* # 32146

Thompson, Geoffrey Nortel

Comment Type **TR** *Comment Status* **A**

D3.1 comment 16
The response to Mr Claseman is insufficient and inaccurate.
a) The "group" referred to in the response is presumably the TF/CRG, NOT the balloting group which is the Working Group.
b) There is no vote of "the group" cited regarding the response given to actually provide evidence of "the feeling of the group".
c) There was no technical rationale nor reference to approved documentation for the project to support the rejection.
Therefore, I am "piling on" to his comment.

SuggestedRemedy

Either:
Provide an appropriate technical rationale for the TF/CRG "recommendation" that Mr Claseman's comment be rejected along with a documented vote of the TF/CRG

-OR-
Accept his comment.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment 55 for resolution of the 4P comments.

Accepting this comment results in no change to the text.

This comment (D3.1 comment 16) was a comment against D3.0 that the Comment Editor inadvertently left out (actually part of a group of comments). These were carried forward into D3.1 and reviewed to ensure the commenters concerns were addressed. This comment was similar to other comments in D3.0, all of which were resolved as OBE by D3.0 comment 72. The text in the response to D3.1 comment 16 is the exact text used to close the comments in D3.0.

Perhaps it was poorly worded but the agreement in the room was that the comment resolution group agreed by voice to reject the comment as the concept was that a 4P system is twice a 2P system and the 2P standard is not yet complete. The D3.0 commenter agreed that we reject his comment and he respond as unsatisfied so it would carry forward. If D3.1 comment 16 would have been in D3.0, it would have been closed as 'REJECT OBE 72'. This is what was done in effect, except the text from D3.0 comment 72 was brought over to D3.1 comment 16 so that the reader would not have to refer back to older comments. There was one other 4P comment in D3.1, it was a straight reject with no reason (again, at the agreement of the commenter to carry it forward) so D3.1 comment 16 could point to this other 4P comment as it would give the commenter no background on why it was rejected.

Based on the number of comments this go around, the 2P standard STILL isn't done and 4P comments will likely be rejected again and carried forward.

Cl **25** *SC* **25.4.4a.1** *P* **19** *L* **27** # 32119

Dawe, Piers — Avago Technologies

Comment Type **TR** *Comment Status* **R**

This is not a standard for test equipment. You are defining an 'equivalent system time constant' which you should do precisely, without 1% (or is it 2%)? ambiguity and slop. It's up to the test equipment manufacturers and customers how accurately they want to measure this, or anything else, and whether they use instruments that won't give false positives, or false negatives, or will give their best estimate.

SuggestedRemedy

Remove the '+/- 1 %' from Figure 25-1.

Response *Response Status* **U**

REJECT.

I see the same approach taken in other clauses. ex/ section 7.4.1.5 DC Common Mode Output Voltage

Piers Dawe reply to the rejection:

Yes, other clauses did it in the past. Doesn't mean we should do it again.

Cl **25** *SC* **25.4.4a.1** *P* **19** *L* **31** # 15

Dawe, Piers — Avago Technologies

Comment Type **TR** *Comment Status* **X**

To resolve comment D3.2/119, 'This is not a standard for test equipment.' We can't tell the tester to use accurate or inaccurate test fixtures. It's his job to work out his own tolerances so that when he says something passes (or fails), it does. If you want to give guidance, NOTE 1 is an ideal place.

SuggestedRemedy

Delete the +- 1% from the figure. Change note to:
NOTE 1-The value of the 100 W termination resistor can be adjusted to compensate for the test circuit resistance. A 1% resistor tolerance is recommended. The test circuit resistance should exceed 2 kW.

Proposed Response *Response Status* **O**

Cl **25** *SC* **25.4.4a.1** *P* **19** *L* **51** # 18

Dawe, Piers — Avago Technologies

Comment Type **T** *Comment Status* **X**

What does 'The test circuit resistance should exceed 2 kW.' mean? Is that the differential resistance of the current source I_BIAS?

SuggestedRemedy

Please clarify.

Proposed Response *Response Status* **O**

Cl **25** *SC* **25.4.4a.1** *P* **19** *L* **51** # 6

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3

Figure 25-1 title:
The title use "test fixture" and the text in Note 1 use "test circuit"
Let's use the same term in both.

SuggestedRemedy

Group to pick one of the terms and synchronize between Figure 25-1 title to Note 1 text.

Proposed Response *Response Status* **O**

Cl **25** *SC* **25.4.4a.1** *P* **19** *L* **51** # 5

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3 Note 1 page 19 line 51 says:
"NOTE 1—The value of the 100 ohm termination resistor can be adjusted to compensate for the test circuit resistance. The test circuit resistance should exceed 2 kohm."

Assuming that the reader is not familiar with presentation and discussions on the the issue which are not relevant for the normative requirements or guidelines in the spec, the following are not clear from Figure 25-1 nor the text:
1. What is "the test circuit resistance" which part of figure 25-1 is it?
(I guess that it is the par from the PHY output to the Capacitor input. Please confirm.)
2 "The test circuit resistance should exceed 2 kohm" will be clear too if (1) will be clarified.

SuggestedRemedy

Group to clarify it.

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.1.3** *P* **37** *L* **8** # 16

Dawe, Piers — Avago Technologies

Comment Type **TR** *Comment Status* **X**

To resolve comment D3.2/123, which points out that Fig 33-3 shows a PI connected to a non-PoE PHY through a midspan.

SuggestedRemedy

Label the broken right hand end of the medium 'To PD' and add PD to the abbreviations list in the figure. Draw a rectangle (or something) over the medium within the midspan to the left of the connection to the PSE, and label 'See 33.2.2'.

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.1.3** *P* **37** *L* **8** # 32123

Dawe, Piers — Avago Technologies

Comment Type **TR** *Comment Status* **R**

Fig 33-3 shows a PSE in a Midspan capable of applying power to a medium. There is a PI on the right, and an interface without a name on the left, the medium continues to a PHY with no PD (which you should not apply power to). By comparison, Fig 33-6 shows two arrangements which power the right hand side but not the left. The medium is not continuous through the Midspan. D3.0 comment 380 raised this problem before.

SuggestedRemedy

Correct Fig 33-3. Show some arrangement to break the continuity within the Midspan. Could also show a PHY with PD on the left.

Response *Response Status* **U**

REJECT.

The reply to D3.0 comment 380 still applies "A midspan doesn't have a PHY, therefore it doesn't have an MDI. This is our best effort to
illustrate a midspan. Commentor is welcome to submit his own drawing"

The comment hints at a possible lack of understand of the concept of a midspan. This is a device that applies power to a PD that sits in between a non-PoE switch and a PD. The drawing shows the PI on the right which can be thought of as the output of the midspan. This is where you connect the PD and the only place where the midspan would ever apply power (hence the label PI). The unnamed connection to the left is to the legacy non-PoE switch. The midspan will not apply power to this portion of link segment (not if it wants to be compliant).

Piers Dawe reply to the rejection:
If the PHY on the left in this Figure 33-3 is a non-powered PHY you shouldn't connect it to the PI through the Midspan, which is what you show even though you say "The midspan will not apply power to this portion of link segment (not if it wants to be compliant).".
All you need to do is add some indication of a break in the medium within the midspan, to the left of the PSE.

Cl **33** *SC* **33.1.4** *P* **37** *L* **39** # 17

Dawe, Piers — Avago Technologies

Comment Type **T** *Comment Status* **X**

Why has '0.60' been changed to '0.600'?

SuggestedRemedy

This may be a topic for the maintenance meeting.

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.4** *P* **44** *L* **4** # 20

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3
The text says:
"The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–10, and Figure 33–11."
However it is important to emphasis that although the PSE and PD specifications are written as independent parts and may be tested as independent parts, the expected behaviour of the PSE state diagram should be tested with compliant PD test fixture and this is true for the PD state diagram.

SuggestedRemedy

Change from:
"The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–10, and Figure 33–11."

To:
"The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–10, and Figure 33–11 when connected to a compliant PD"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.4.4** *P* **44** *L* **21** # 4

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3

There is no such term PD Inrush.
It should be "PD Inrush current"

SuggestedRemedy

Lines 21 and 22 (two occurrences): Replace "PD inrush" with "PD inrush current"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.4.4** *P* **44** *L* **22** # 11

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Dtaft D3.3
The wording of "Using only this PI voltage information is insufficient" is confusing.
Discussion:
If it "is insufficient" as the text says thEn why we allow it? it may cause interoperability problems...
The reason why we allow it is to continue to support legacy which work fine so using the wording "is insufficient" tells the reader that we know for a fact that in all cases that this method is used it is not working which is also not true.

SuggestedRemedy

Change "is insufficient" to "may be insufficient"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.4.6** *P* **49** *L* **14** # 7

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3
do_short_detect function detects short circuit condition and not overload condition.
However short circuit condition may be many scenarios that is ended with "short circuit" condition from the PSE point of view examples:
1. Very high load that coresponds to very low output resistance load < 1 ohms.
2. Overload that coresponds to current > Icut_max
All of the above may be considered as overload conditions or "short circuit" condition from the PSE point of view.
I belive that short circuit doesnt mean zero ohms.
As a result do_short_detect function detects short circuit and overload as well.

SuggestedRemedy

Change from:
"do_short_detect
This function monitors the PSE output current and detects an overload condition for TLIM within a sliding window."

To:
"do_short_detect
This function monitors the PSE output current and detects a short circuit condition or an overload condition for TLIM within a sliding window."

(All short circuits are overload as well but not all overload is short circuit. It depends by the PSE output impedance as well. The difference between do_short_detect and do_overload_detect is a) the time TLIM or TOVLD b) Current thresholds c) Enforcement d) different states which requires two seperate functions)

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.4.6** *P* **49** *L* **19** # 12

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Draft D3.3.
If the result of the do_short_detect function is TRUE, it doesn't necessarily mean that the PSE has detected a current limit condition which is true to specific implementation.
The PSE may detect TRUE condition by only detecting that the current pass some threshold without activating current limit circuitry.

SuggestedRemedy

Change from:
"Values:
TRUE: The PSE has detected a current limit condition.
FALSE: The PSE has not detected a qualified current limit condition."

To:
"Values:
TRUE: The PSE has detected a short circuit condition.
FALSE: The PSE has not detected a qualified short circuit condition.

Note: short circuit current may be any current above Ipeak as illustrated in figure 33-15"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.6** *P* **53** *L* **11** # 3

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3

Figure 33-12 and figure 33-13:
In the text, we change Vdetect to Vport.
We should do it to figures 33-12 and 33-13 as well.
Replace Vdetect with Vport

SuggestedRemedy

Figure 33-12 and figure 33-13:
Rplace "Vdetect" with "Vport"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.6.1** *P* **53** *L* **48** # 8

Darshan, Yair
Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3

remove the word "and"

SuggestedRemedy

remove the word "and"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.6.1** *P* **53** *L* **48** # 13

Darshan, Yair
Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Draft D3.3

The text "The detection voltage VPort shall be within the Vvalid voltage range at the PSE PI (as specified in Table 33–4) with a valid PD detection signature connected (as specified in and Table 33–14)." contains error technically and from legacy text point of view.
Table 33-14 should be replaced with Table 33-5.
See discussion and rational below.

Discussion - Review of the spec development from IEEE802.3af until D3.3:
1. The specification of the 802.3af says:
"33.2.5.1 Detection probe requirements
The detection voltage Vdetect shall be within the Vvalid voltage range at the PSE PI as specified in Table 33-2 with a valid PD detection signature connected."
Table 33-2 describes Vvalid = 2.8V to 10V but talks about "Accept signature resistance" which is 19K to 26.5K but the text specify it as " a valid PD detection signature" which is actually the "valid PD signature" as seen by the PSE and is equivalent to "Accept signature resistance" which is 19K to 26.5K.

2. The specification of the 802.3at says:
2.1 First round of the draft was
"33.2.6.1 Detection probe requirements
The detection voltage Vdetect shall be within the Vvalid voltage range at the PSE PI as specified in Table 33-4 with a valid PD detection signature connected, as defined in Table 33-5."
Table 3-5 is the IEEE802.3af Table 33-2 which confirms that it should be 19K to 26.5K and confirms that we follow our historic intent and explicit old text.

2.2 Second round of the draft is
"33.2.6.1 Detection probe requirements
The detection voltage Vport shall be within the Vvalid voltage range at the PSE PI with a valid PD detection signature connected, as specified in Table 33-4 and Table 33-14, respectively."

Here for the first time Table 33-5 was replaced with Table 33-14 which is the PD signature i.e. 23.75K to 26.25K which is an error as can be seen above.

2.3 The third round of the draft is the current version which is similar to the content of the previous version with some editing work.

Summary: The legacy text requires Vvalid to be 2.8V to 10V with vaild PD signature as seen by the PSE and is 19K to 26.5K per Table 33-5 and not per table 33-14. So from legacy point of view we can not change it...

Techniacl Discussion:
From technical point of view we need to keep Vvalid with 19K to 26.5K and not with 23.75K

to 26.25K otherwise it will infringe Vvalid. Example:
If the designer desing Vvalid to work with e.g. 23.75K than when 19K signature will be connected it will be less than 2.8V which is not compliant behaviour.
But if we design 2.8V with 19K than 2.8V minimum will be kept with 23.75K which is higher than 19K etc. etc. etc.
In general 2.8V to 10V in the PSE should cover "valid signature range as seen by PSE which is "accept signature resistance range" in table 33-5. This is how it is in the original IEEE802.3af.

SuggestedRemedy

Replace Table 33-14 with Table 33-5.

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.6.1** *P* **53** *L* **50** # 2

Darshan, Yair Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D4.0

"Vdetect" is an error. It should be "Vvalid".

SuggestedRemedy

Replace "Vdetect" with "Vvalid"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.8.2** *P* **58** *L* **25** # 1

Darshan, Yair Microsemi Corporation

Comment Type **E** *Comment Status* **X**

DRAFT D4.0, the note in lines 25-26:
The text:

"NOTE—In a properly operating system, the port may or may not discharge to the VMark range due to the combination of channel capacitance and PD current loading."

is not fully acurate due to the fact that it is not only the function of the channel capacitance. It is also a function of the PD capacitance.

SuggestedRemedy

Change from:
"NOTE—In a properly operating system, the port may or may not discharge to the VMark range due to the combination of channel capacitance and PD current loading."

To:
"NOTE—In a properly operating system, the port may or may not discharge to the VMark range due to the combination of channel and PD capacitance and PD current loading."

(The minimum PD capacitance during detection and classification (Table 33-14 =0.05uF) is at least 5 times higher that the channel capacitance so the channel capacitance is only 20% of the minimum system capacitance at the above operating mode.)

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.9** *P* **60** *L* **53** # 10

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3

Table 33-11 item 15, additional information column:
The spec requires that Trise will be measured from 10% to 90% of Vport however Vport is a parameter that is defined in Table 33-11 item 1 which is a number from 44V to 57V for Type 1 and 50 to 57V for type 2.
The correct definition is "From 10% to 90% of the entire port voltage range during turn on at POWER_UP state" or equivalent wording to correct the above error.

SuggestedRemedy

Change the text in the "additional information" column from:
"From 10% to 90% of Vport"

To: "From 10% to 90% of the entire port voltage range during turn on at POWER_UP state"

(This change fix the problem in a way that allows port voltage range to be from:
a) 0V to Vport (Vport as specified in Table 33-11 item 1)
b) Voff to Vport (Voff is specified in Table 33-11 item 17)
c) Vmark to Vport
d) Vclass to Vport
e) Any minimum voltage at the port to Vport

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.2.9** *P* **61** *L* **16** # 32149

Thompson, Geoffrey — Nortel

Comment Type **TR** *Comment Status* **R**

D3.1 comment 198
The comment DOES NOT have the effect of lowing the maximum PD power to 22 watts. The group evidently either misunderstood the intention or wishes to miscommunicate about it.

The proposed change allows for a lower voltage to be used at lower power levels and relieves the spec from having to the highest current at the lowest voltage. Not all power levels have to be provided at all voltage levels. You would get to reduce the power from the max by reducing the voltage.

SuggestedRemedy

As requested in previous comment.

Response *Response Status* **U**

REJECT.

Vote on accepting the suggested remedy from D3.1 comment 198 which is:

Change item 1 Vmin from "44" to "37+(Rch*Icable)" [corrected typos]
Change item 2 Vmin from "50" to "37+(Rch*Icable)" [corrected typo]

Y: 0 N: 17 A: 5

CRG justification for rejection:

The group contends that lowering the port voltage lowers port power. Additionally, interoperability could be compromised by having compliant ports without the ability to provide 30W.

This is a new feature request. It may be a great feature but it is a big change to the text and is best left as a proprietary solution. It is the consensus of the CRG that we achieve all of our objectives without making this change.

SME response:
The task force interpreted the text differently than the subject matter expert.

The task force requested the proposer to resubmit a corrected remedy. This was not done.

See the text, in the original response, below the line "--- Here is what I believe was intended ---" for the subject mater expert interpretation.

Cl **33** *SC* **33.2.9** *P* **61** *L* **16** # 31058

Anslow, Peter
Nortel Networks

Comment Type **TR** *Comment Status* **R**

Requiring 50 V minimum from a Type 2 PSE means that it cannot be operated from commonly available 48 V supplies. See Thompson comment #482

SuggestedRemedy

Change the following:
Table 33-11, Item 1 Vport min PSE Type 2 to 44 volts
Table 33-11, Item 2 min value, PSE Type 2 to 44 volts
Table 33-18, Item 1 Vport min PSE Type 2 "50" value to "44" becoming "44-(RCh×ICable)"
Table 33-18, Item 3 Voverload min PSE Type 2 "50" value to "44" becoming "44-(RCh×ICable×400/350)"

In addition, it makes no sense to have different voltage ranges for Type 1 vs. Type 2 PDs as each has to be able to operate with the both types of PSEs during start-up. In particular a Type 2 PSD has to operate at the low voltage of a Type 1 during start-up while establishing the Data Link Layer communication

Response *Response Status* **U**

REJECT.

See 198 for lack of support to lower the PD power. This proposal lowers the power even further than comment 198.

show of hands for people in favor of lowering power of the PD to slightly lower than 22W:
for: 0
against: 20

You are also missing a subtle point that when a type 2 is behaving as a type 1 at boot up, it has to operate over the type 1 range; therefore there are no difference in the operating ranges of a PD.

Additionally, the same resolution to D3.0 comment 482 applies.

During the May 2006 Interim, the IEEE 802.3at task force voted to adopt 50 V as the minimum Vport.
Y: 37 N:0 A: 1
This was done after extensive evaluation of the system tradeoffs. One result of the discussions was the revelation that battery back up systems have only supplied about 10% of their available power when the voltage has reach 44V, therefore a boost system would be required to best utilize the available power fomr the battery backup system. It was determined that boosting to 50V was no more of a burden than boosting to 44V.

Multual identification of the PSE and PD type is possible. A Type 2 PD may provide useful functionality on a legacy system or it may indicate that it is under powered.

A type 2 PD range fits within a type 1 PD operating voltage range. Therefore, a type 1 (legacy) PD can be powered by a type 2 PSE.

A PSE normally would not change its voltage range when it provides power to different PD types.

Cl **33** *SC* **33.2.9** *P* **61** *L* **16** # 32147

Thompson, Geoffrey Nortel

Comment Type **TR** *Comment Status* **R**

D3.1 comment 58
The response to Mr Anslow is inaccurate.
a) There is no reasonable rationale that all power levels have to be available at all voltages. That wouold require the PSE to be a voltage source rather than a current source which is an implementation matter and not proper for the standard to regulate.
b) Since the max current and power is beng lowered, there is no technical reason to mandate the higher voltage.

Therefore, I am "piling on" to his comment.

SuggestedRemedy

Allow a Vport min value down to as low as 44 volts in any situation in which the remaining operating requirements of the moment are being met.

Response *Response Status* **U**

REJECT.

Vote on accepting the suggested remedy.

Y: 1 N: 16 A: 7

CRG justification for rejection:

The group contends that lowering the port voltage lowers port power. Additionally, interoperability could be compromised by having compliant ports without the ability to provide 30W.

This is a new feature request. It may be a great feature but it is a big change to the text and is best left as a proprietary solution. It is the consensus of the CRG that we achieve all of our objectives without making this change.

SME response:
The interpretation of this comment appears different from the original proposer. The new comment reduces interoperability. Only some PDs will operate at the lower voltages and or lower power levels.

This appears to be a feature that is outside the scope of this standard.

Also see response to D3.1, 58.

Cl **33** *SC* **33.2.9** *P* **61** *L* **16** # 31198

Thompson, Geoff Nortel

Comment Type **TR** *Comment Status* **R**

Also line 20
It makes no sense to require different voltage ranges for Type 1 vs. Type 2 PSE supplys except to the extent required to maintain far end voltage at the supplied (larger) current. That design freedom shuld be left to the implementor. See also next comment

SuggestedRemedy

Change item 1 Vmin from "50" to "37 + (Rch + Icable)"
Change item 2 Vmin from "50" to "37 + (Rch + Icable)"

Response *Response Status* **U**

REJECT.

Accepting the comment has the (perhaps) unintended effect of lowering the PD power to 22W.

Straw poll taken from room:
are you in favor to lowering the PD power to 22W
20 people opposed to lowering the power to 22W
zero people in favor of lowering the power to 22W

rationalization follows:

The remedy appears to have errors in it. I assume the proposer wants PSEs to provide a PSE voltage (lower than present values) that the PDs need, that is dependent on system parameters (cable length, cable quality, Ipd, PD type).

This would be very difficult to test. I suggest the task force vote to determine if they want to give the proposer time to correct their text, or reject this because these changes may significantly complicate this specification.

-------- Here is what I believe was intended ------

The proposed remedy adds a voltage to a resistance and a current. Assume the remedy should be:
Vmin = 37 + Rch * Icable

Here 37 is suppose to be the Vpd. The proposal would be incorrect for type 2 PDs.

Type 1 PD Vpd = 37

Type 2 PD Vpd = 50 - Rch * Icable

A minimum voltage could be calculated for a type 2 PD (Vpd = 50 - 12.5*0.6 = 42.5 V) and then the formula used could become:

Vmin = Vpd_min + Rch * Icable.

This formula is only valid during average power demand. Different values would result when PD Ipeak was drawn.
Type 1 PD Vpd = 44 - 0.4*20 = 36 V

Type 2 PD Vpd = 50 - 0.6*400/350*12.5 = 41.4 V

This gets more complicated when Ipeak changes and a quadratic formula needs to be used to calculate currents.

Cl **33** *SC* **33.2.9.2** *P* **61** *L* **49** # 9

Darshan, Yair Microsemi Corporation

Comment Type **E** *Comment Status* **X**

We change Imin2 and Imin 1 to Imin.
Change Imin2_max to Imin_max.

SuggestedRemedy

1. Change Imin2_max to Imin_max.
2. Also in 33.2.9.4 p. 62 line 13.

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.3.1** *P* **71** *L* **42** # 31035

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **R**

Draft D3.1:

The note in line 42 precludes the ability to reduce power loss over the cable and increase overall system efficiency.
Rational:
Using a Type 2 PD that requires a total of 24W (example) on a 2P can also take a toatal of 24W over all 4 pairs with simple PD implementation.
In this case this PD can work on 2P PSE or on 2x2P PSEs with the same PD behaviour which is transparent to the user.

In addition let's assume that in this case both pairs are comming from the same box and the same power supply. This is a classical case in which by using all pairs we effectively reduce the channel power loss and allows interoperable and relaible operation.

If Icable meet the specification of 2P then I<Icable certaily meets the same specification so preventing feeding the current all over the 4 pairs doesnt make sense.

This is implementation that is inline with the global effort for reducing power loss and in my opinion we are not authrized to preclude implementations that meet the numbers and state machines of this standard.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:
"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously may recieve power from both Mode A and Mode B is out of scope of the standard"

Response *Response Status* **U**

REJECT.
1) Comment is technically incorrect. This sentence does not preclude 24W over 4 pairs.
2) The rest of the comment glosses over a set of complex issues involving how the PSE would determine it was acceptable to power all four pairs.
3) The comment glosses over the special considerations needed in the PD to accommodate this new mode of operation.
4) The Task Force has specifically made it clear that 2 separate PDs per four pair cable must be accomodated.
5) Recommended solution does not address 2, 3, 4 and is not possible to implement in the context of a standard.

Cl **33** *SC* **33.3.4** *P* **73** *L* **54** # 19

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft D3.3
Table 33-14, Input Inductance.
The reader may assum that it can be inductance in paralel to the port which is not the case (otherwise port will be shorted at DC voltage). This is "series input inductance".

SuggestedRemedy

Replace Table 33-14 item "Input nductance" with "Series input inductance"

Proposed Response *Response Status* **O**

Cl **33** *SC* **33.3.6** *P* **76** *L* **12** # 32148

Thompson, Geoffrey — Nortel

Comment Type **TR** *Comment Status* **R**

D3.1 comment 194
I do not accept the response.
The methodology is contrary to the well accepted and proven practices of 802.3

SuggestedRemedy

Of the the 3 systems elements, PSE, cabling, PD
specify only two.

Response *Response Status* **U**

REJECT.

Vote to pursue suggested remedy from D3.1 comment (many choices, TF to pick one):

Y: 0 N: 15 A: 2

The methodology has served well since the release of 802.3af in June 2003 so it is not without precedent. Furthermore, while commenter may be correct with respect to data communications standards, this degree of specificity is not uncommon in remote powering systems.

The system is defined by a quadratic equation which has two solutions for each operating point; one of which is unstable. Our rigid specification ensures operation at the stable solution.

Additionally, this is a new feature request. The TF has adopted the stance that it will take on no new work as of July 08. New feature requests require an accompanying solution. Commenter is welcome to submit marked up sections and new text required to implement comment for consideration. This is not a trivial change as it would touch many parts of the document.

Cl **33** *SC* **33.3.6** *P* **78** *L* **12** # 31194

Thompson, Geoff — Nortel

Comment Type **TR** *Comment Status* **R**

Overall comment.
I believe that the system (i.e. PSE, cabling and PD) is over specified. Given our system configuration once you specify two fo the elements, you have defined the results for the third and additional "shalls" just get in the way and provide the potential for technical conflict.

SuggestedRemedy

A number of solutions are possible. I suggest making PSE and cabling normative and just make the PD tolerate the results. That would require changing 33.3.7, page 78, line 12 to read something like:
"The power supply of the PD shall operate within the system constraints of the specified PSE and cabling systems. Those resulting values are provided in Table 33-18 for reference."

Response *Response Status* **U**

REJECT.

The TF has purposely engineered margin into the specifications of the PSE and PD by rigidly specifying each end, with the added bonus of ensuring interoperability. The Table has worst case values and a PD that conforms will be ensured to interoperate.

Vote to reject
y- 14 n-1

Cl **33** *SC* **33.3.7** *P* **78** *L* **25** # 31199

Thompson, Geoff — Nortel

Comment Type **TR** *Comment Status* **R**

Also, line 34
It makes no sense to have different voltage ranges for Type 1 vs. Type 2 PDs as each has to behave identically during the start-up when Data Link Layer communication is being established. Specifically a Type 2 PSD has to operate at the low voltage of a Type 1 during this phase of operation

SuggestedRemedy

In Table 33-18, item 1, eliminate the Type 2 entry and have the Vmin parameter be 37 for all PDs under all conditions.

In Table 33-18, item 2, eliminate the Type 2 entry and have the Vmin parameter be 36 for all PDs under all conditions.

Response *Response Status* **U**

REJECT.

The differing minimum input voltages ensure maximum power delivery for each PD type. Higher operating voltages result in less cable loss making the system more efficient.

Also, see comment 58 for additional arguments against this solution.

Table 33-18 item 1 is for static operating input voltages, and includes the rated input power. This is correct. However it is desirable that a type 2 PD start like a type 1 PD if installed in an ".af" worst-case environment. This appears to be covered by the following:

Section 33.3.2 (P72 l5) indicates that a type 2 PD must conform to type 1 power restrictions.

33.3.5.2 (P77 l15) states a T2 PD only seeing a T1 PSE should conform to T1 electricals of T33-18.

33.3.7.3 states that a T2 PD should behave like a T1 PD during/after inrush/poweron.

Cl **33** *SC* **33.4.8** *P* **87** *L* **51** # 32076

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **R**

We are doing the same mistake we did in the past in which the 350uH adhoc was formed to resolve by allowing the droop method (implementation independent) as alternative to the OCL (specific implementation).

In order to achive 350uH (or its equivalent droop numbers) operation when Type 2 100BT ALT A Midspan is connected we forced implementation (regulating Iunb to Type 1 levels) instead of specifying the Midspan output TX signal requirements so legacy recivers in the Switch will work.

SuggestedRemedy

Set the Midspan ad hoc to discuss it and propose a solution.
See attached file "Midspan 100BT ALT A TX output signal template" with possible alternative.

Response *Response Status* **U**

REJECT.

The TF has reviewed the presentation and the following vote was taken on the adoption of the presentation.

Y: 4 N: 11 A: 8

26%, no consensus to change existing text and existing text stands.

Cl **33** *SC* **33.4.8** *P* **87** *L* **51** # 14

Darshan, Yair
Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Draft D3.3 , 33.4.8, page 87 line 51

Comment:

There is already a requirement in the specification that guarantees the operation of 100BT ALT A Midspans.

We can add it as alternative to 33.4.8 text.

(Rational: The only difference between 350uH systems with Midspan to a 120uH systems with Midspan is the 120uH in the PD transmitter.

The rest of inductances in the Type 2 systems is 350uH minimum.

The worst case effect of the 120uH inductance in the TYPE 2 PD cause 0.2dB max change at the system transfer function at frequency below 300KHz (see my presentation in November 2008) and 0.2dB is nothing compared to above 20dB margin in the system that we have. In addition, we can even modify 33.4.9.2 equation by adding 0.2dB to account for the worst case case of 120uH in the PD TX i.e. harden the requirements from 33.4.9.2 by 0.2dB more…)

SuggestedRemedy

Change from:
"Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–11).

To:
"Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–11) or meet 33.4.9.2.

Proposed Response *Response Status* **O**