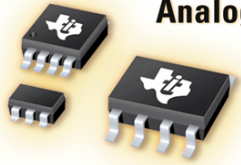IEEE802.3af POE meeting
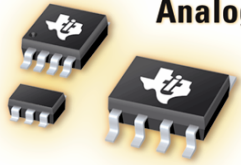
High Power-over-Ethernet over Two Pairs

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IEEE802.3af POE meeting January 2006 : High Power-over-Ethernet over Two Pairs

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- Scope of investigation:

  1. To define and perform the analysis of a system providing more power on

     2 pairs

  2. To evaluate a proposed center-tapped (CT) transformer configuration for

     delivering increased power levels over the signal pair

  3. To confirm sufficient current handling capability, and determine any

     resultant impact on signal integrity

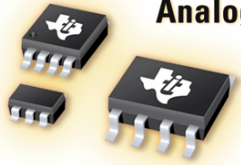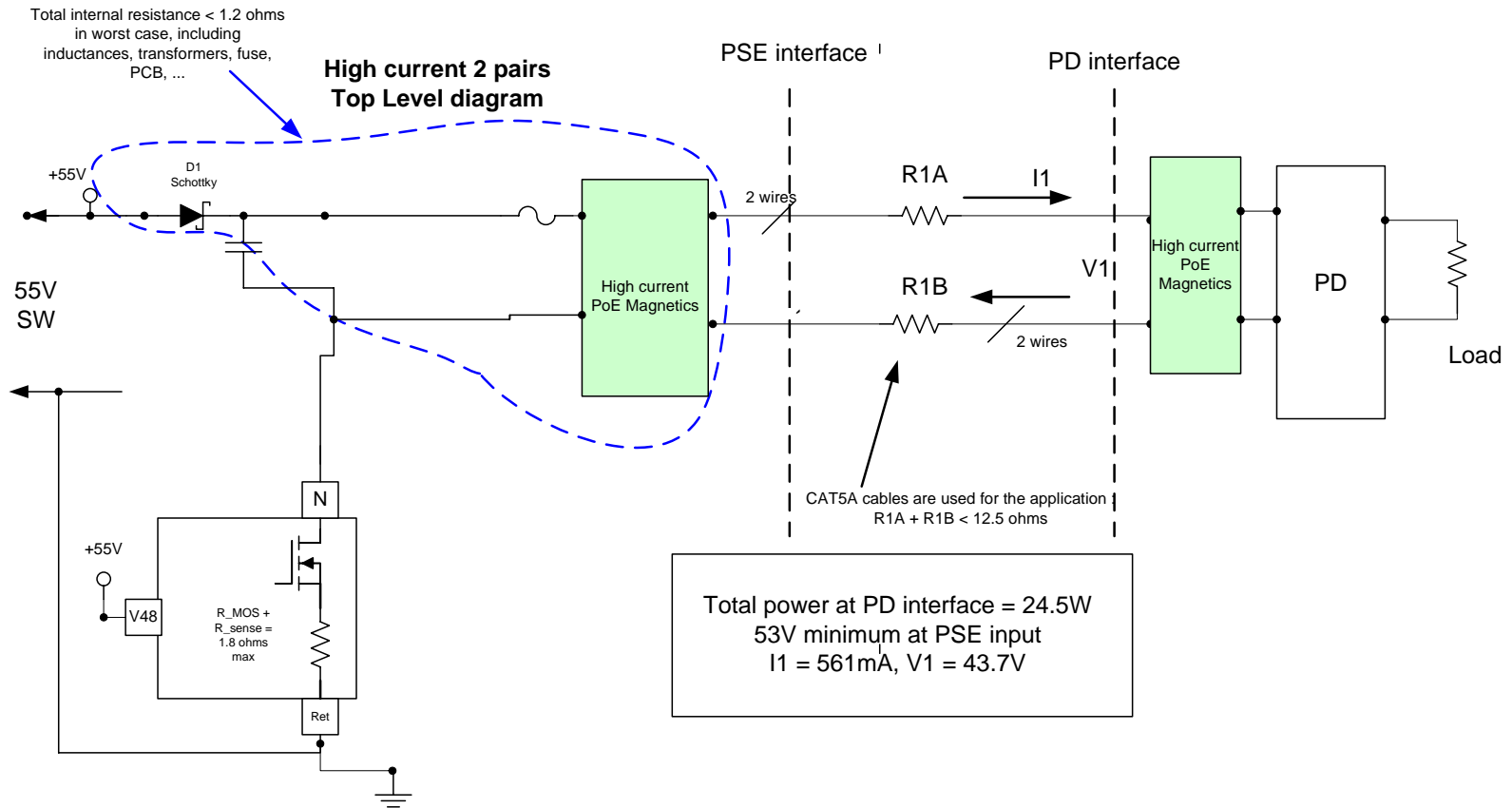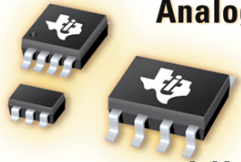**IEEE802.3af POE meeting January 2006 : High Power-over-Ethernet over Two Pairs**

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# Figure 1 : Simplified diagram of high current on 2 pairs application

Total internal resistance < 1.2 ohms in worst case, including inductances, transformers, fuse, PCB, ...

High current 2 pairs Top Level diagram

PSE interface

PD interface

+55V

D1 Schottky

55V SW

High current PoE Magnetics

2 wires

R1A — I1

High current PoE Magnetics

PD

Load

V1

R1B

2 wires

N

+55V

V48

R_MOS + R_sense = 1.8 ohms max

Ret

CAT5A cables are used for the application
R1A + R1B < 12.5 ohms

Total power at PD interface = 24.5W
53V minimum at PSE input
I1 = 561mA, V1 = 43.7V

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UNH Test Setup and Test description

➢ Existing TI PSE and PD EVM were modified to allow sourcing of up to 33.4 W (up to a nominal limit of 660 mA).

➢ This circuit provides a method for coupling DC power to the CAT-5 twisted pairs, without passing that additional current through the data transformers.

➢ The 48-V PoE power is applied to the port circuit in accordance with the present 802.3af specification, except for the modified power and current limit thresholds.

➢ Signal integrity tests :

- Equipment connected in a loop-back configuration, with sourced data passed through the high-power port, across cable plants to the powered EVM/load, where the data is decoupled to pass back to the Smartbits card

- The packet error ratio estimation tests were then repeated at various DC load levels

- Tests were performed at 10 times the standard number of packet transfers, to replicate more of an endurance stress test.

- At each of the DC load levels, traffic was passed as 4,680,000 (64-byte) and 197,000 (1518-byte) packets, for a net transfer of nearly 300 million bytes for each case.

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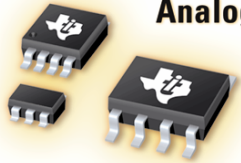
Limitations ofTest Setup

➢ Although millions of packets of data were transferred during testing, this still is a limited sample of devices

➢ All testing was done at room temperature

➢ These tests make no attempt to assess the suitability of CAT-5 cable for delivering power at greater than 350 mA DC in typical installations.

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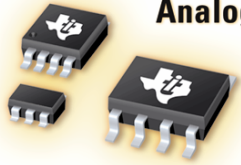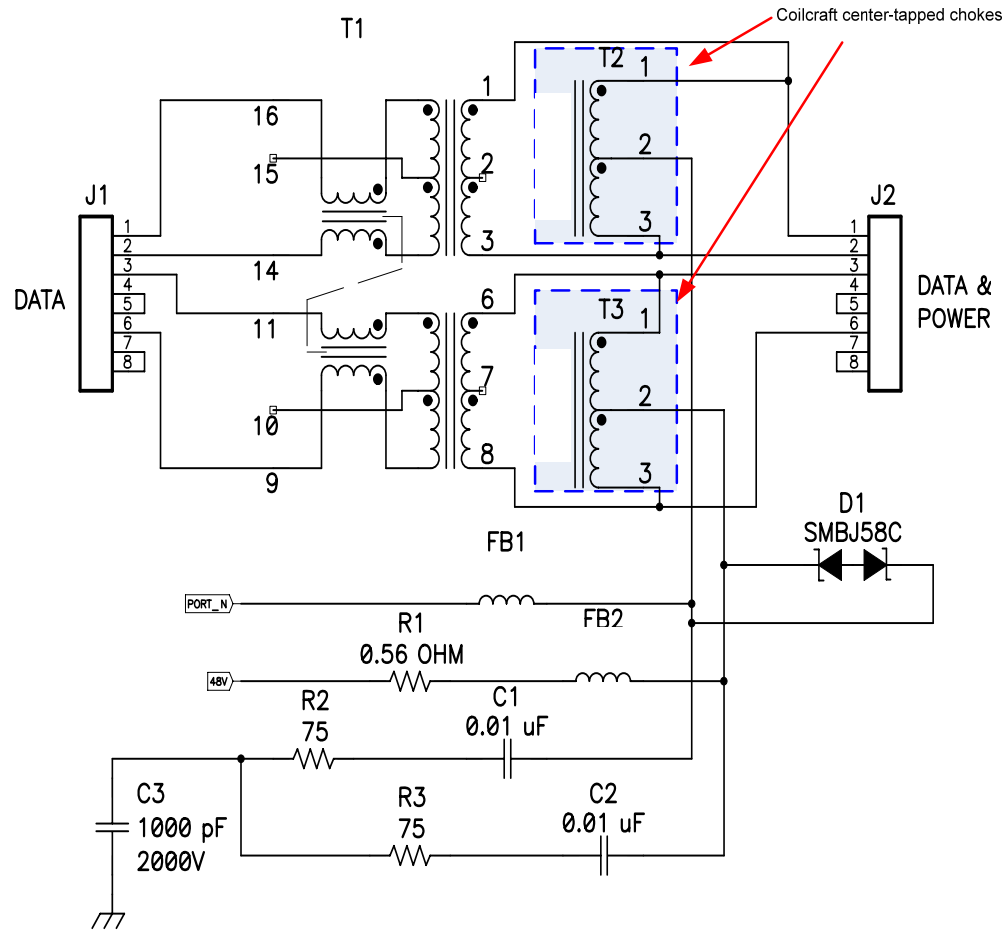
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Figure 2 : Center-Tapped Choke High-Power PSE Port Schematic

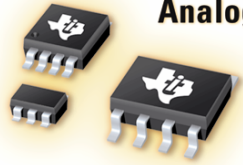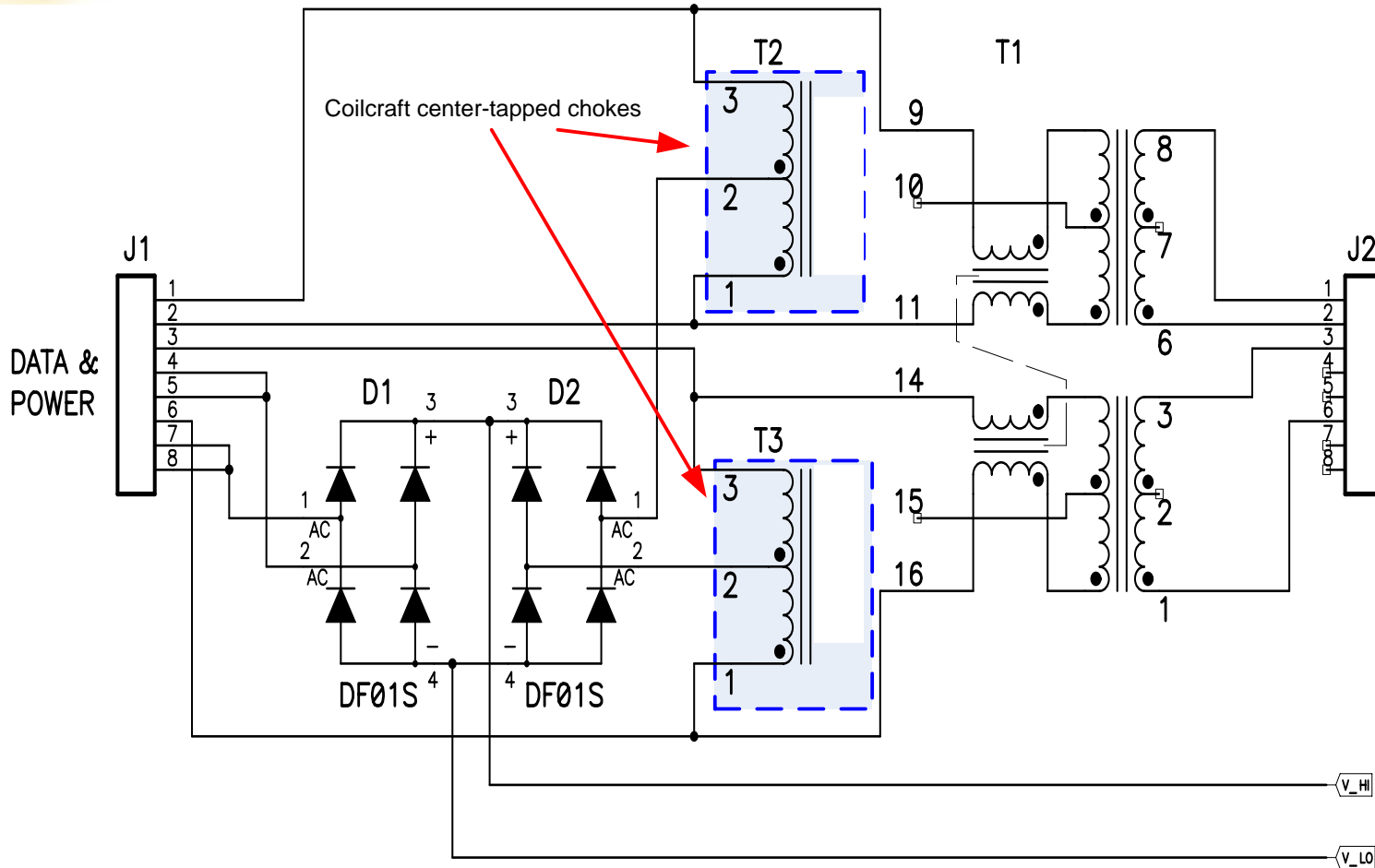**IEEE802.3af POE meeting January 2006 : High Power-over-Ethernet over Two Pairs**
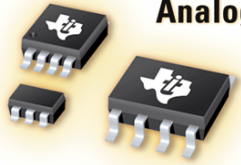
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Figure 3 : Center-Tapped Choke High-Power PD Input Circuit Schematic

Coilcraft center-tapped chokes

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Test results

➢ The CT transformer configuration worked successfully under all load conditions, with no discernable impact to data integrity, up to loads of 650 mA DC

➢ During all traffic pattern tests, the PSE DUT experienced <u>zero</u> packet errors, including when delivering at high power and over the long (high-attenuation) cable plant.

➢ These results suggest that the CT transformer configuration is a viable scheme for delivering higher DC power over the Ethernet signal pair.

➢ The measured current imbalance was 14.5mA. The test setup did not allow to change that current imbalance however. A tolerance to more than 20mA is recommended.
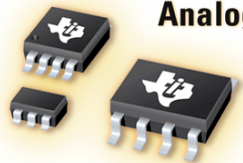
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Table 1. Endurance Stress Test – with Center-Tapped Choke, at 48V

	Endurance Stress (Data Pass-through) Test			
	High Attenuation Channel		Low Attenuation Channel	
PD Load Current	64 Byte	1518 Byte	64 Byte	1518 Byte
200 mA	0	0	0	0
300 mA	0	0	0	0
400 mA	0	0	0	0
500 mA	0	0	0	0
600 mA	0	0	0	0
650 mA	0	0	0	0

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