Power over 2 Pairs and 4 Pairs – Silicon Implementation Issues

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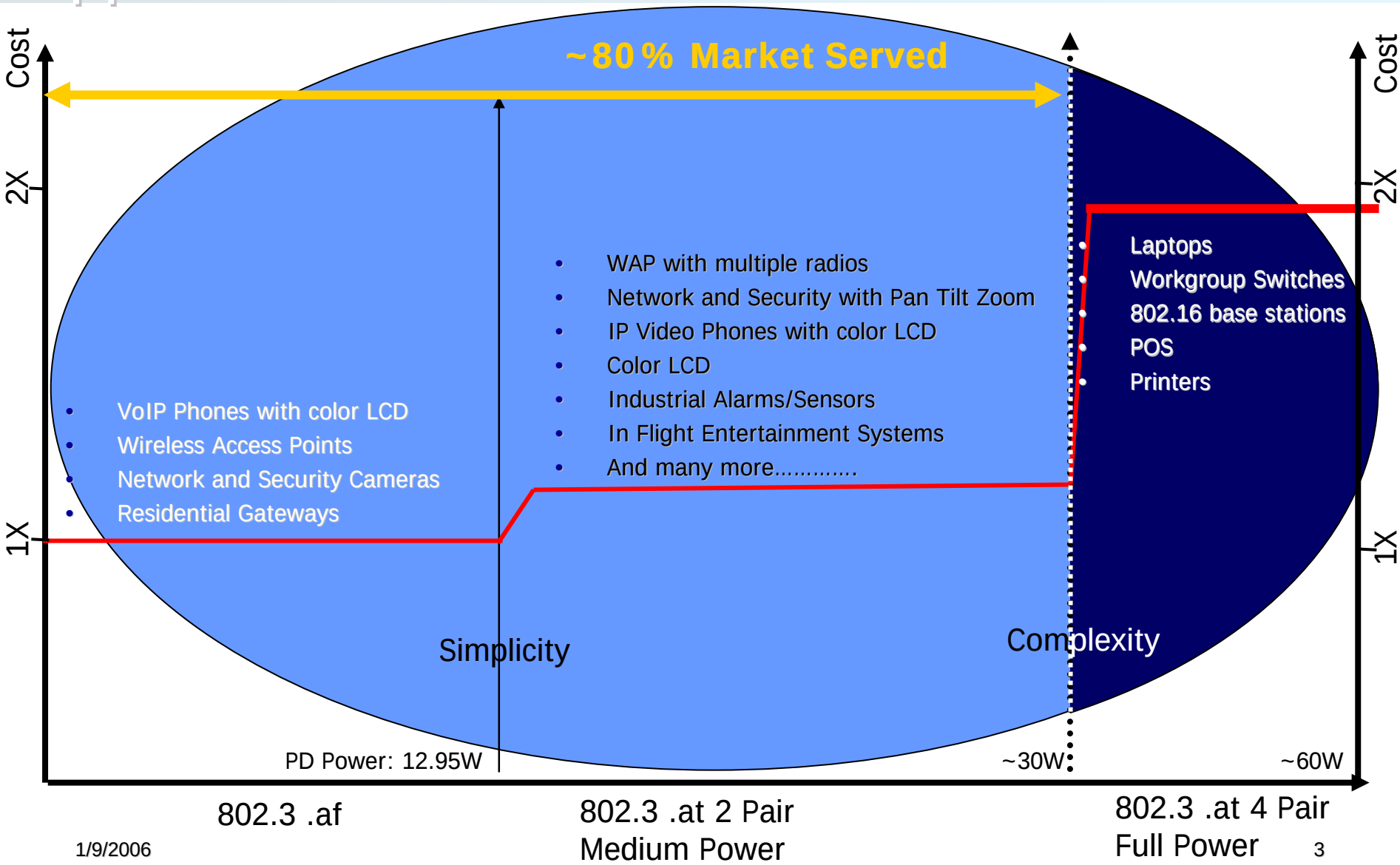
Agenda

- 2 Pair Medium Power Enables New Markets
- 2 pair implementation in silicon
- 4 pair implementation in silicon
- Conclusion and recommendations

2 Pair Medium Power Enables more Applications with lower cost



2 pair implementation in silicon

- Simpler PD or PSE Controller
  - Increasing current requirement from 350mA to 700mA
    - Marginal increase of silicon cost
- No change in signature resistor
  - Ping pong classification scheme reduces silicon overhead enabling multiple (>4) classes
- Linear change to power switch size (350mA – 700mA)
- No impact to DC-DC converter architecture
- Bottom Line: ~10% increase in system cost wrt .af

4 pair implementation in silicon

- Complicated PD or PSE controller
  - Complex current summing schemes to bridge power from 4 pairs
  - Large increase in silicon cost
- No change in signature resistor
  - Ping pong classification scheme reduces silicon overhead enabling multiple (>4) classes
- Major change to power switch size (350mA – 1,400mA)
- Impact to DC-DC converter
  - transformer and power MOSFET needs to handle 1.4A
- Bottom Line: expensive and complex solution for less than 30W apps
  - 180% increase in system cost wrt .af
  - Medium power applications carries cost overhead for 4P

Conclusion and recommendations

- 2 pair is simpler and cost effective to implement
- 4 pair is a more expensive solution due to current sharing
- Medium power applications should not be burdened with substantial costs for higher power applications

- Recommend
  - Extending 802.3af 2P to medium power
  - Add 4P for high power
  - Allow 2P only PSEs or 2P/4P PSEs