Magnetics for Higher DC Imbalance

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IEEE P802.3at
DTE Power Enhancements Task Force
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Topics

- 10/100/1000Base-T backward compatible
- Targeted 24mA and 34mA DC imbalance
- Electrical parameters measured:
  - Insertion loss, Return Loss, OCL with DC bias
- Component power dissipation and temperature rise
- Distortion of Insertion Loss and Return Loss with power applied
- Component size increase, single port and multi-port components

Schematic and Electrical Parameters

- 1000Base-T circuit used for backward compatibility
- Two pairs used for calculations, worst case scenario
- Tested with 700mA of current

ELECTRICAL CHARACTERISTICS

OCL @ 100kHz, 20mVRMs AND 24mA DC BIAS FROM 0°C TO 70°C
PAIRS (1-2), (3-6), (4-5) AND (7-8) 350µH MIN.

INSERTION LOSS, ALL PAIRS

0.1MHz TO 1MHz	-1.1 dB MAX
1MHz TO 65MHz	-0.5 dB MAX
65MHz TO 100MHz	-0.8 dB MAX
100MHz TO 125MHz	-1.4 dB MAX

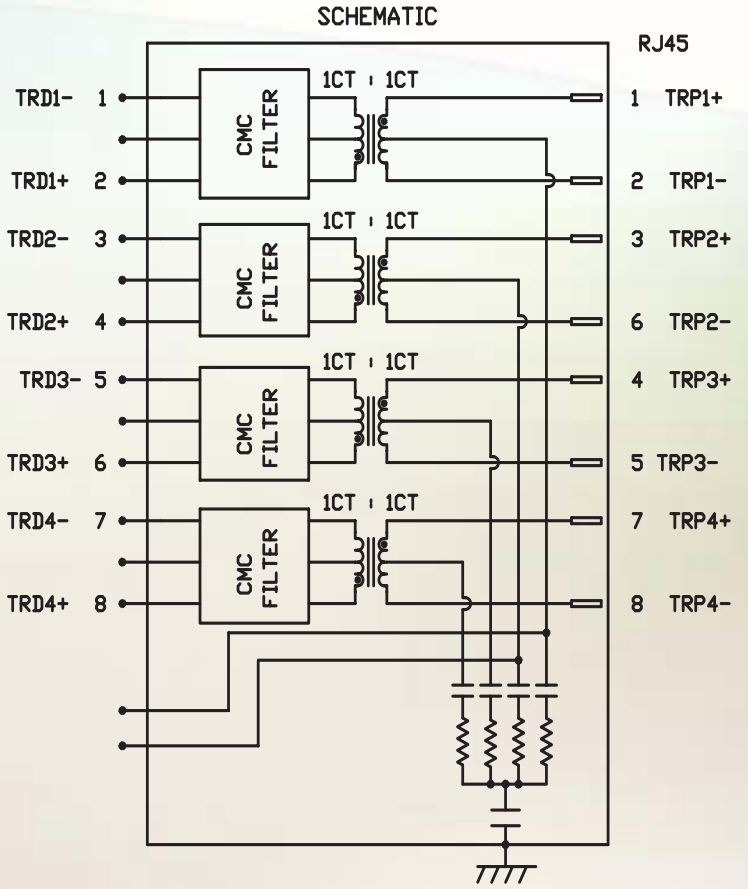
RETURN LOSS, ALL PAIRS (MIN)

0.5MHz-40MHz	-18 dB
40MHz-100MHz	-12+20LOG(f/80MHz) dB

HIPOT (Isolation Voltage, ALL PAIRS): 2250 VDC

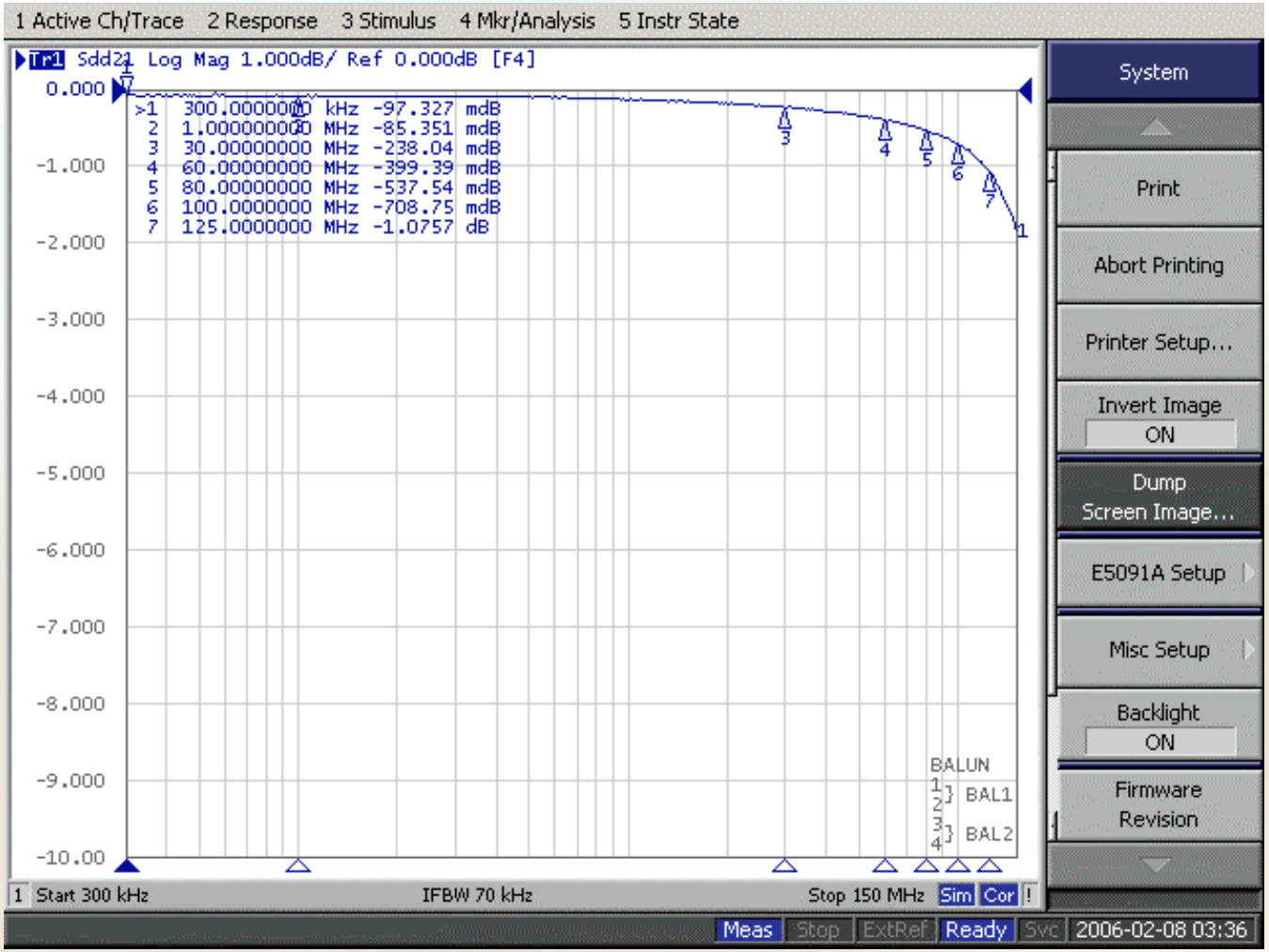
DCR PINS CABLE SIDE (1-2), (3-6),(4-5),(7-8):
1.0 OHMs MAX, .78 OHMs TYPICAL

BALANCED DC LINE CURRENT 700 mA.
@ 57 VDC CONTINUOUS
1.2 A MAX.
@ 57 VDC forSECOND



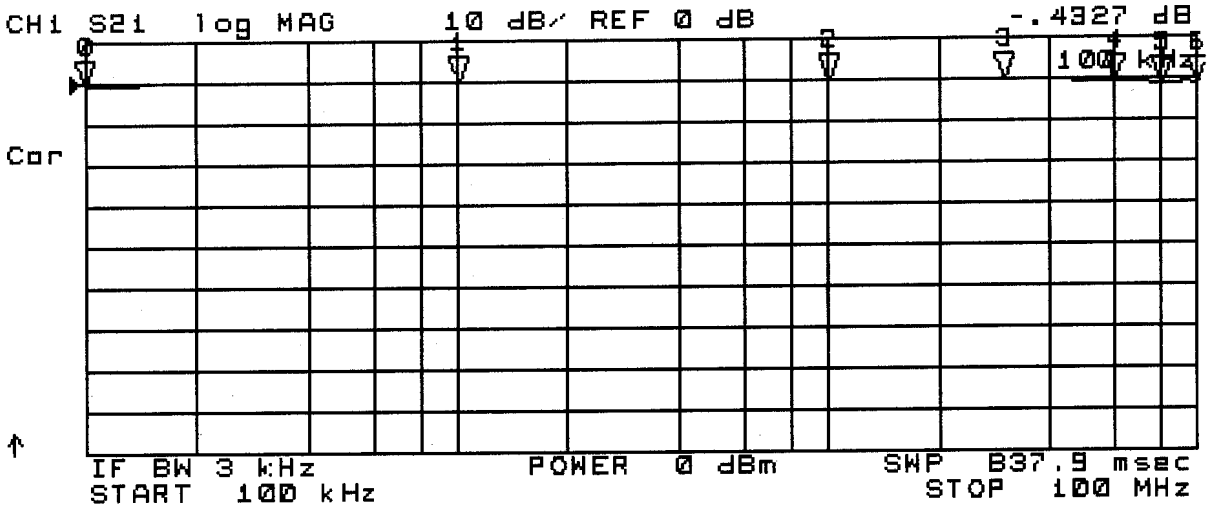
Insertion Loss

- Insertion Loss <u>without</u> 700mA of current applied to center tap of transformer



Insertion Loss

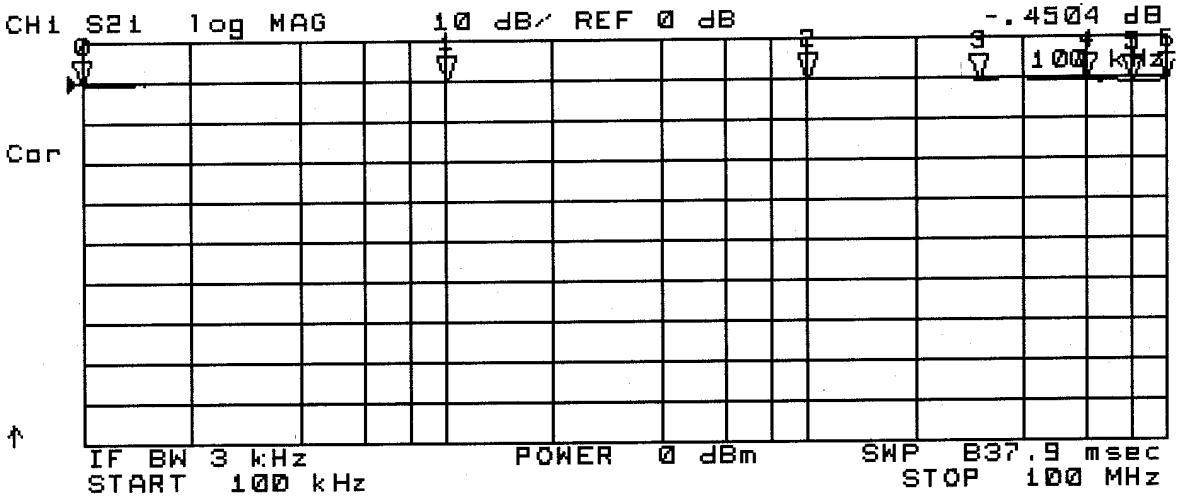
- Insertion Loss without 700mA
- Plot shows IL Test Fixture distortion



N	SWP PARAM	VAL
0	.100 kHz	-.4327 dB
1	1 MHz	-.1169 dB
2	10 MHz	-.1336 dB
3	30 MHz	-.2096 dB
4	60 MHz	-.5758 dB
5	80 MHz	-1.1247 dB
6	100 MHz	-.9801 dB

Insertion Loss

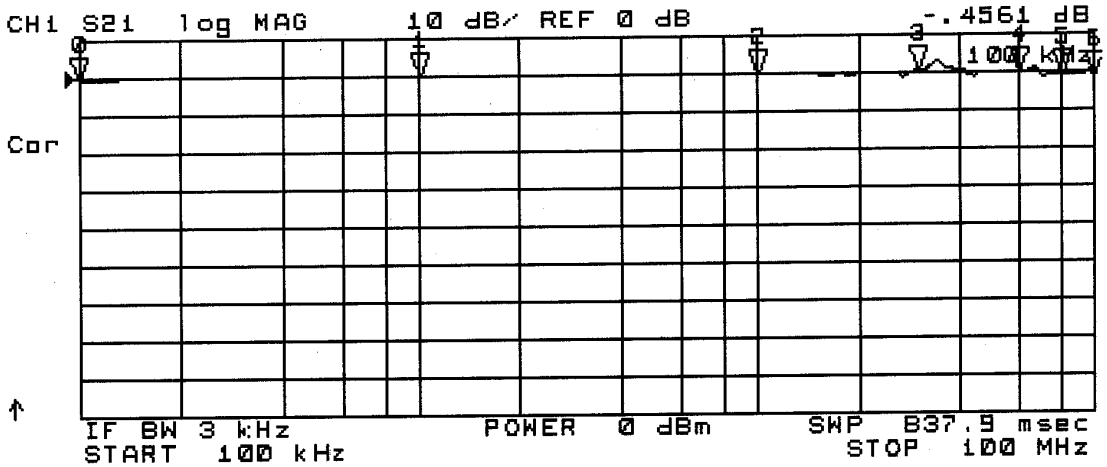
- Insertion Loss with 700mA



N	SWP PARAM	VAL
0	100 kHz	-.4504 dB
1	1 MHz	-.1006 dB
2	10 MHz	-.1201 dB
3	30 MHz	-.3317 dB
4	60 MHz	-.6859 dB
5	80 MHz	-1.1532 dB
6	100 MHz	-.8207 dB

Insertion Loss

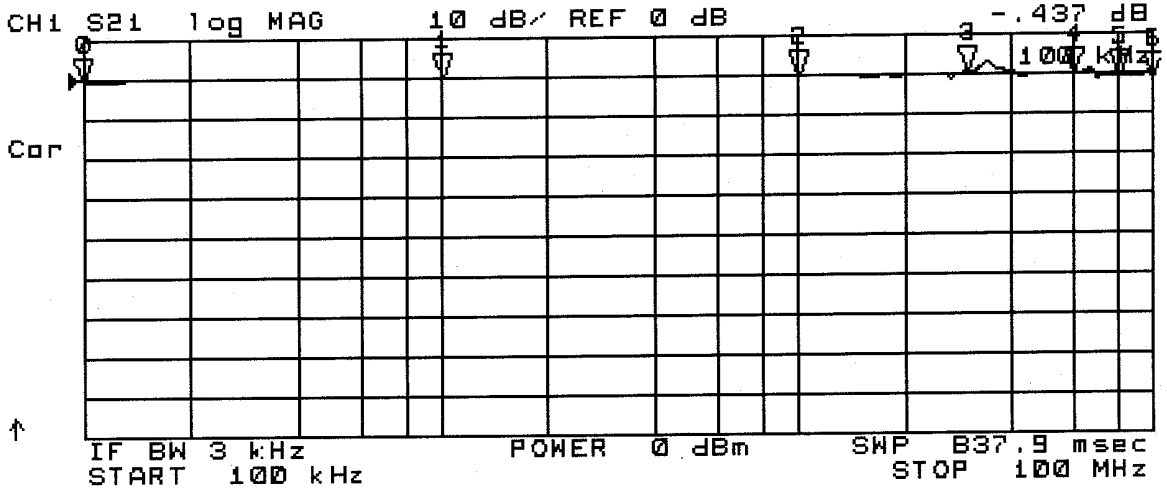
- Test circuit, no power
- Plot shows Imbalance Test Fixture distortion



N	SWP PARAM	VAL
0	100 kHz	-.4561 dB
1	1 MHz	.1432 dB
2	10 MHz	-.1834 dB
3	30 MHz	.4767 dB
4	60 MHz	.0128 dB
5	80 MHz	-.7329 dB
6	100 MHz	-1.4214 dB

Insertion Loss

- Insertion Loss with 26mA imbalance = 337 mA one leg, 363 mA other leg



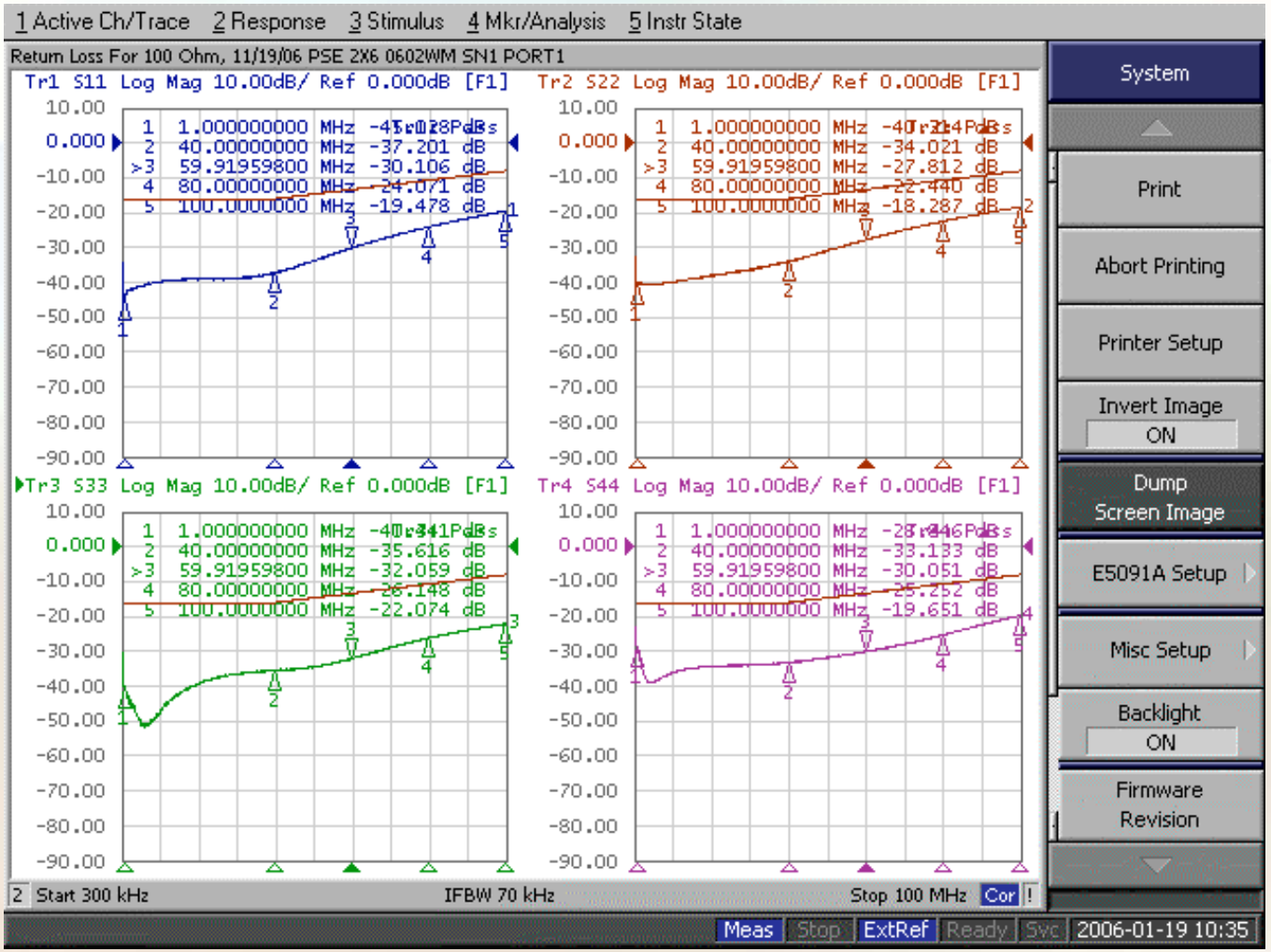
N	SWP PARAM	VAL
0	100 kHz	-.437 dB
1	1 MHz	.1434 dB
2	10 MHz	-.1799 dB
3	30 MHz	.4975 dB
4	60 MHz	.0304 dB
5	80 MHz	-.7074 dB
6	100 MHz	-1.4325 dB

Insertion Loss - Conclusions

- Insertion Loss does not distort with 700mA
- Insertion Loss does not degrade using magnetics for 24 mA imbalance design

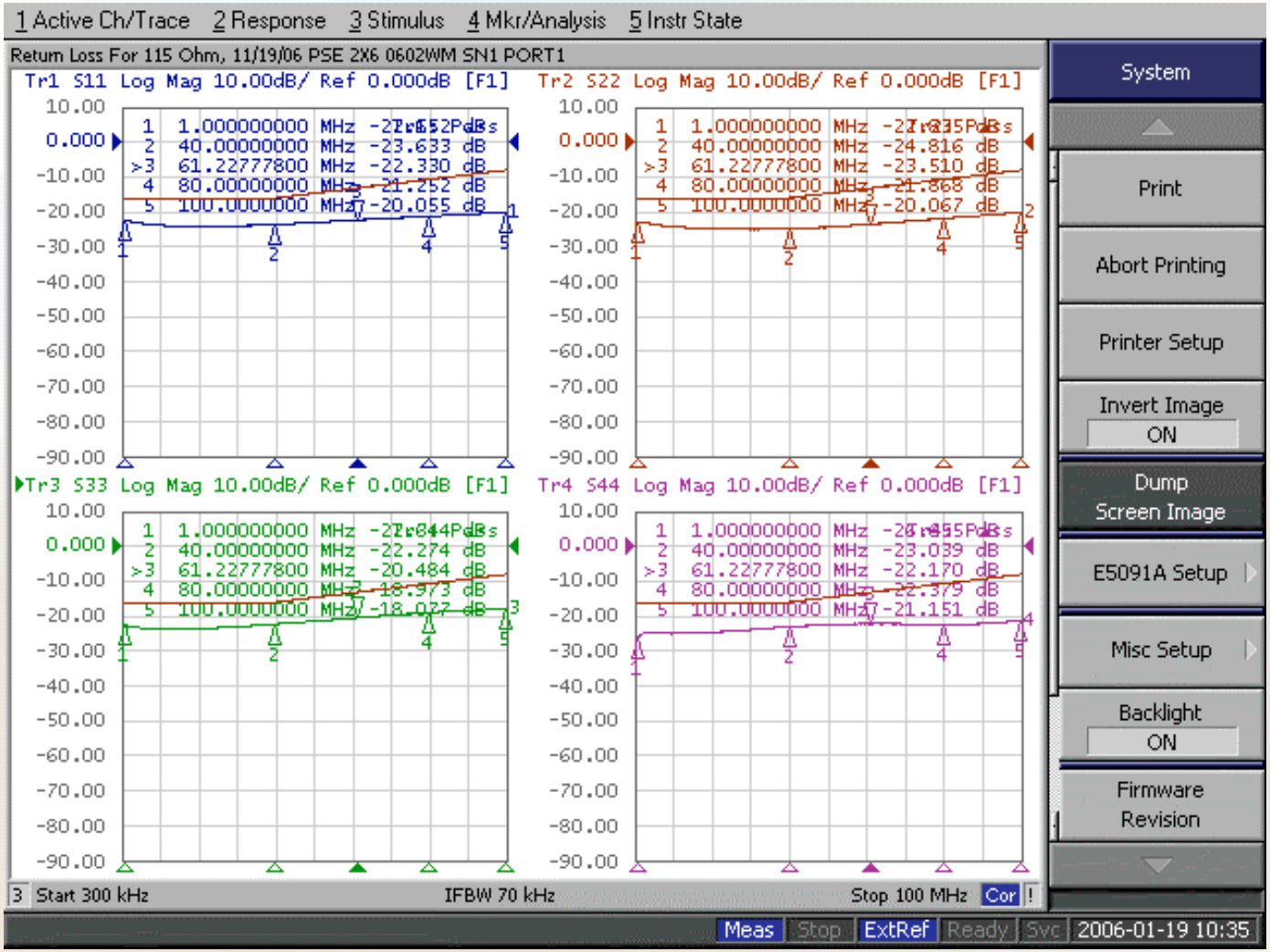
Return Loss

- Return Loss 100 Ohms without 700mA of current applied to center tap of transformer



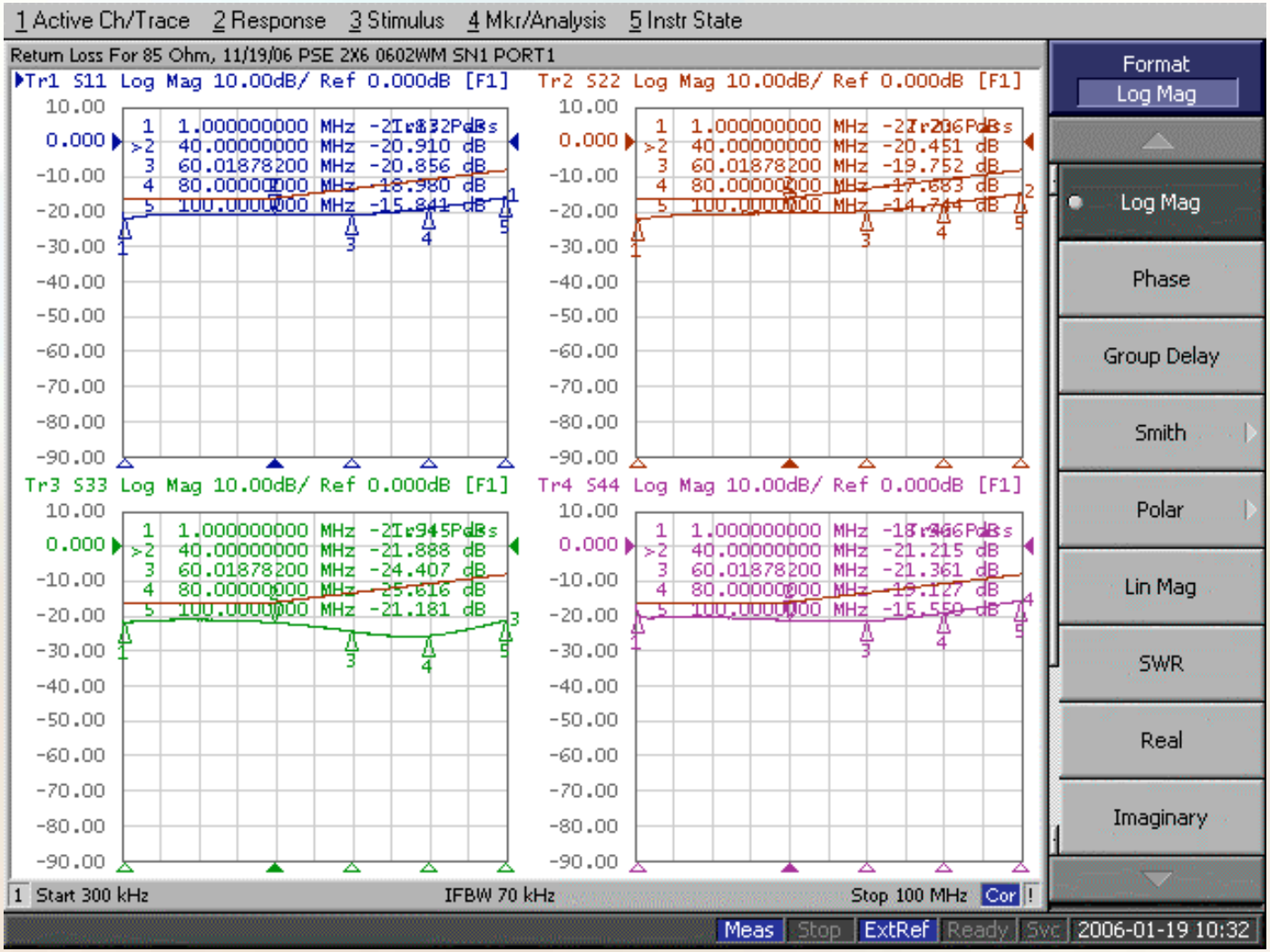
Return Loss

- Return Loss 115 Ohms without 700mA of current applied to center tap of transformer



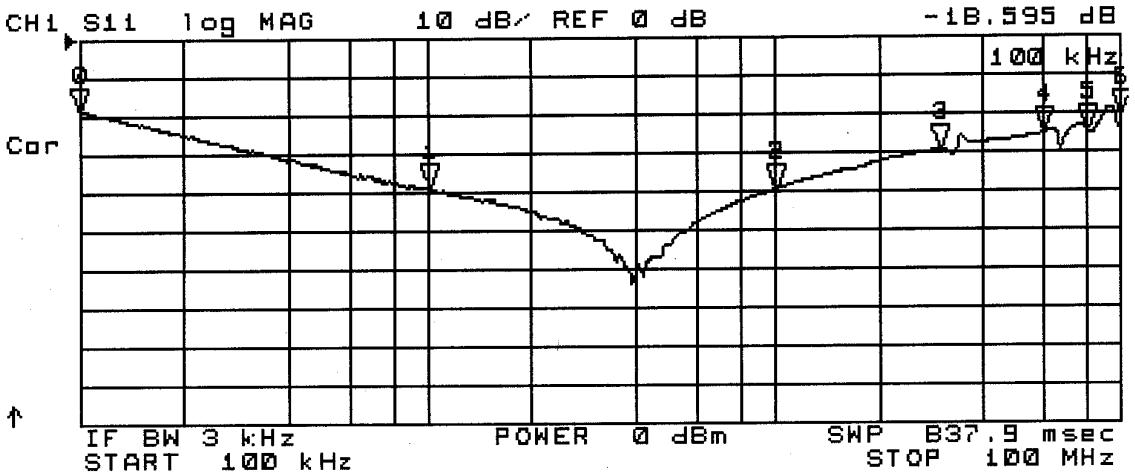
Return Loss

- Return Loss 85 Ohms without 700mA of current applied to center tap of transformer



Return Loss

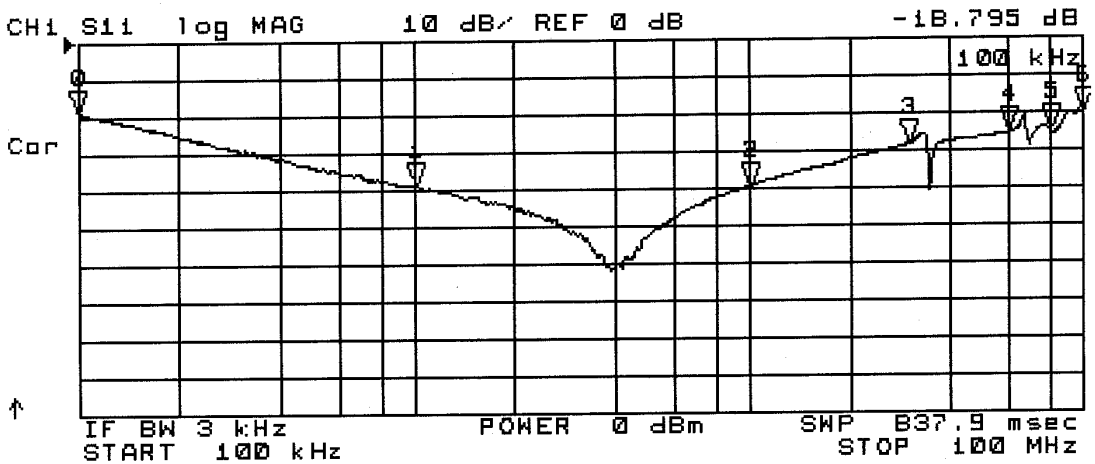
- Return Loss **without** 700mA, 100 Ohms
- Plot shows RL Test Fixture distortion



N	SWP PARAM	VAL
0	100 kHz	-18.595 dB
1	1 MHz	-38.974 dB
2	10 MHz	-39.594 dB
3	30 MHz	-29.524 dB
4	60 MHz	-25.052 dB
5	80 MHz	-24.188 dB
6	100 MHz	-20.729 dB

Return Loss

- Return Loss with 700mA, 100 Ohms
  - 85 Ohms and 115 Ohms are the same with and without 700mA



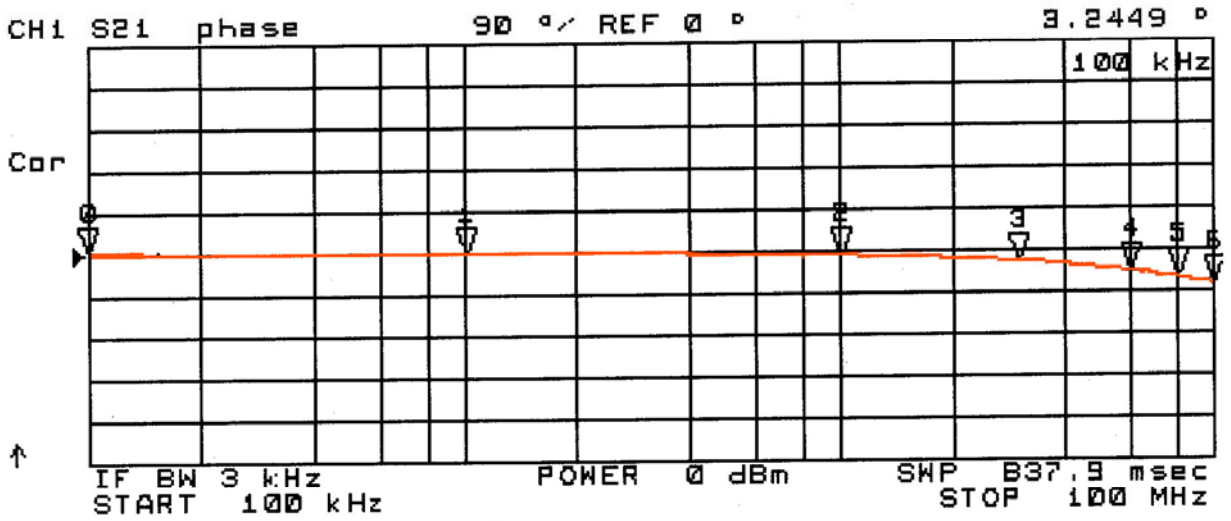
N	SWP PARAM	VAL
0	100 kHz	-18.795 dB
1	1 MHz	-39.006 dB
2	10 MHz	-39.375 dB
3	30 MHz	-28.148 dB
4	60 MHz	-25.173 dB
5	80 MHz	-24.666 dB
6	100 MHz	-19.746 dB

Return Loss - Conclusions

- Return Loss does not distort with 700mA
- Return Loss does not degrade using magnetics for 24 mA imbalance design
- Return Loss still meets IEEE 802.3 10/100/1000Base-T specifications

Phase

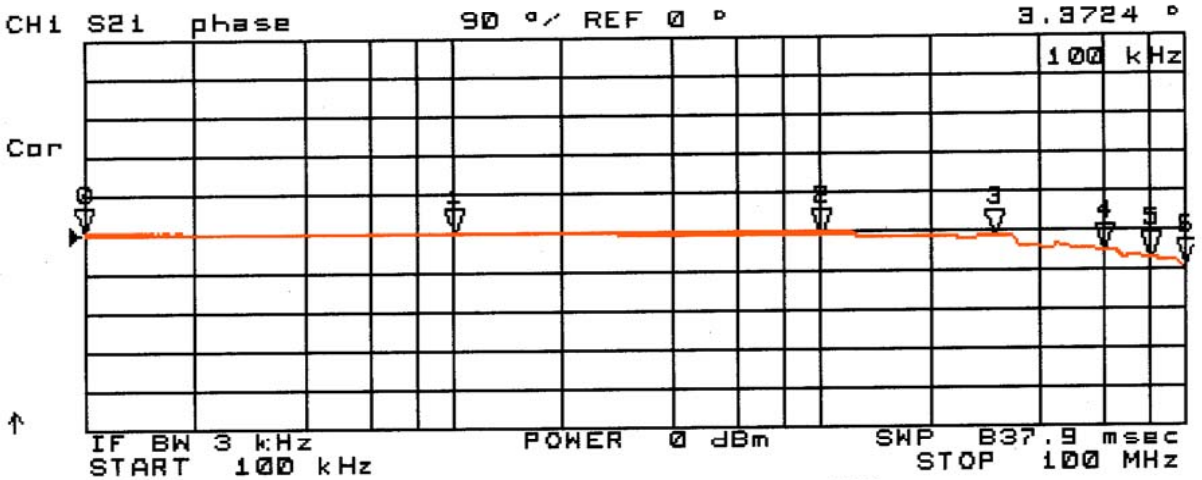
- Phase with 700mA of current applied to center tap of transformer



N	SWP PARAM	VAL
0	100 kHz	3.2449 °
1	1 MHz	-394.08 m°
2	10 MHz	-7.5163 °
3	30 MHz	-22.607 °
4	60 MHz	-44.644 °
5	80 MHz	-58.398 °
6	100 MHz	-73.911 °

Phase

- Phase with DC imbalance of 26mA
- Conclusion: Phase does not distort with 700mA



N	SWP PARAM	VAL
0	100 kHz	3.3724 °
1	1 MHz	203.18 m°
2	10 MHz	-6.9501 °
3	30 MHz	-11.871 °
4	60 MHz	-44.964 °
5	80 MHz	-61.515 °
6	100 MHz	-79.82 °

OCL

- 24mA design over temperature with bias
- Designed for 50µH of margin

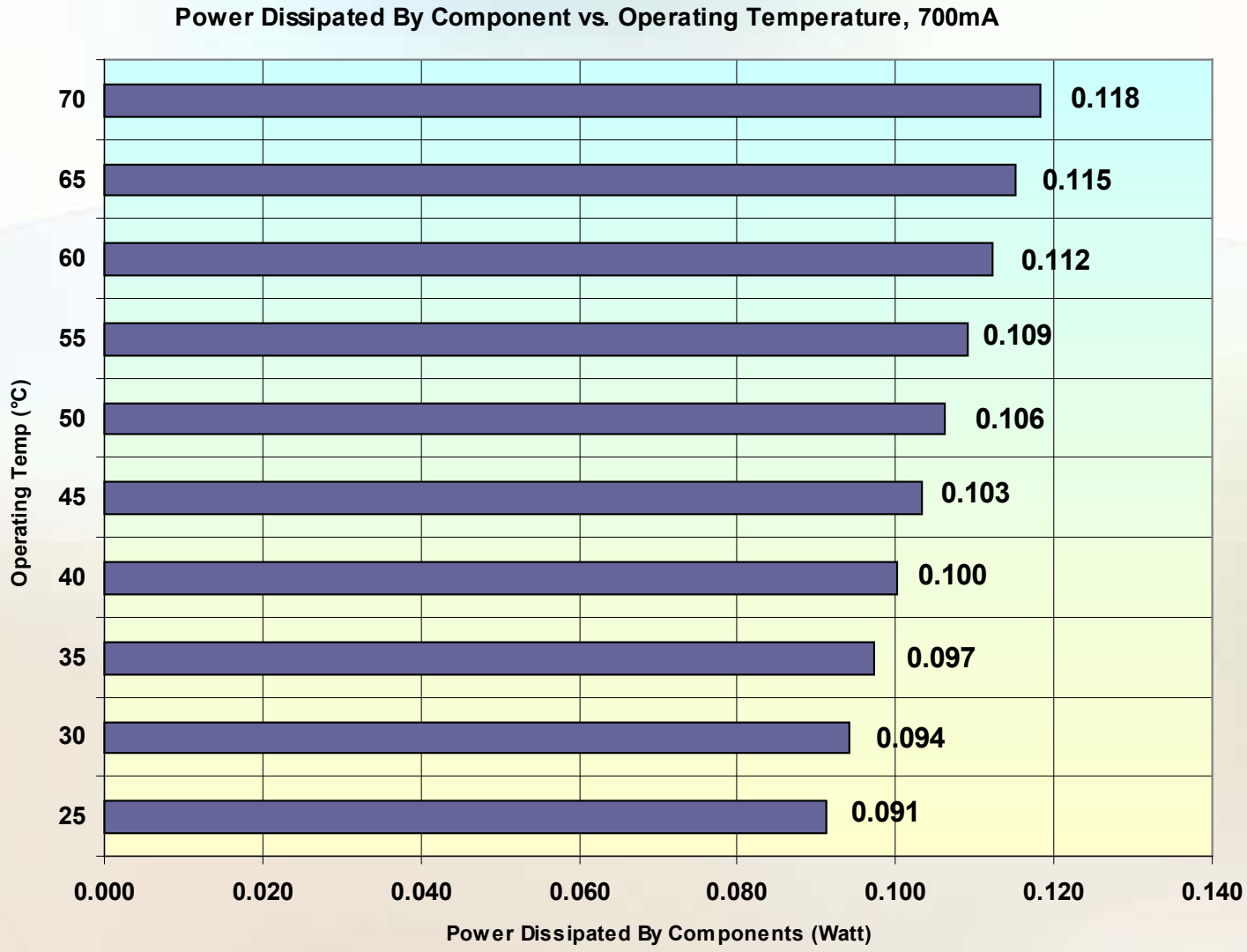
24mA Design	OCL 20mA µH	OCL 21mA µH	OCL 22mA µH	OCL 23mA µH	OCL 24mA µH	OCL 25mA µH	OCL 26mA µH
0° C	535	523	516	508	495	490	483
25° C	628	617	606	593	580	566	552
70° C	521	499	473	446	421	398	377

OCL

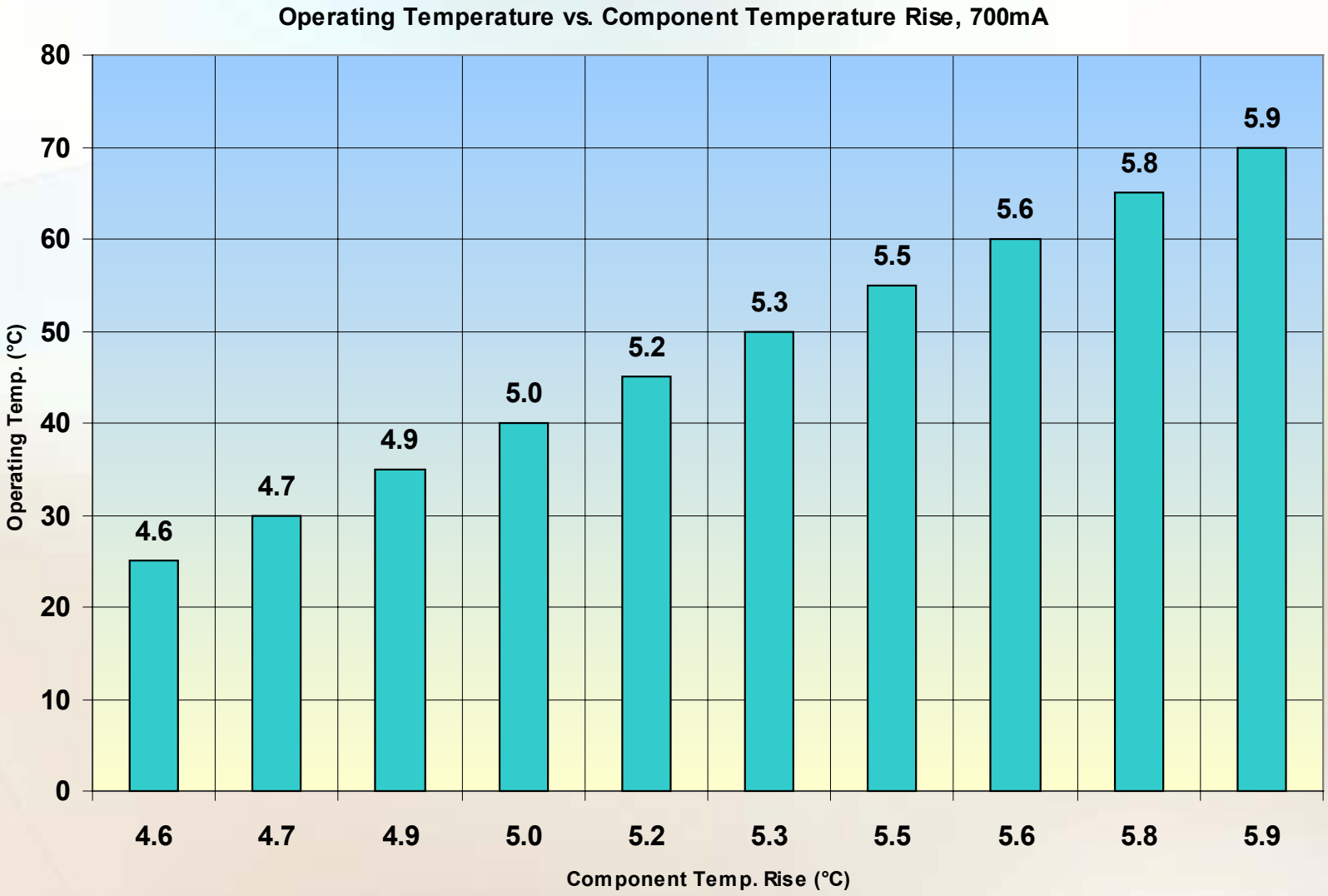
- 34mA design over temperature with bias
- Designed for 50µH of margin

34mA Design	OCL 30mA µH	OCL 31mA µH	OCL 32mA µH	OCL 33mA µH	OCL 34mA µH
0° C	760	727	690	675	668
25° C	935	886	837	789	743
70° C	521	448	463	424	405

Component Power Dissipation vs. Temperature, Calculated



Component Temperature Rise vs. Operating Temperature, Calculated



Component Temperature Rise vs Operating Temperature Measured

- Measured temperature rise of component using 800mA, probe molded into center of magnetics winding area
- Minimal rise seen using 700mA, so increased to 800mA

DC Bias / Operating Temperature	0mA	800mA	Temperature Rise
0° C	0.5° C	2.4° C	1.9° C
25° C	25.1° C	27.7° C	2.6° C
70° C	69.4° C	72.3° C	2.9° C

Component Size Increase
Depth Only

Description	% Increase	
	24mA	34mA
Single port, 10/100Base-T	0%	0%
Single port, 10/100/1000Base-T	15%	20%
Multi-port, 10/100Base-T	0%	0%
Multi-port, two-pair, 10/100/1000Base-T	10%	20%

Conclusions

- 1000Base-T backward compatible magnetics are capable of supporting 24mA of DC bias
- Distortion with DC bias is not an issue
- Temperature rise is ~ 6° C when operating at 70° C and applying 800mA of current per port

Future Work

- Different circuit topologies need to be tested
- 1000Base-T backward compatible magnetics are capable of supporting 34mA of DC bias but require further test validation. Insertion Loss, Return Loss and different circuits topologies.

Thank you for your time