Worst-Case Analysis of PoE System Efficiency

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Overview

- One of the biggest costs in a PSE is the cost of the main power supply.
- Presently, the main PS is oversized in many systems because a lot of power is wasted in various ways.
- If waste could be reduced, we may be able to significantly reduce the size of the main PS, and thus the cost of a PSE system.
- This document seeks to:
  - Analyze the various ways that power is wasted.
  - Suggest ways to reduce these waste factors.
  - Estimate the resulting PSE system cost savings.

What is "Wasted Power"?

- Normally in power electronics we talk about efficiency and losses.
- The term "loss" traditionally refers to energy that is converted to heat. To avoid confusion, we'll stick with that definition.
- But in PoE systems, losses are only part of the inefficiency: Most of the waste is caused by margining, and protocol limitations.
- Definition: Wasted power, is power within the capacity of the PSE to provide, but it can't actually be used by the PDs for some reason.
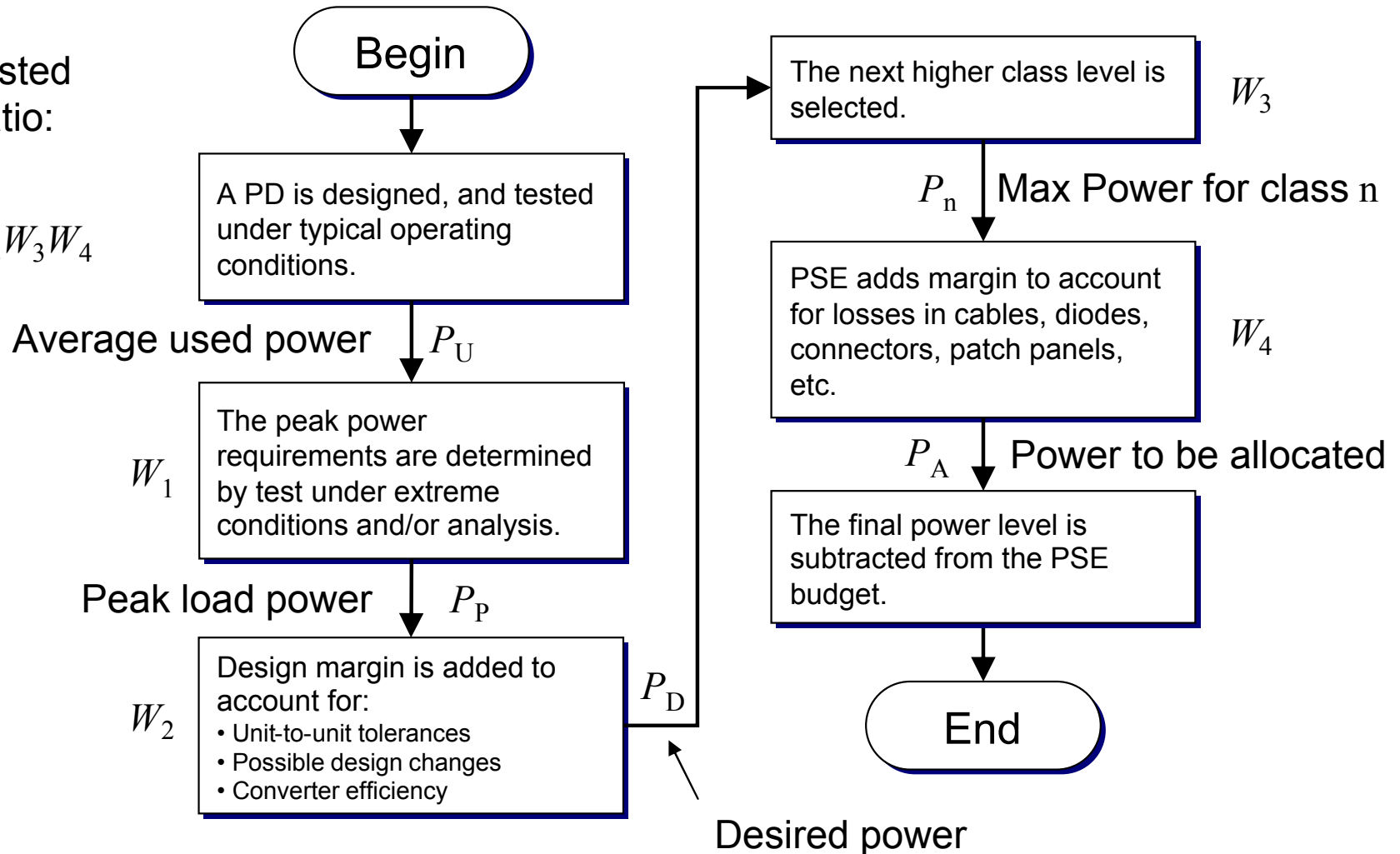
Where Does All the Power Go?

- First, let's define "wasted power ratio", denoted as W.
  - The ratio of power <u>allocated</u> from PSE budget (P_A), to power actually <u>used</u> by PD (P_U).
  - $W=P_A/P_U$ (Note: W is the reciprocal of *Power Utilization.*)
  - For the purpose of this analysis, P_U is the average power output from the converter inside the PD under typical operating conditions.
- Power is wasted in four ways ($W=W_1 W_2 W_3 W_4$):
  - W_1: Requesting peak power rather than average.
  - W_2: Adding PD design margin.
  - W_3: Waste due to finite classification granularity.
  - W_4: Margin for losses in components (including cables).
- Each of these terms is explained in detail later.

Modeling The Waste Process

Total wasted
power ratio:

$$P_A = WP_U$$
$$W = W_1 W_2 W_3 W_4$$

Begin

A PD is designed, and tested under typical operating conditions.

Average used power $\downarrow P_U$

W_1 | The peak power requirements are determined by test under extreme conditions and/or analysis.

Peak load power $\downarrow P_P$

W_2 | Design margin is added to account for:
• Unit-to-unit tolerances
• Possible design changes
• Converter efficiency

P_D

The next higher class level is selected. | W_3

P_n | Max Power for class n

PSE adds margin to account for losses in cables, diodes, connectors, patch panels, etc. | W_4

P_A | Power to be allocated

The final power level is subtracted from the PSE budget.

End

Desired power

Some Key Points

- The expression for W is the *product* of 4 factors, not the *sum* of 4 terms.
  - We may not know how big W_1 is, but we do know that a 10% reduction in either W_3 or W_4 will result in a 10% reduction of W.
  - We don't need to know W_1 or W_2. It is possible to reduce the cost of PSE by working with just W_3 and W_4.
- All 4 factors are examined here for the sake of completeness, but the emphasis is on W_3 and W_4.

W_1: Peak vs. Average Power

- This is definitely the biggest waste of power, and the most difficult to prevent or even predict.

- Example: A PD uses 2W on average (P_U=2), but can draw up to 10W during occasional peaks (P_P=10). Then W_1=5.

- Possible ways to reduce W_1: None for L1.
  - We can't change the protocol to use average instead of peak power.
    - Not backward-compatible with 802.3af
    - Could lead to over-committing of the main PS.
  - The issue is best handled with a Layer 2 protocol, which would allow dynamic negotiation and reallocation. (Outside the scope of this presentation.)

W_2: PD Design Margin

- This is probably the second largest waste of power.
- Example: You design a PD and your prototype draws 10W at peak load. (P_P=10W.) But you shouldn't request only 10W, you need some margin:
  - There will be unit-to-unit variations.
  - Converter efficiency must be considered.
  - There may be new features, field upgrades, or bug fixes that increase peak power.
  - You decide to set P_D=12.5W (for 25% margin). Then W_2=1.25.
- Possible ways to reduce W_2:
  - If the PD controller chips encoded the class signature in EEPROM instead of fixed resistors, then PD designers would probably be comfortable with smaller margins.
  - Could the task force establish guidelines or recommendations for minimum converter efficiency?

W_3: Classification Granularity

- This was a huge waste of power for 802.3af, but will (hopefully) be much less in 802.3at.
- Example:
  - Suppose a Af-PD requires 6.5W peak.
  - This falls within the range of Class 3. (Table 33-10)
  - The PSE must allocate 15.4W for a Class 3 PD. (Table 33-3)
  - $W_3 W_4 = P_A / P_D = 15.4/6.5 = 2.37$.
  - Assume $W_4 = 1.15$ in this case (see page 17).
  - Then $W_3 = 2.37/1.15 = 2.06$
  - Therefore 51% of the allocated power is wasted due to class granularity alone.
- Possible ways to reduce W_3:
  - Increase class granularity.
  - Use an exponential curve (see page 11).

W_3: Worst-Case Analysis

- $W_3=P_n/P_D$ where P_n is the upper end of the power range of class n. The worst-case is when $P_D=P_{n-1}$. Therefore we use $W_3=P_n/P_{n-1}$. Let N be the number of classes, and n=\{1,..,N\}.

- The function $P_n(n)$ has a great impact on the analysis.
  - □ If we choose a <u>linear</u> curve then,

$$P_n = \frac{(n-1)P_{MAX} + (N-n)P_{MIN}}{(N-1)} \quad \Rightarrow \quad W_3(n) = \frac{(n-1)P_{MAX} + (N-n)P_{MIN}}{(n-2)P_{MAX} + (N-n+1)P_{MIN}}$$

  - □ If we choose a <u>exponential</u> curve then,

$$P_n = P_{MIN}\left(\frac{P_{MAX}}{P_{MIN}}\right)^{(n-1)/(N-1)} \quad \Rightarrow \quad W_3 = \left(\frac{P_{MAX}}{P_{MIN}}\right)^{1/(N-1)}$$

  - □ Both curves have end-points $\{1, P_{MIN}\}$ and $\{N, P_{MAX}\}$.

W_3: Comparison of Curves

- Example: Let N=30, P_{MIN}=2W, and P_{MAX}=100W.
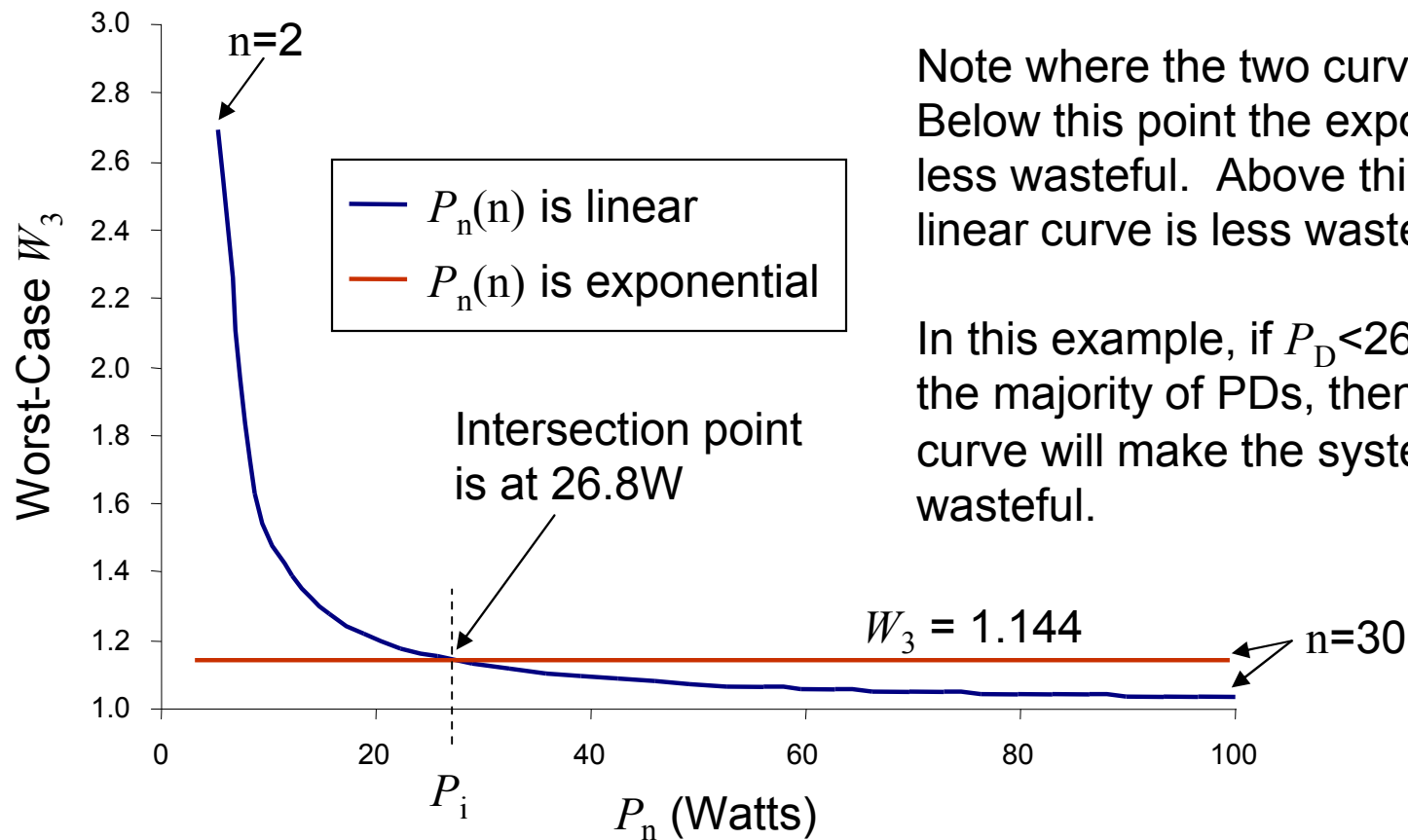
Note where the two curves intersect. Below this point the exponential curve is less wasteful. Above this point, the linear curve is less wasteful.

In this example, if P_D<26.8W is true for the majority of PDs, then the exponential curve will make the system less wasteful.

W_3: Cost Analysis

- **Definition of variables**
    - C_{SYS}=Total cost of manufacturing a Af-PSE (including test).
    - C_{TEST}=Cost of testing a Af-PSE (PoE and non-PoE tests).
    - C_{PS}=Cost of main power supply inside PSE.
    - N_{TEST}=Total number of test cases presently performed for Af-PSE.
    - N_{CLASS}=Number of test cases needed to verify functionality associated with all Af class signatures. (Classes 0, 1, 2, and 3.)
- **Cost models (in terms of % of total system cost)**
    - Added cost of additional testing resulting from N class signatures.

$$\Delta C_{TEST} = \left(\frac{C_{TEST}}{C_{SYS}} \right) \left(\frac{N_{CLASS}}{N_{TEST}} \right) \left(\frac{N}{4} - 1 \right)$$

    - Cost savings from reducing main PS size, enabled by smaller W_3.

$$\Delta C_{PS} = \left(\frac{C_{PS}}{C_{SYS}} \right) \left(1 - \frac{W_3}{2.06} \right)$$

Note: 2.06 is the worst-case W_3 for Af-PSE Class 3 (See page 9).

W_3: Cost Analysis (Continued)

Assumptions: P_{MAX}=100W, P_{MIN}=2W, curve is exponential. $\left(\dfrac{N_{CLASS}}{N_{TEST}}\right) = 5\%$

Savings= $\Delta C_{PS} - \Delta C_{TEST}$ N_{OPT}=Optimal number of classes

N_{OPT}/Savings		C_{TEST}/C_{SYS}			
		5%	10%	15%	20%
C_{PS}/C_{SYS}	60%	47/25.6%	33/23.5%	28/21.8%	24/20.5%
	50%	42/20.9%	31/19.0%	25/17.5%	22/16.3%
	40%	37/16.3%	28/14.6%	23/13.2%	20/12.1%
	30%	33/11.7%	24/10.2%	20/9.1%	18/8.2%

Example: C_{PS}/C_{SYS}=50%, C_{TEST}/C_{SYS}=10% $\Rightarrow$ N_{OPT}=31, Savings=19%

W_4: Passive Losses

- This will probably be the third largest waste of power (assuming class granularity is improved over 802.3af).
- Define "passive" losses to include:
  - Resistive losses in cables, connectors, patch panels, FETs, current-sense resistors, transformers, etc.
  - Diode drops.
  - If Active Current Sharing (ACS) is adopted, there will be some additional losses in 4P systems. (See next slide.) But this might be unavoidable to achieve the highest power.
- Possible ways to reduce W_4:
  - Use 4P power feeding.
    - If the PSE can sense that 4 pairs are present and going to the same PD, then it can reduce the margin.
  - Provide a good worst-case analysis so that we don't overestimate these losses, and take too much margin.

W_4: Passive Losses (continued)

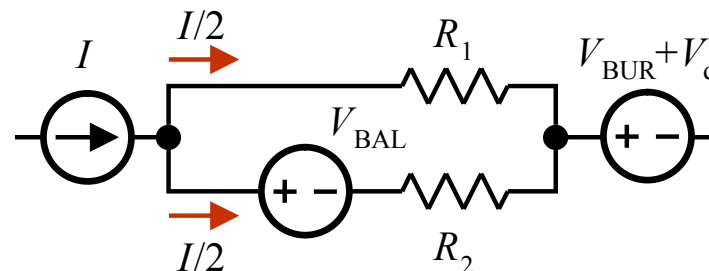- ## How would ACS affect the "passive" losses in 4P?

Without ACS
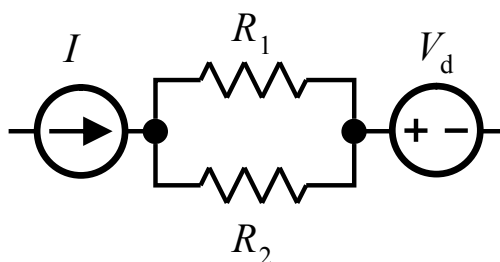
$$P_{L1}=I^2(R_1\|R_2) + IV_d$$

$$P_{L1}=I^2R_1R_2/(R_1+R_2) + IV_d$$

With ACS

$$P_{L2}=(I/2)^2(R_1+R_2) + (I/2)V_{BAL} + I(V_{BUR}+V_d)$$

$$V_{BAL}=(I/2)(R_1-R_2)$$

$$P_{L2}=I^2R_1/2 + I(V_{BUR}+V_d)$$

R_1, R_2= Resistance of one pair, including connectors, transformers, etc.

V_d = Total diode drops in one side of the circuit.

V_{BAL} = Differential voltage impressed by ACS circuit to balance the currents.

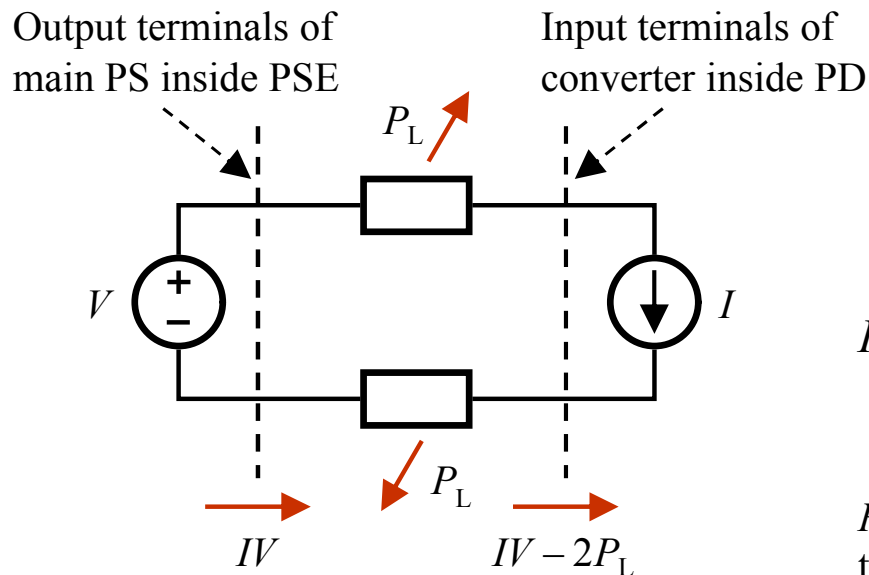V_{BUR} = Common-mode burden associated with non-ideal ACS circuit.

Let's define a ratio representing the extra losses associated with ACS:

$$\eta = \frac{P_{L2}}{P_{L1}}$$

Let $R_1=R+\Delta R/2$, $R_2=R-\Delta R/2$. Assume $R>>\Delta R$ so $R_1R_2\approx R^2$. Then,

$$\eta \approx \frac{I(R+\Delta R/2) + 2(V_{BUR}+V_d)}{IR + 2V_d}$$

W_4: Passive Losses (continued)

Output terminals of
main PS inside PSE

Input terminals of
converter inside PD

$$W_4 = \frac{IV}{IV - 2P_L}$$

P_L

V $+$ $-$

I

P_L

IV

$IV - 2P_L$

$$P_L = \begin{cases} I^2R + IV_d & \text{2P PSE} \\ I^2R/2 + IV_d & \text{4P PSE without ACS} \\ (I^2R/2 + IV_d)\eta & \text{4P PSE with ACS} \end{cases}$$

R = Sum of all resistance in one pair, including connectors, transformers, FETs, current-sense resistors, etc.

Note: These equations are looking at one PSE port and one PD. Any resistance term that is common to multiple PSE ports (for example, PS output resistance) must be treated separately. This issue was neglected here for simplicity.
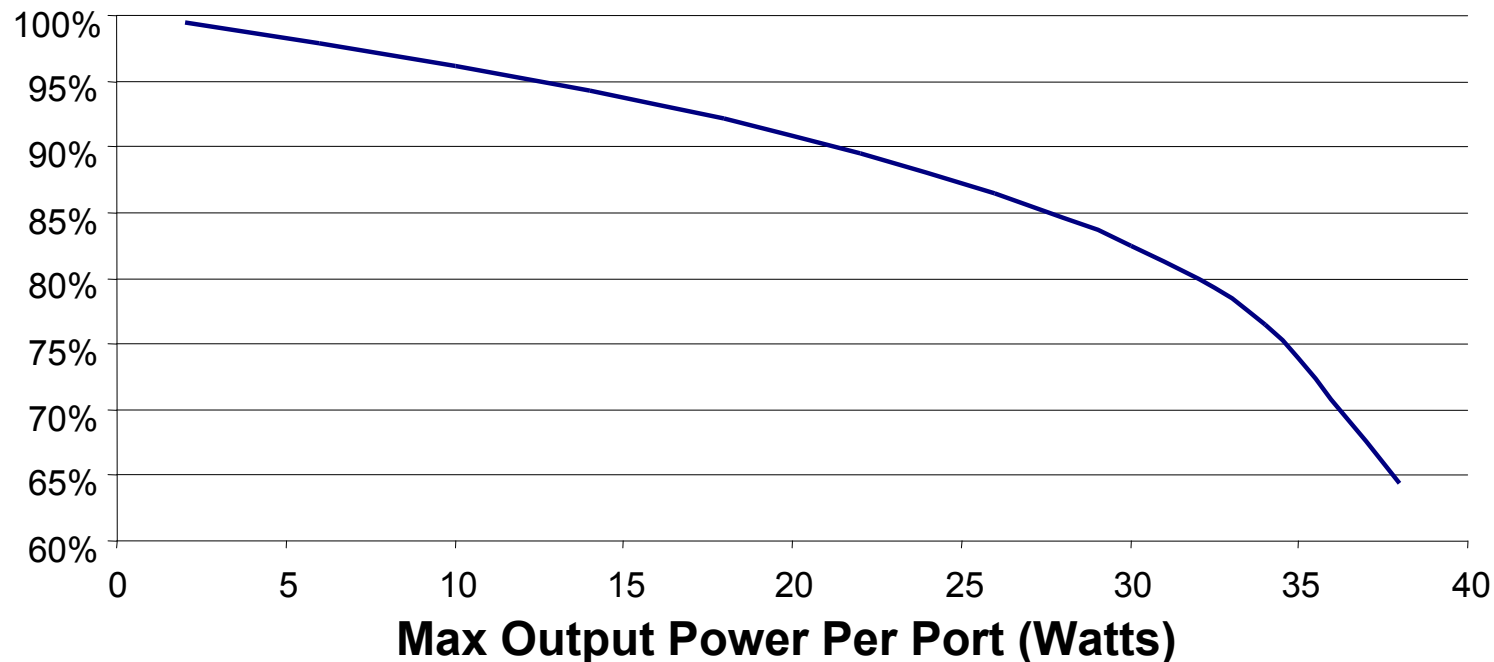
W_4: Waste Estimates
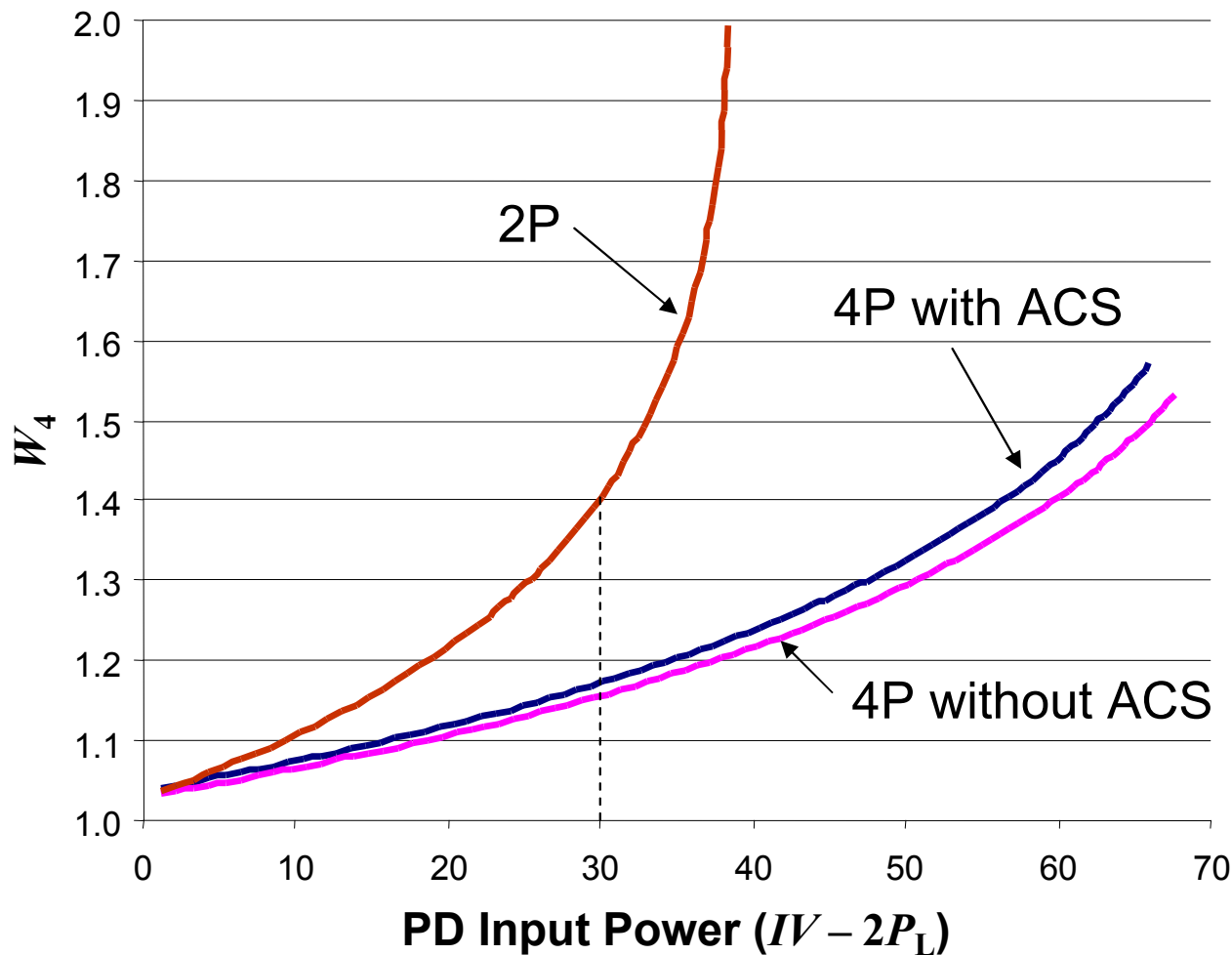
ASSUMPTIONS

- V = 57V (PSE bus)
- R = 10Ω/Pair (one way)
  - □ 9.5Ω for 100m CAT-3
  - □ 0.5Ω for other stuff
- $\Delta R = 0.03R$
- V_{d} = 0.8V
- V_{BUR} = 0.2V

Plot labels: 2P, 4P with ACS, 4P without ACS

Y-axis: W_4 (1.0 to 2.0)

X-axis: PD Input Power ($IV - 2P_{L}$) (0 to 70)

W_4: 2P vs. 4P Cost Analysis

- Required size of Main PS for 4P (without ACS) as a percent of size required for 2P.
  - Example: For 35W/port the PS can be 26% smaller for 4P vs. 2P.

NOTE: This is just the cost reduction of the main PS, and does not take into account the other costs associated with 4P such as extra FETs, etc.

Conclusions

- Since the cost of the main power supply is a large portion of the overall PSE system cost, reducing wasted power can potentially result in a significant cost reduction.

- Increasing the granularity of classification may result in approx 10% to 20% cost savings.
  - The optimal power curve seems to be exponential up to approx 27W, and linear for higher power.

- Using 4P instead of 2P may reduce the cost of the main power supply by another approx 25%.

- More economic analysis should be done.