Analysis of Multiple Classification Attempts concept
802.3at Classification Ad Hoc

Yair Darshan/PowerDsine

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1. Recommendations

Recommended PSE Timing Specifications			
Classification Wave form Section	Minimum [ms]	Maximum [ms]	Notes
1st classification attempt	10	30 (Recommended)	See note 3
1st and 2nd voltage mark rise/fall time, tr+tf.		1.5	Informative only. See note 1
1st and 2nd voltage mark duration	2	4	
2nd classification attempt	10	30	See note 3
Total classification time	**24**	**68**	See note 2

Notes:

1. Tf should not be part of the standard due to the fact that it is determined by Iclass1_min, Cport_max and maximum voltage chance from Vclass_max to Vmark_low.

2. 2nd finger need to end below 10V to allow PD to recognize that two classification attempts were done and any other Vmark phenomena should be ignored.

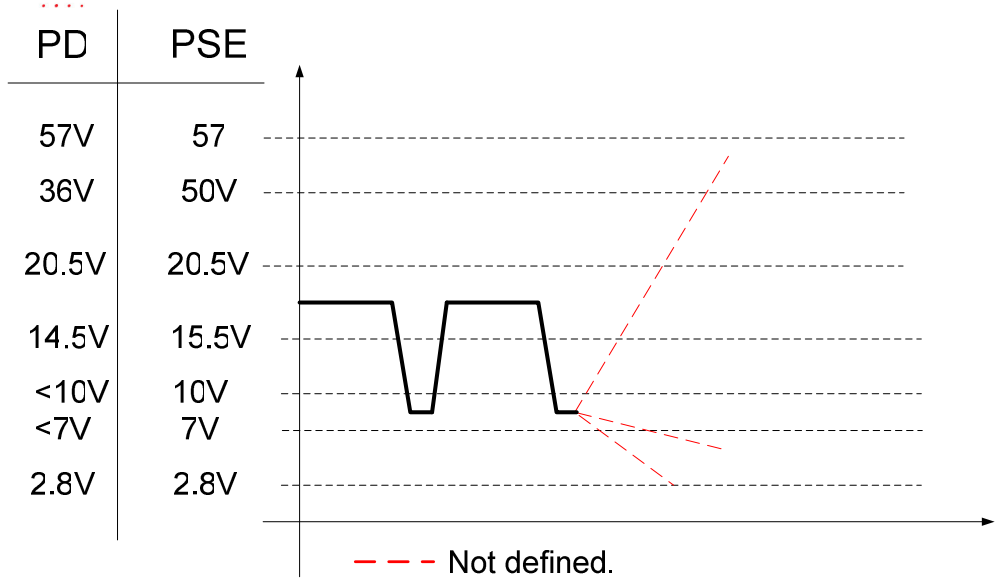
3. 30ms may be reduced to get total classification time of 75ms if 3rd finger is going to be used. We may need to evaluate effects on multi-port system cost related timing Issues which may require us to reduce classification time attempts.

Recommended Voltage and current Specifications				
Classification Wave form Section	PSE		PD	
	Minimum [V]	Maximum [V]	Minimum [V]	Maximum [V]
Classification attempt	15.5	20.5	14.5	20.5
Classification Current	Iclass 1	Iclass 4	Iclass 1	Iclass 4
Mark voltage range	7	10	6.37	10
Mark Voltage transition range	10	15.5	10	14.5
Classification Current prior to transition detection.	NA	NA	Iclass 1	Iclass 4
Classification Current after transition detection.			2mA	Iclass 4
Reset classification circuitry – Lower range	0	2.8	0	2.8
Reset classification circuitry – Upper Range	TBD (50V?)	57	TBD (30?, 36V?)	57

Additional requirements for 802.3at PD:

1. During detection phase, classification circuitry and other circuitry should not consume more than 10uA in addition to Rsig, forming total 25K+/-5%. (Similar to 802.3af)

2. After 1st classification attempt, PD should consume at least Iclass_1 current until PD detects Vmark transition. Resetting from this state will occur on Reset voltage range (low and/or high range)


PD
PSE
57V
57
36V
50V
20.5V
20.5V
14.5V
15.5V
<10V
10V
<7V
7V
2.8V
2.8V
Not defined.

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Classification Table

Based on Clay's presentation from June 28 with additional information added.

It looks like that we can use 2 fingers and may cover future use as well by adding 2 more classes only.

The enhanced granularity will be covered by layer 2.

New Classes	1st attempt	2nd attempt	Code Interpretation	PD[W]	PSE[W]
	0	0	ERROR		
	0	1	ERROR		
	0	2	ERROR		
	0	3	ERROR		
	0	4	ERROR		
	1	0	ERROR		
	1	1	AF PD	3.84	4
1	1	2	AT PD	2	2.02
2	1	3	AT PD	2.84	2.88
3	1	4	AT PD	15.87	17.38
	2	0	ERROR		
4	2	1	AT PD	18.78	20.99
	2	2	AF PD	6.49	7.00
5	2	3	AT PD	21.7	24.77
6	2	4	AT PD	24.62	28.75
	3	0	ERROR		
7	3	1	AT PD	9.72	10.24
8	3	2	AT PD	27.53	32.97
	3	3	AF PD	12.95	15.40
9	3	4	AT PD	30.45	37.47
	4	0	ERROR		
10	4	1	AT PD Future	35	45.23
11	4	2	AT PD Future	40	55.28
12	4	3	AT PD Future	45	68.38
	4	4	AF PD	12.95	15.4

Vpse	50
Rcable	12.5
Ppd_max	30
# of classes for 802.3at PDs Not including 802.3af	6
Linear Power Step	2.92

2. Detailed Analysis

2.1 Concept Principles.

The Multiple Classification Attempts method (MCA) is actually using the 802.3af PSE-PD classification function by repeat it N times in order to extend the available classification codes in order to cover higher power range then 802.af.

The extension of the classification codes is obtained by allowing the PD to change its class every time the PSE requires classification result.

2.2 Design guide lines

2.2.1 PSE: Total classification time: Target = 75ms. (Same as in 802.3af)
PD: 75ms minimum.
Note: .at PSE and PD may use longer time if allowing easier implementation and cost reduction. Additional 30% is tolerable i.e up to ~100ms if necessary.

2.2.2 Classification current level and operating voltage: The same as in 802.3af. (to keep backwards compatibility of 802.3at connected to 802.3af PD and vice versa)

2.2.3 To allow meeting PD Indication objective. (802.3at knows if it is 802.3at PSE or 802.3af) without changing 802.3af/at classification operating voltage regulation requirements. (we can not use voltage changes within the 802.3af classification range as a data to the PD to change its class. Voltage changes might happen due to poor regulation or port to port cross regulation))

2.2.4 Classification current below and above classification voltage range is not defined. It can be zero or any other number.

2.2.5 Class 4 which was reserved for future use, treated by 802.3af PSE as class 0 (15.4W). PD was requested no to use this class. In reality it was used for proprietary implementations. *We need to check if it affects 802.3at available codes.*

2.3. How to meet paragraph 2.2.3 requirements?

PSE has to generate voltage changes which are above or below the 802.3af range in order to uniquely distinct from 802.3af PSE.

If the voltage is higher then 802.3af, it might stay high after PSE tries to reduce it again to 802.3af range due to the fact that 802.3af may use class zero=0 mA so no discharge path is supplied to the PD caps located after the diode bridge.

If voltage is lower then 802.3af classification voltage range and higher then detection voltage range the current is not defined so it can be zero again so PD can not distinguish if it is .at PSE or not.

If voltage is going down to detection range and we mandate .at PD not to use class 0 then we can guarantee a discharge path and a valid voltage change to be used by the PD to change its class.

2.3. Detailed voltage and timing requirements analysis.

2.3.1 System parameters

PSE port capacitance: 0.5uF max.
PD port capacitance: 0.15uF max.
Total system port capacitance during detection and classification: 0.65uF

2.3.2 1st classification attempt:

PD requires stabilizing the current within 5ms. (802.3af requirements)
PSE requires measuring the current not earlier then 10ms.
Hence minimum PSE time for 1st attempt is 10ms.
Max time is X1.

2.3.3 1ST PSE voltage mark

Voltage at the PSE goes down below 10V (max detection voltage level for compliant PD)
In order to allow low cost implementations that is not requiring high voltage accuracy measurement e.g **30%** total accuracy. Hence PSE voltage between 7V min to 10V max.

The PD voltage at the RJ45:
Taking in account cable voltage loss and diode bridge drop:
Iclass_4_max*Rcable_max=51mA*12.5Ω= 0.6375
The minimum voltage at the PD will be: 7V-0.6375V=**6.37V**

The Voltage across the PD chip:
6.37V -2*Vd(0 deg C)=4.37V.

PD chip vendors need to verify if it is practical operating voltage range.

2.3.4 What will be the fall time?

Case 1:

We mandate that during classification voltage range Iclass_min=Iclass1_min i.e. 802.3at can not use class 0.
Bellow 15.5V we have to assume that only Rsig is connected to for 802.3af PDs.
In this case it doesn't matter once Vport is again in classification region.

For 802.3at PD:

Cport=0.65uF max.
Iclass min=Iclass 1 min=9mA.
Rsig_max=25K*1.05=26.25K
Hence tf is the sum of tf1+tf2.
tf=tf1+tf2=Cportx(20.5-15.5)/Iclass_min+ R*C*LN(5/15.5)=0.36ms+188.5ms >>75ms ==> not a valid solution.

Case 2:

We need to mandate that until PD detects the transition to Vmark, it consumes Iclass_1 to Iclass 4.
Once transition is detected current can go down to 2mA.

Transition detection range is 10V to 15.5V.
Example: If PD detects transition to Vmark at 11.1V then from 15.5V to 11.1V the PD current will be any number between Iclass1 to Iclass 4.
Below 11.1V the current may go down to 2mA.

It requires additional hardware at the PD which will disconnect the classification circuitry from Rsig circuitry to avoid loading of Rsig during detection phase.
Once detection phase is over, and Vclass is first delivered by the PSE, the PD detects this scenario and allows the required discharge current as explained above.

Hence Tf may be reduced to: Tf=0.65uFx(20.5V-10V)/9mA =0.76ms max.

At this point we ensure that if PSE is reducing the port voltage to a value Vmark_low <10V, it is guaranteed by compliant 802.3at PD to discharge the port to allow transition detection.

Detection of the transition by the PD is used as a trigger to change the PD class to the next class code.

In order to ensure robust operation, the PSE has to guarantee a minimum time in which the port is at Vmark_low level. What is the recommended time duration, Tmark?
It is best that Tmark should be >3xtf to allow a mix of edge and level triggering for flexible and noise free operating of the PD circuitry.

If we OK with Tmark_min=3xtf_max and Tmark_max=6*tf_max
Then:
Tmark_min=2.3ms, Tmark_max=4.5ms.
2ms min to 4ms max is OK too.

2.4 Classification Table: TBD

2.4.1 Principles of classification table

a) supporting 2W power level at the PD
b) to add additional class between class 2 and class 3.
c) Limit number of classes over 2P to 10 classes including 802.3af classes
d) Allow extension for more classes for future use to cover higher power then TBD and less then 50W over 2P.
e) Ensure interoperability of 802.3af/at PSEs and PDs
- codes 0,0..0 ; 1,1..1; 2,2..2; 3,3..3; 4,4..4; will be red as 802.3af PD
- Class 0 can not be used by 802.3at PD due to the fact that it can be zero current and will not discharge the port voltage to the Vmark range in order to indicate 802.3at PD that we are connected to 802.3at PSE.

2.4.2 PSE Class=PD Class+Cable loss

$$\frac{Vpse - Vpd}{Rcable} = \frac{Ppd}{Vpd}$$

$$Vpd = 0.5 \cdot Vpse + 0.5 \cdot \sqrt{Vpse^2 - 4 \cdot Rcable \cdot Ppd}$$

$$Iport = Ppd / Vpd$$

$$Ploss = Iport^2 \cdot Rcable$$

$$PSE\_class = PD\_class + Ploss$$

PSE class levels in 802.3af PDs will not be changed to keep interoperability.
(They were calculated with 20 ohm Rcable and Vpse=44V)

2.5 False Classification Mark voltage due to PD isolation switch time delay

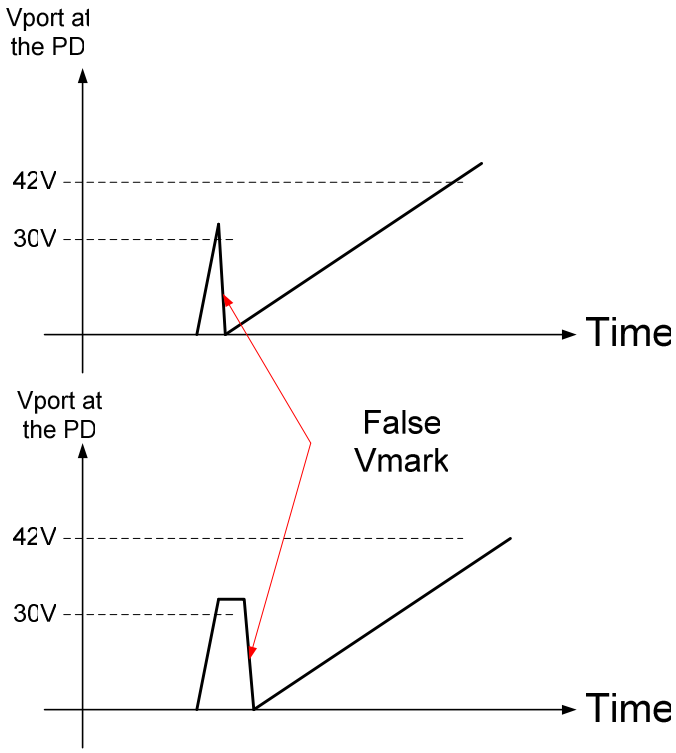
2.5.1 Background

The PD is equipped with a switch that isolates the signature resistor and the classification circuits from the DC/DC converter input impedance.

During startup phase, when Vport at the PD is lower then 30V the DC/DC input capacitor is discharged.

Once the isolating switch is on, a voltage is applied to the PD DC/DC input capacitor which present a short circuit causing the Port voltage to reach zero and then ramping up again.

This behavior is permitted by the standard however may cause to false mark voltage when PSE is transiting from classification voltage to power ON state.



2.5.2 Possible solution

1. To create special voltage signature that will differentiate between Initiated Vmark and port voltage drop due to time limited short circuit or low impedance condition.

   Example 1: PD is counting the number of Vmark transitions. If N>2 for 802.3at then ignore other events while Vport is below 30V.