# Vport ad hoc dynamic discussion July 2006


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# Agenda

- **Solutions facilitated by providing a dynamic port voltage specification.**
- **Existing constraints review.**
- **Simplified view of the PD.**
- **Review of questions.**
- **Next step.**

# Existing Concerns

- **The IEEE specifies a single PSE to PD connection.**
  - **Real systems have multiple ports.**
- **PoE is pervasive and requires fault tolerant mechanisms.**
  - **Power supplies have one of the lowest MTBF of a system.**
  - **Several mechanisms exist to backup a supply.**
- **Additional IEEE specification constraints may be required in order to facilitate solutions.**

# Existing Constraints: Port Power

- **Average power over 1 second.**

  **PSE Table 33-5, item 14, Continuous Output Power**

  **PD 33.3.5.2, Input average power**

- **Other times power is over ~50 ms.**

  **Ex/ $P_{port\_max}/V_{port}$**

  **PSE 33.2.8.6 (Tovld = 50 to 75 ms)**

  **PD 33.3.5.4 (50 ms, 5% duty,RMS)**

- **Concern**

  **The ad hoc will need to come up with a definition for power.**

# Existing Constraints: Current Demand

- **PSE 33.2.8.2 Load Regulation**

  **dv/dt <= 3.5 V/us @ di/dt <= 35 mA/us**

- **History:**

  **Common mode voltage noise of 795 mV @ 7 MHz affects 100BASE-T Ethernet at 145 m cable lengths.**

  **An additional 20 dB margin results in a common mode constraint of dv/dt of 3.5V/uS.**

  **This constraint was imposed when common mode current is 35mA/uS because the pair cable impedance is 100 ohms.**

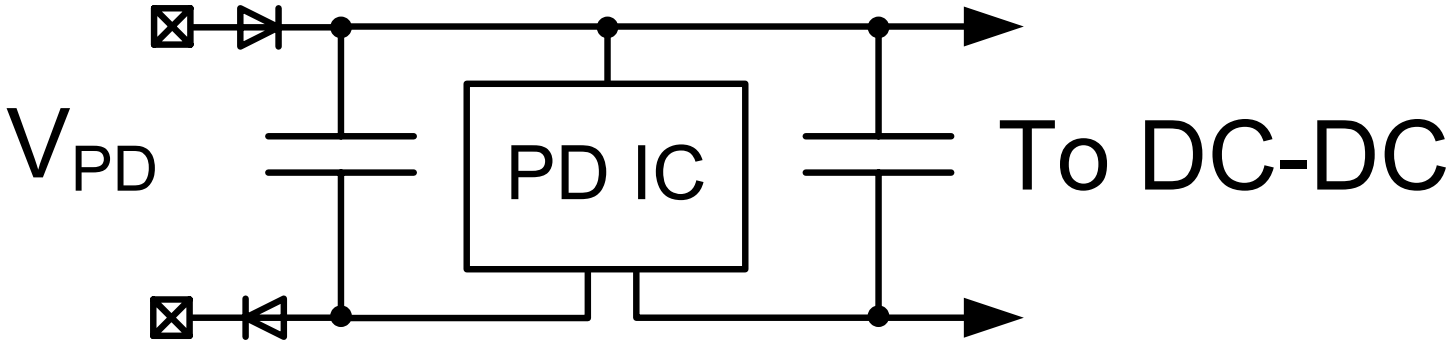
- **Concern:**

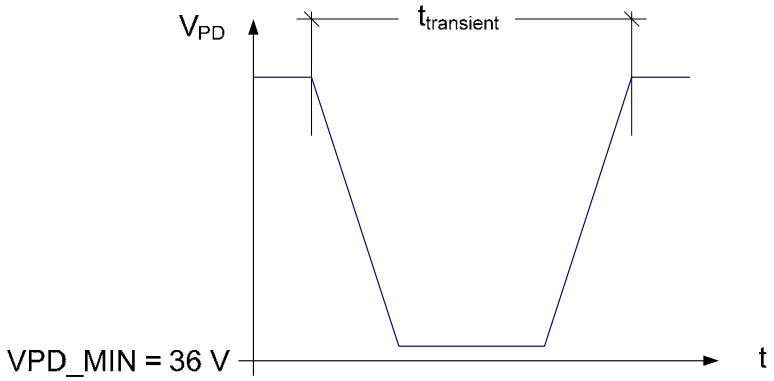
  **A differential mode impedance does not correctly translate a common mode voltage to a common mode current.**

  **The PD constrains will determine the di/dt seen.**

  **This dv/dt may cause existing PDs to shut down.**

# dv/dt may cause existing PDs to shut down



# Existing Constraints: Current Demand

- **PSE current limits**

  **33.2.8.6 Overload detection range, $I_{CUT}$ = 15400/Vport, $T_{ovld}$**

  **33.2.8.8 Output current—at short circuit condition. $I_{LIM}$ for $T_{LIM}$**

- **Concerns**

  **This requirement is for any valid DC input. What minimum voltage is valid? The 30 V limit is in an amendment which is not part of the specification.**

  **Measurement to be taken after 1 ms. What about a transient and dead shorts?**

# Existing Constraints: Current Demand

- **PD 33.3.5.4 Peak Operating Current**

  **$P_{port\_max}/V_{port}$, 50 ms and 5% duty cycle, R.M.S calculation**

  **and Table 33-12 item 4, $I_{port}$ max. (larger than I = P/V estimate)**

- **Concerns**

  **What constraints exist on di/dt?**

# Existing Constraints: PD Capacitance

- **PD 33.3.5.5 PI Capacitance during normal powering mode**

  **When $C_{in}$ > 180uF, a voltage change of 44 to 57 V with a 20 ohm series resistance $I_{port}$ is limited by Table 33-12 item 4.**

  **When $C_{in}$ <= 180 uF, no limitations.**

- **Concerns**

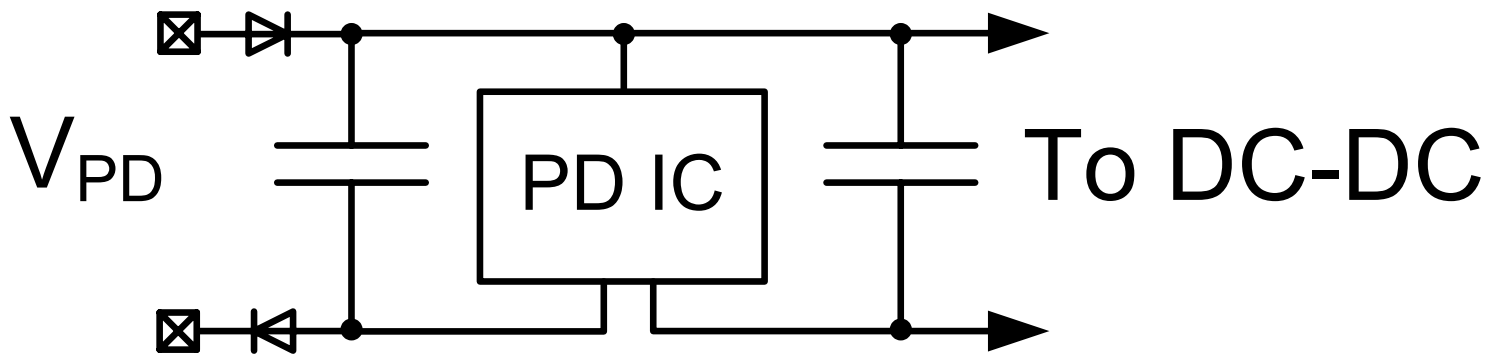
  **What is the di/dt for these?**

  **Ex/ 13 V change, Ipeak = 13V/20ohm = 650 mA, tau = 3.6 ms**

  **650 mA/(13 V/3.5 V/us) = 175 mA/uS**

  **di/dt will be worse with a lower cable resistance.**

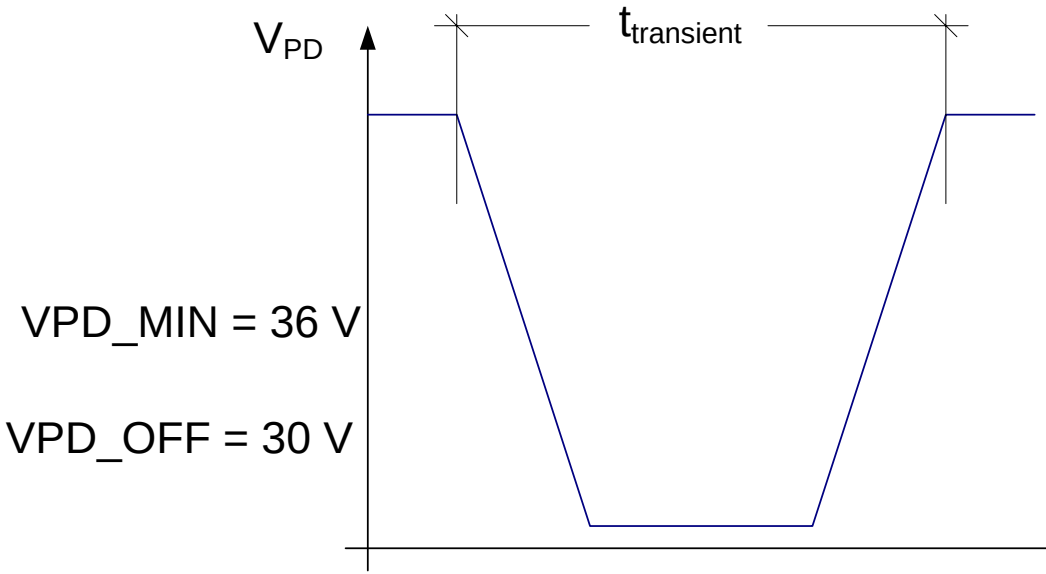
# PD View of Supply transient




**$V_{PD}$ > 2 $V_D$ + $V_{cap}$ then DC-DC draws current from $V_{PD}$.**

**$V_{PD}$ < 2 VD + $V_{cap}$ then DC-DC must operate at $V_{cap}$.**

# VPD < 2 $V_D$ + $V_{cap}$, diodes reverse biased




**Energy = ½ C $V^2$**

**(Power x time) = Energy**

**P < E/t**

**P < 1/2$CV^2$/t**

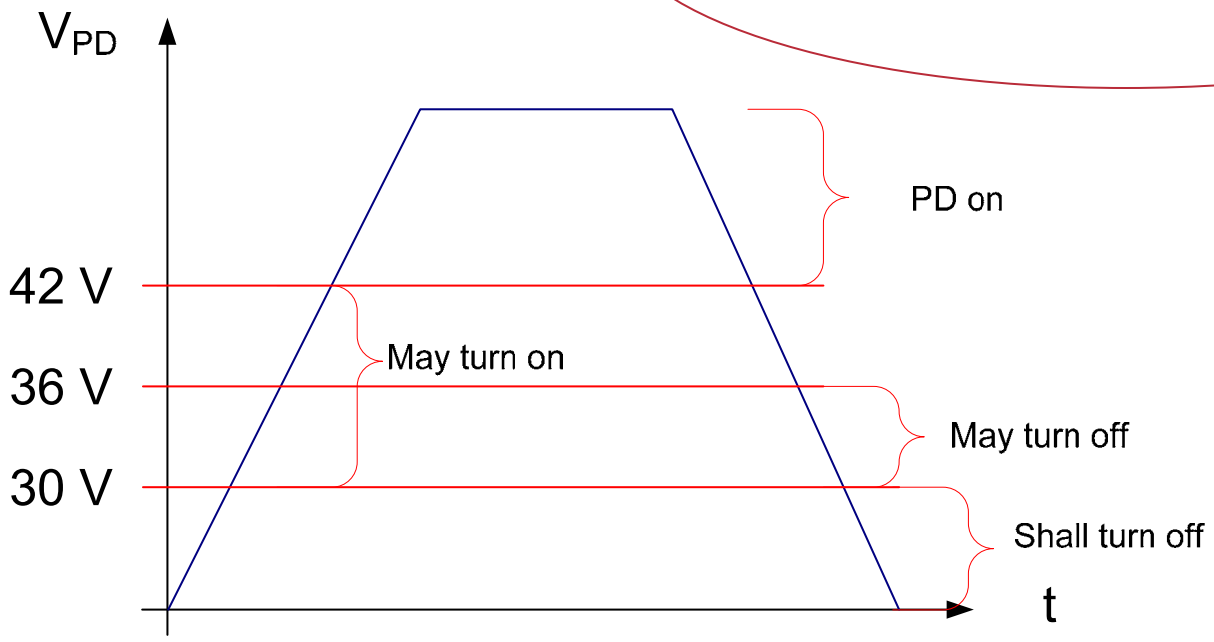
# PD demands during a transient

- **PSE 44 V, PD 30 W**

  **$I_{port}$ = 1.0 A**

  **$V_{pd}$ = 29.8 V**

**Encourage use of Vport Spreadsheet see May Interim**



# Review of questions

- **Power definition.**
- **dv/dt**

  **@ di/dt**

  **Shut down of PD at existing levels.**

  **di/dt PD limit due to bulk capacitance.**
- **PSE current limits**

  **Short timing and Vmin**

  **Bandwidth**

  **di/dt**

# Next Step

- **Help answer questions.**
- **Collect PD and PSE system input.**
- **Define PSE, PD and dynamic Vport, needs.**