IEEE P802.3at

Editor Report

Status

- D0.1 released
  - 2 whole days for review before meeting commenced
- Maintenance items not highlighted
  - These are approved changes to 802.3-2005: NOT SUBJECT TO CHANGE
  - Will mark them differently in D0.2 for convenience
- Mistakes on timing specs for Type 2 hardware classification
- Proposed to polish PSE text before tackling PD
  - Comments? Objections?

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Open Questions

- Now that midspans can officially operate over 1000BASE-T, should they have an Alternative A implementation?
- Do we have an official I_{Port_max}?
- How will we handle cable references and derating?
- Type 2 Classification Details
  - Should Clay's figure go in an informative Annex?
  - Should mark event current limit be more in the 2-5 mA range?
    - I just made up the 5-10 mA as a place holder
  - Include a PSE state diagram?
    - Current diagram does not necessarily handle fault conditions or Type 2 PSEs that want to look like Type 1
- Layer 2 Classification Details
  - ?
- Vport Ad Hoc Details
  - Need to flesh out I_{LIM}, I_{CUT}, &c.

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Closed Questions

- None at this time

Next Steps

- Comment resolution process?
- Agree on Hardware Classification text (33.2.7)
  - Informative Annex for diagrams
  - PSE state machine
  - Fix timing specs
- Close on I_{LIM}, I_{CUT}, energy-based limits
- Short circuit maintenance
- Maybe some L2 inclusions