

Vport ad hoc PD di/dt and PSE voltage transient limits proposal

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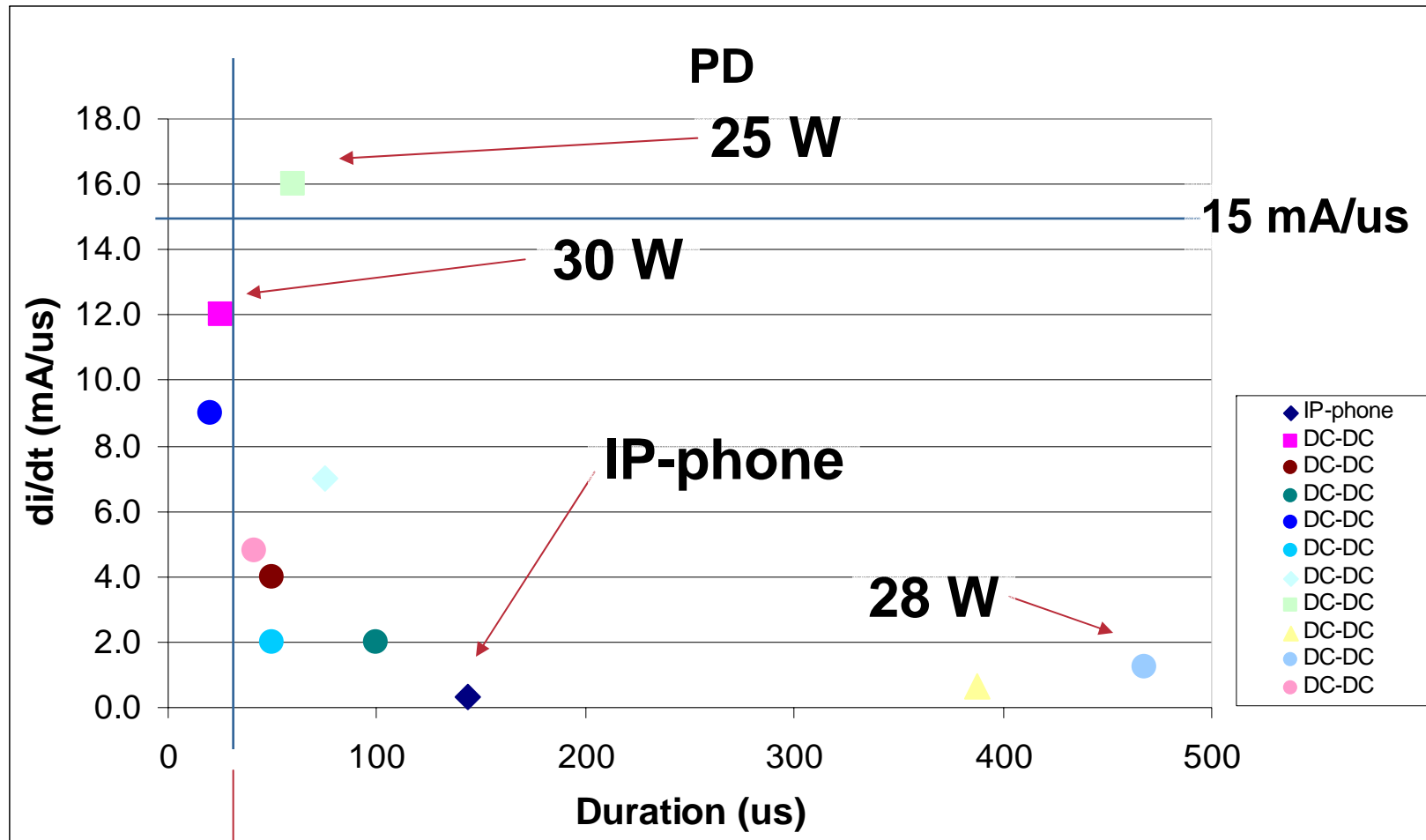
Texas Instruments
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Four ad hocs with an average attendance of 12 people since the last IEEE meeting. People that attended since the last IEEE meeting are shown in **bold**.

Agenda

- **PD data collected**
- **PD di/dt limit**
- **PSE data collected**
- **PSE current limits**
- **PSE voltage transient limits**
- **Motion**
- **Supplemental materials**

Sample PD di/dt values



A 5 μ F PD capacitor supports transients of less than 30 μ s.

All but the IP-phone are PD DC-DC measurements.

The PD di/dt limit

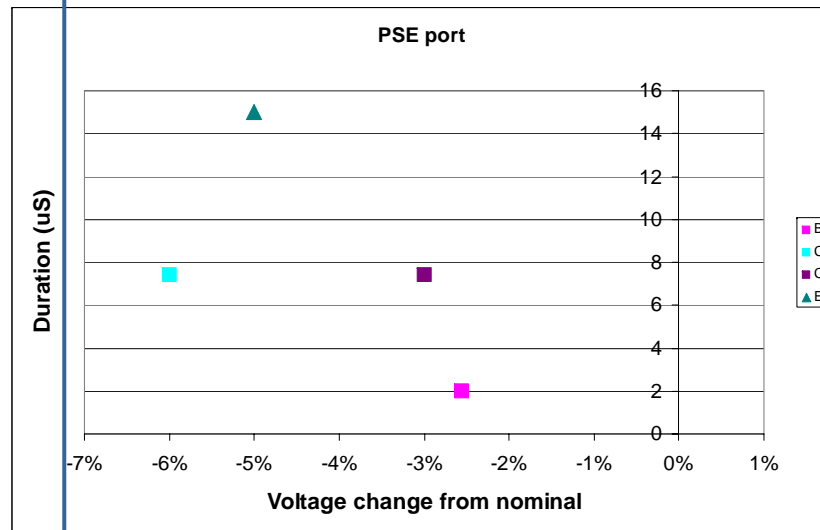
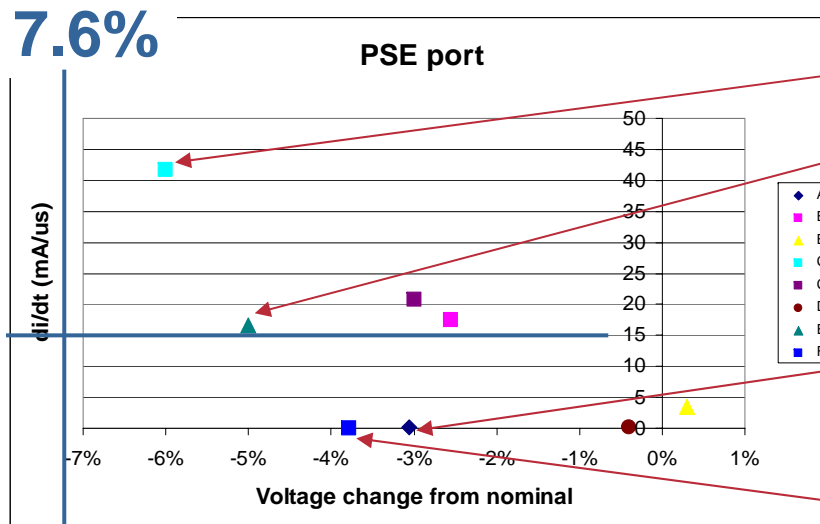
- **Ensures interoperability.**
- **Ensures reasonable system cost.**
- **< 35 mA/μs ensures Ethernet data integrity.**
- **Ad hoc straw polls**
 - 15 mA/μs, unanimous ok 12/12**
 - 10 mA/μs, 11/12 ok**
 - 5 mA/μs, most prefer higher**

Proposed PD di/dt limit

Proposed an absolute PD limit of 15 mA/ μ s after inrush and the static PD MDI voltage exceeds $V_{\text{port_min}}$. This does not include disconnect.

Sample PSE load change effects

15 mA/ μ s



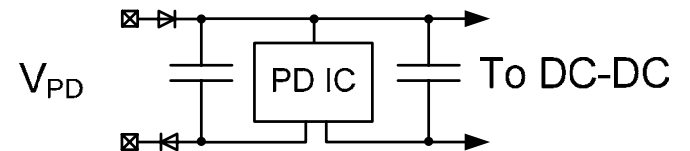
No load to 400W.

Switch from AC to DC, 500W.

Slow 0 to 100% load change.
~160 μ s transient.

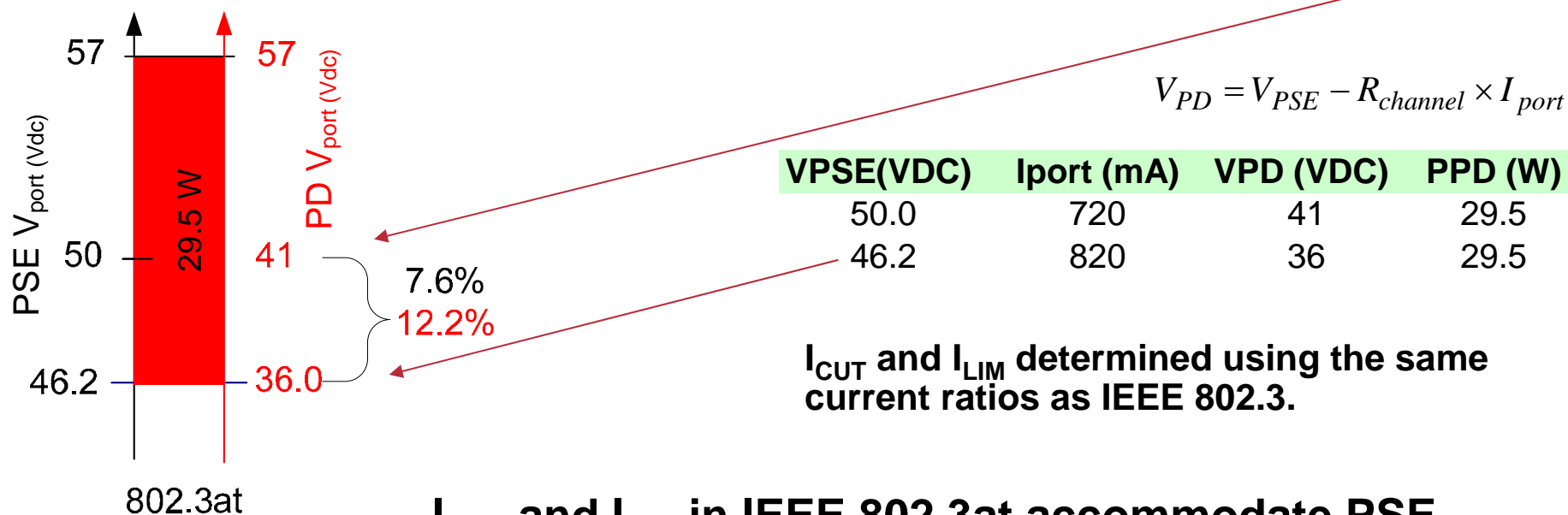
900 W load change.
This is a change in static port voltage.

Durations < 30 μ s do not affect the PD.



29.5 W PD

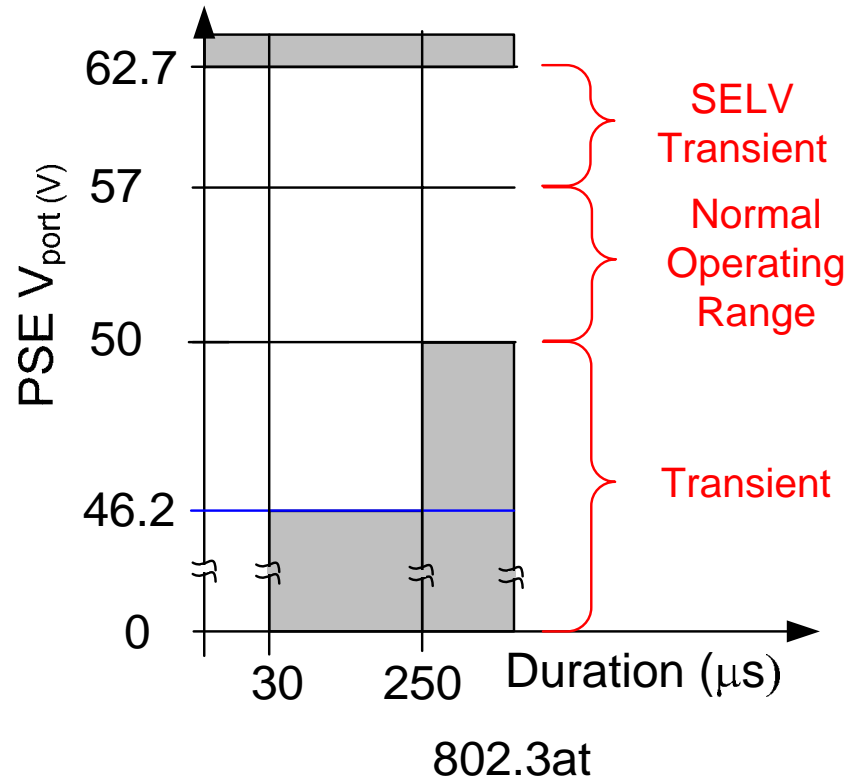
Ratio	Parameter	PD Vport (V)			
		802.3	AT	802.3	AT
1.29	I_{LIM_MAX} (mA)	450	920	35	38.5
1.14	I_{LIM_MIN} (mA)	400	820	36	39.8
1.00	I_{CUT_MIN} (mA)	350	720	37	41.0



I_{CUT} and I_{LIM} in IEEE 802.3at accommodate PSE voltage transients and PD current transients.

The largest droop for the sample PSEs is 6%.

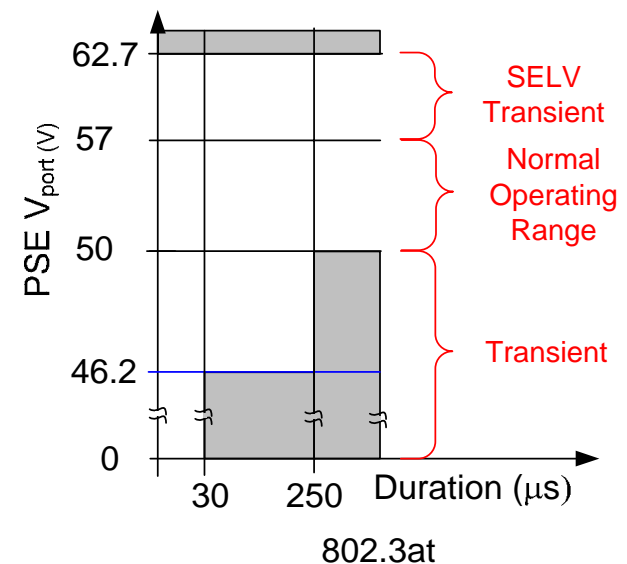
PSE-on V_{port}



Grey regions are prohibited when the PSE is on.

Proposed Voltage Transient Specification

- Propose a PSE PI voltage limit, for transients present more than $30\ \mu\text{s}$, of 7.6% below the PSE $V_{\text{port_min}}$ level for less than a period of $250\ \mu\text{s}$ and 10% above the $V_{\text{port_max}}$ level.



Motion

Move that:

**The IEEE 802.3at Task Force adopt presentation
schindler_1_03_07.pdf slides 5 and 9 to be incorporated in
P802.3at draft D0.2.**

M: Fred Schindler

S: Thong Huynh

All Present

For: 36

Against: 0

Abstain: 5

802.3 Voters

For: 25

Against: 0

Abstain: 4

Existing Constraints: Current Demand

- **PSE 33.2.8.2 Load Regulation**

$$dv/dt \leq 3.5 \text{ V/us} @ di/dt \leq 35 \text{ mA/us}$$

- **History:**

45%
Margin

Common mode voltage noise of 795 mV @ 7 MHz affects 100BASE-T Ethernet at 145 m cable lengths.

900%
Margin

An additional 20 dB margin results in a common mode constraint of dv/dt of 3.5V/uS.

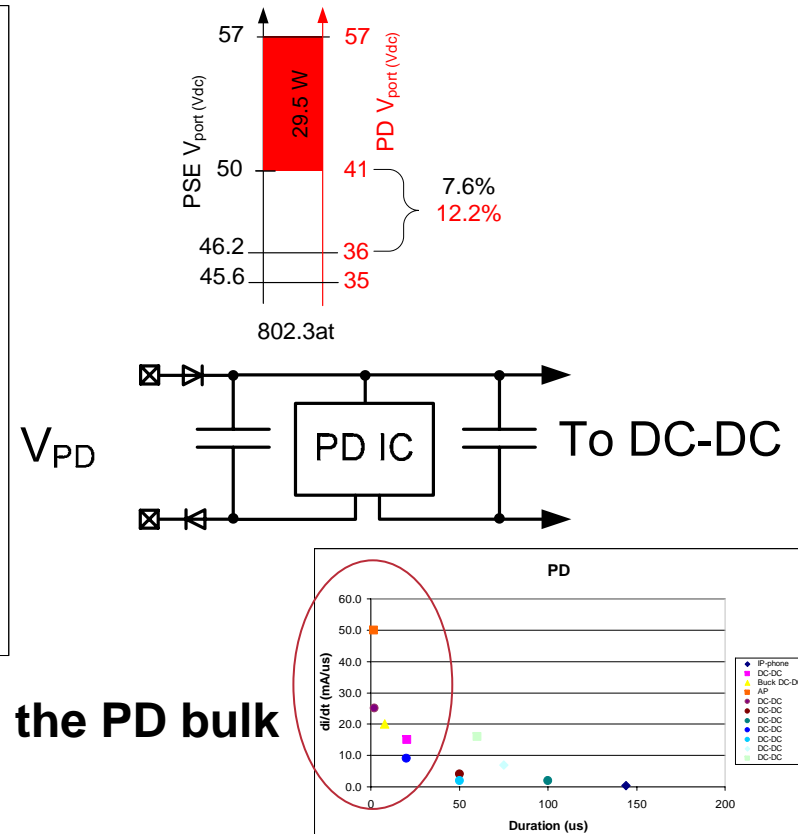
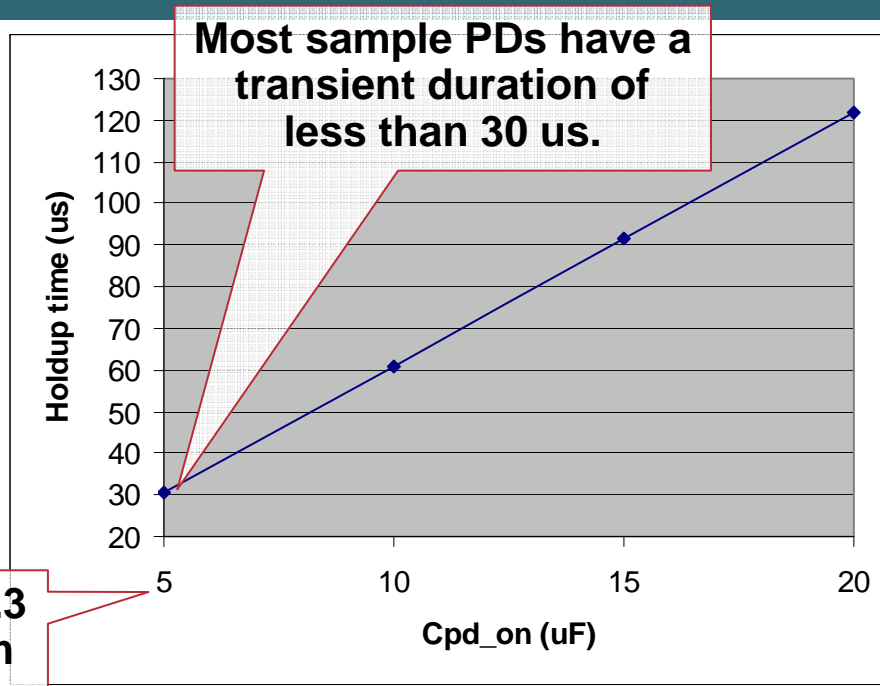
This constraint was imposed when common mode current rate is 35mA/uS for a resistive (100 ohms) PD drawing 12.95W that is subject to a 3.5V/us slew rate.

Indirect PD di/dt limits

- **Table 33-5, item 3 and table 33-12 item 7.**
< 1 MHz, $V_{pp} < 0.1 V_{pp}$
 $dv/dt \text{ (max)} = V_p 2\pi f = 0.3 \text{ V}/\mu\text{s}$
- **PD di/dt limit. $di/dt = dv/dt/R$**
 $di/dt = 0.3/(Z_{PSE} + 12.5)$
- **$di/dt = 0.3/(0.9 + 12.5) = 22 \text{ mA}/\mu\text{s}$**

Table 33-5, item 3 references section 33.2.8.3. **33.2.8.3 ...** The limits are meant to ensure data integrity. ...

Fast transients



$dt = CdV/I$, $I = I_{LIM_MIN} = 820$ mA, at this current a 29.5 W, PD has at least 36 V at its input.