Vport ad hoc update part 2
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Fred Schindler

Cisco Systems

Andrew Smith	**Power Integration**
Anoop Vetteth	**Cisco Systems**
Bill Delveaux	Cisco Systems
Brian Buckmeir	Bel
Chad Jones	Cisco Systems
Christen Beia	ST Microelectronics
Clay Stanford	**Linear Technology**
Dan Dove	**HP Procurve Networking**
Daniel Feldman	**Microsemi**
David Law	3COM
David Lucia	**SIFOS**
Derick Koonce	Independent
Ferdinando Lari	**ST Microelectronics**
Frank Yung	SystemX
Fred Schindler	**Cisco Systems**
Geoff Thompson	**Nortel Networks**
Helen Kastner	Cisco Systems
Hugh Barrass	Cisco Systems
Jean Picard	Texas Instruments
John Jetzt	Avaya
Keith Hopwood	Phihong
Ken Bennett	**SIFOS**
Martin Patoka	**Texas Instruments**
Matthew Landry	**Silicon Labs**
Michael Altmann	**Akros Silicon**
Pavlick Rimboim	Microsemi
Ramesh Sastry	Cisco Systems
Raul Lozano	Pulse
Riccardo Russo	**ST Microelectronics**
Sajol Ghoshal	Akros Silicon
Taufique Ahmed	**Akros Silicon**
Thong Nguyen	**Maxim**
Thuyen Dinh	Pulse
Tim Parker	**Nortel Networks**
Wael Diab	**Broadcom**
Yair Darshan	**Microsemi**
Youhoa Xi	**National Semiconductor**

Four ad hocs with an average attendance of 12 people since the last IEEE meeting.
People that attended since the last IEEE meeting are shown in **bold.**

System Considerations

- **IEEE parameters are valid only at the points where they are tested for compliance.**

  A PSE dv/dt rate of 3.5V/μs is valid when test at a load rate of 35 mA/μs.

- **Philosophy: move the solution burden to the source of the problem.**

System Concerns being addressed by I_{LIM}

- **Situations that lead to a PSE dv/dt rate that causes excess PD current demand.**

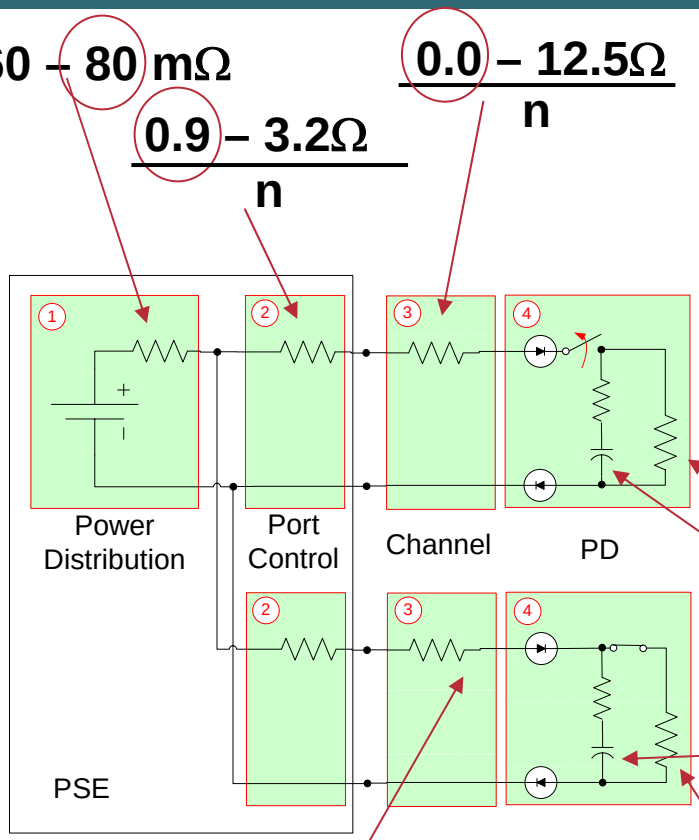
  Multiple PDs reducing their load.

  A PSE switching in a new power supply to deal with a power supply failure.

  Assuming a PSE transitions from the minimum supply voltage to the maximum supply voltage at the dv/dt test point of 3.5V/μs.

Philosophy: move the solution burden to the source of the problem.

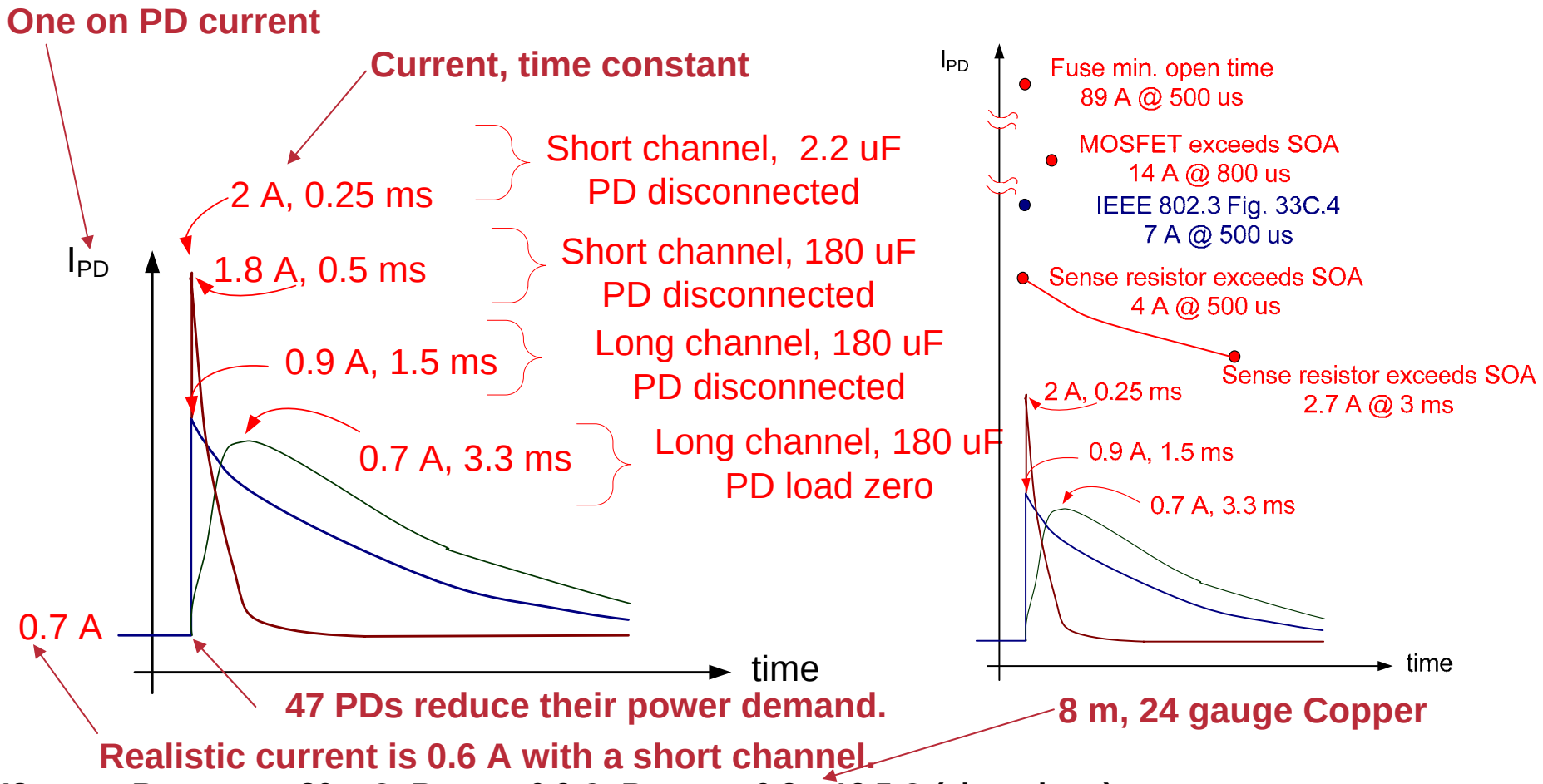
Use Case: PSE load reduction



1. All PDs draw maximum power.
2. All but one PD reduces power demand to zero.
3. The PSE distribution voltage ramps up.
4. The remain on PD has current injected into it.

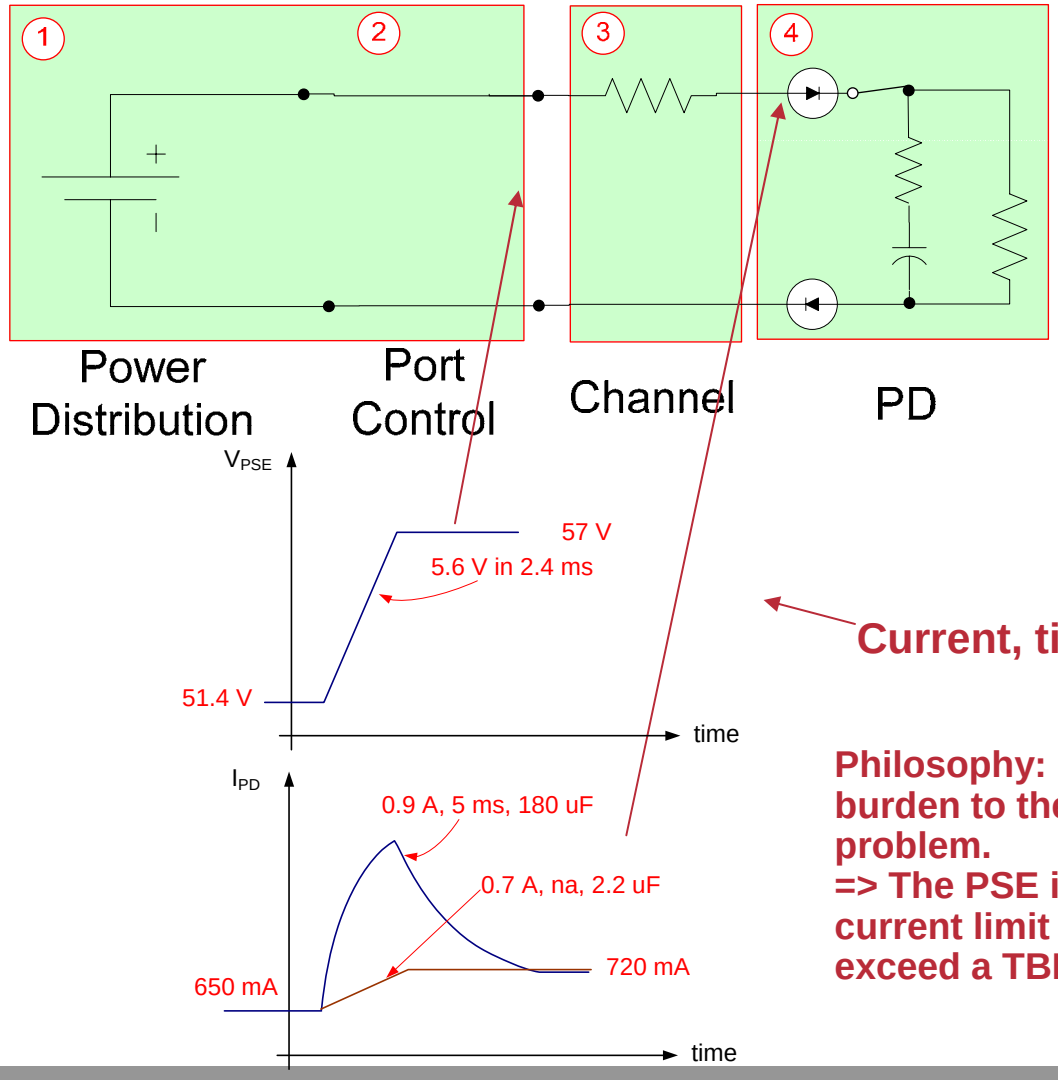
A PSE providing 50 V at 720 mA results in a PD voltage of 41 V (29.5 W).

Use Case: PSE load reduction



48 ports, $R_{distribution}$ = 80 mΩ, Rport = 0.9 Ω, $R_{channel}$ = 0.8 – 12.5 Ω (short, long),
C_{PD_OFF} = 180 μF, C_{PD_ON} = 180 μF, tan δ = 0.07, or C_{PD_ON} = 2.2 uF, tan δ = 0.0 (no ESR)
1 A fuse (1.98 A^2s), Generic NCH MOSFET, V_{DS} = 10 V @ I_D = 14 A

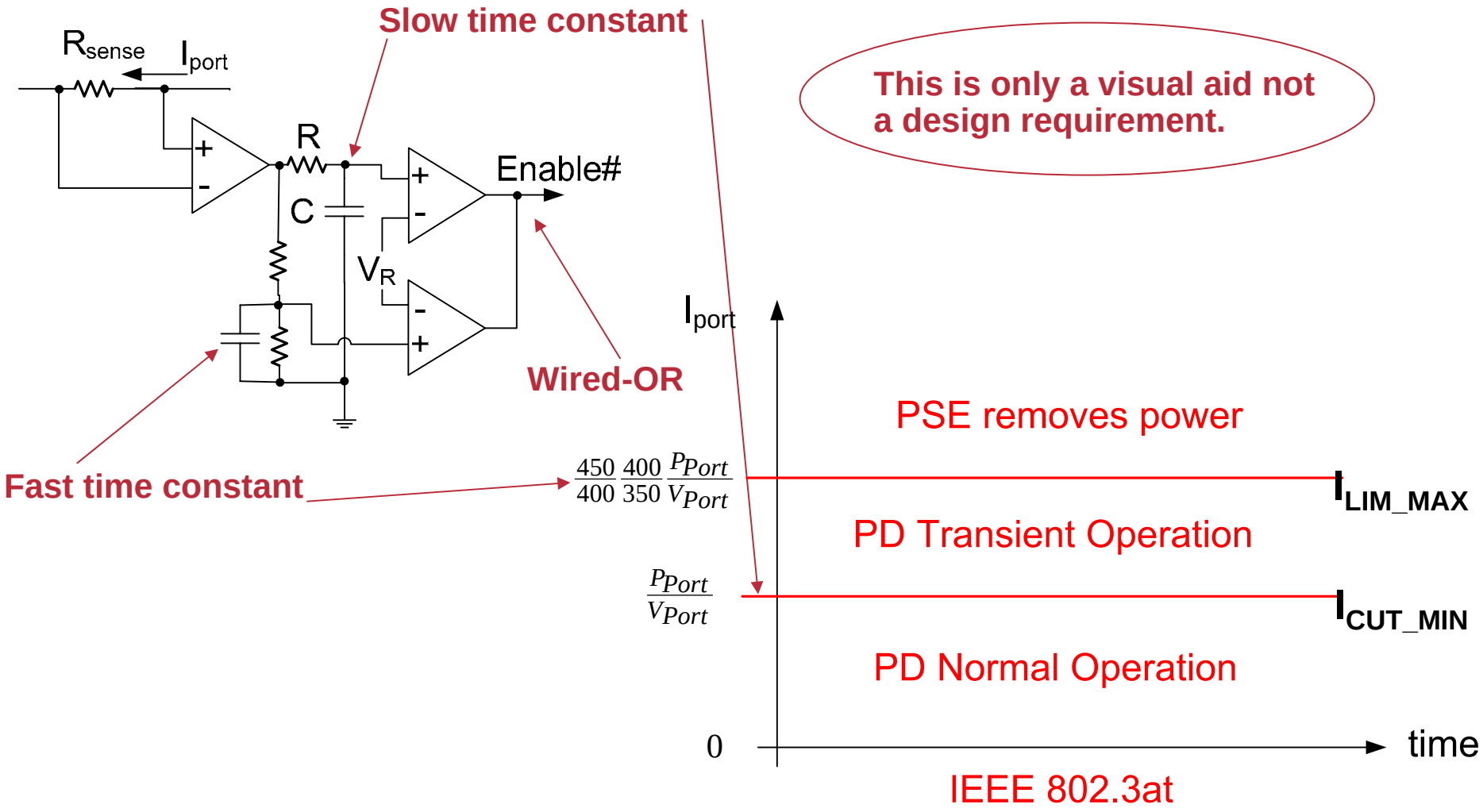
Use Case: PSE power supply backup



Current, time constant

Philosophy: move the solution burden to the source of the problem.
=> The PSE is required to use current limit if the PSE could exceed a TBD energy limit.

Proposed PSE current monitor



How to specify?

- **Goal: Create a energy transfer compliance test that ensures system interoperability and permits a current limit design or an energy based design.**
- **Current limiting designs require more time to charge PDs than energy limited designs.**
- **Energy limit designs allow higher current for a shorter period of time than current limiting designs.**
- **Both transfer the same amount of energy to the PD capacitor but have different channel losses.**

PSE Limiting the Current

Due to PSE supply change

$$Max\_Energy = \frac{1}{2} C_{PD} (V_f^2 - V_i^2)$$

$$= V_{PSE\_MIN} \times (I_{LIM\_MIN} - I_{CUT\_MIN}) \times T_{LIM\_MIN}$$

Current available for charging the PD capacitor.

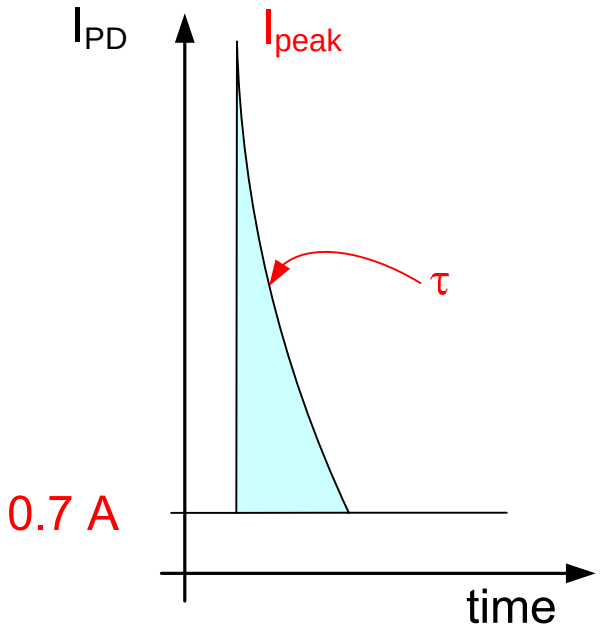
$$\frac{1}{2} 180\mu (57^2 - 50^2)$$

$$= 50 \times (0.820 - 0.720) \times T_{LIM\_MIN}$$

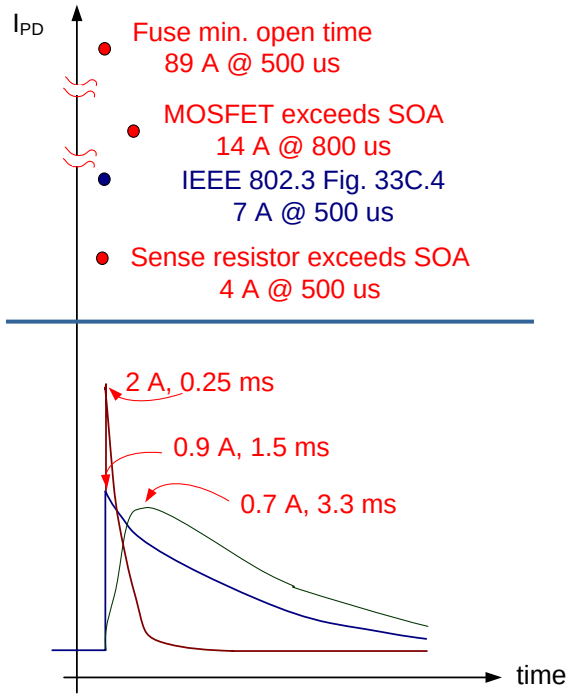
These two parameters are under the control of the PSE.

T_{LIM_MIN} = 13.5 ms

PSE Energy Limit



$$i(t) = I_{CUT\_MIN} - (I_{CUT\_MIN} - I_{peak})e^{-t/\tau}$$



Power = V_{PSE} x I_{port}
Energy = Power x time

$$AREA = \int_0^{4\tau} i(t)dt = I_{peak}\tau e^{-t/\tau}\Big|_0^{4\tau}$$

Next Step

- **Review and expand details on the proposed energy based limit.**
- **Create a simple method to test for compliance.**
- **Update the task force on progress made.**

Based on V13 Spreadsheet.