IEEE802.3at Task Force

Vport ad hoc

Derivation of minimum TLIM for IEEE802.3af/at

Revision 002

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Objectives

- To analytically determine worst case Minimum T_{LIM}.
- Derive Spice Model and simulation results to confirm the analytical calculations.
- Setting Minimum T_{LIM} requirements.

Analytical Derivation of TLIM , Icut max and not Icut min

Equation derivation is based on solving differential equation in the current domain and not energy equation as suggested in ref 1.

The energy equation used in last ad-hoc reports is not correctly describing the physical energy transfer from the PSE to PD.

reasons:

1. The left side of the equation is change of energy transfer. The 2nd part contains constant voltage hence they cant be equal.
2. The left side of the equation refer to the PD side and the right side refering to to the PSE. Losses is a mjor factor in setting TLIM minimum.
3. The term (ILIM_MIN – ICUT_MIN) is not constant which adds more error by increasing the TLIM_MIN value.

   The dynamics of the system is differential in two domains: In time and in negative resistance closed loop behavior. The energy equation doesn't address these two domains and creates errors.

4. The above were confirmed by simulations presented in this document.

News from 802.3af..

- **33.2.8.4:**

"For VPort > 44 V, the minimum value for IPort_max in Table 33–5 **shall** be **15.4 W/VPort**."

- **33.2.8.4:**

"The PSE **shall** support the following **AC current waveform** parameters:

a) **Ipeak = 0.4A** minimum for 50ms minimum and 5% duty cycle minimum.

b) **For VPort > 44V, Ipeak = 17.6 W/VPort.**"

- **33.3.4**

"The PD is classified based on power."

- **33.3.5.4** Peak operating current

At any operating condition the peak current **shall** not exceed **PPort max/VPort** for more than 50ms max and 5% duty cycle max. **Peak current shall not exceed IPort max.**

The maximum **IPort_dc** and **IPort_rms** values for all operating **VPort** range **shall** be defined by the following equation: **IPort_max [mA] =12950/VPort.**

- **33.3.5.9 PD stability**
- **CAUTION**—When connected together as a system, the PSE and PD ….due to the presence of **negative impedance** at the PD input. See Annex 33D for PD design guidelines to ensure stable operation.

PD models summary

- Constant current model

$$TLIM = \frac{Cpd \cdot dv}{di} = \frac{Cpd \cdot dv}{(I_{LIM\_MIN} - Ipd)} = \frac{Cpd \cdot dv}{(0.4A - 0.35A)}$$

- Icharge=50mA constant. Not addressing the case of 0.4A overload at PD!
- At PD overload of 14.4W (0.4A) , Icharge=0. TLIM=Infinite.

- Constant power model

$$TLIM = \frac{Cpd \cdot dv}{di} = \frac{Cpd \cdot dv}{(I_{LIM\_MIN} - \frac{Ppd}{Vpd})} = \frac{Cpd \cdot dv}{(0.4A - \frac{12.95}{Vpd})}$$

- Icharge starts at 50mA and increases over time due to Cpd ramping voltage! Hence charging current is increased over time.
- If Ppd is going from 12.95W (0.35A) to 14.4W (0.4A) then:

  Charging current is zero at t=0 but Icharge>0 AT t>0 which address partially the case of 14.4W (0.4A) over load at the PD.

TLIM_MIN in constant current at PSE
Constant current Model at PD

$$TLIM = \frac{Cpd \cdot dv}{di} = \frac{Cpd \cdot dv}{(I_{LIM\_MIN} - Ipd)} = \frac{Cpd \cdot dv}{(0.4A - 0.35A)}$$

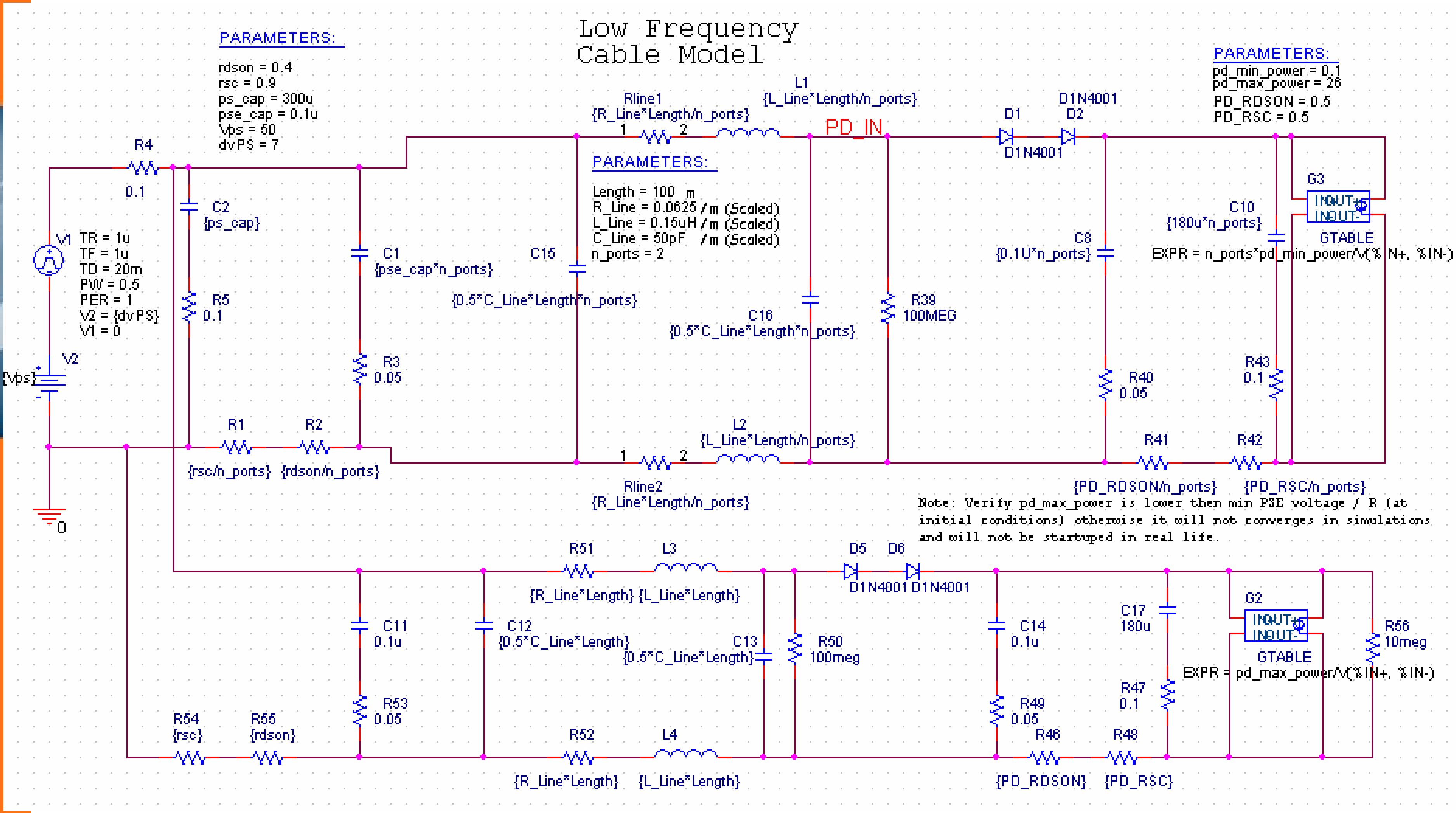
		TLIM[ms]	
Channel	Model	AF	AT
Short	C. Current	40.26	9.7
Long	C. Current	38.36	7.27

Choosing the PD model

- PD model: Constant Power
- Used in 802.3af for **average** and **peak** current!
- What ever TLIM value is, we can later add margin to cover corner cases.

The important issue is to use the same physically correct model for all questions in the specification and deal with corner cases separately.

General Model



Simplifying the model

Parameter	Affect on		Notes
	Ipeak	TLIM	
Cable Inductance	NO	NO	L/R<<R*C
Cable Capacitance	NO	NO	C_cable<<Cpd
Cps	YES	NO	$0.08\Omega \cdot Cps << Cpd \cdot \sum R$
Cpd	~YES	YES	
T_{LIM} crossing point	NO	YES	Tcut (50ms) >> T_{LIM_MIN} For Iport <= ICUT_MAX port is ON, Port voltage is within operating range, no excess heat as potentially in I_{LIM} range.
PD model type	NO	YES	Constant power load (as used by IEEE802.3af all over the spec.) Other model types (R or constant current) differs only in TLIM.

Who Affects T_{LIM_MIN}

- Case 1: Cross Regulation Effects [1,2]
  - N-1 ports are changing load from Full Load to No load.
  - 1 Port is consuming Full load. As a results PSE port voltage rapidly increased causing positive current transient at the PDs.
  - The positive current transient crosses ILIM region.
- Case 2: PSE Power Supply Voltage changes [1,2]
  - Happens during backup power function or equivalent events
  - PSE PS voltage changes from Vmin to Vmax causing positive current transient at the PD.
- Objectives [1,2,3] :
  - We would like to keep the port ON for the duration of this transient for max $\{T_{LIM\_MIN}\}$ i.e Worst Case T_{LIM_MIN}.
  - To find I_{LIM} v.s. T_{LIM} operating envelope

Who Affects T_{LIM_MIN}

- Case 1: Cross Regulation Effects [1,2]
- PSE port voltage is changed by all (N-1) ports going from Full Load to minimum load.

$$dVcross = Iport \cdot (N-1) \cdot \frac{Rchannel + Rcontrol}{(N-1)} + Iport \cdot (N-1) \cdot Rs =$$

$$Iport \cdot (Rchannel + Rcontrol) + Iport \cdot (N-1) \cdot Rs =$$

$$dVcross = Iport \cdot [(Rchannel + Rcontrol) + (N-1) \cdot Rs]$$

Who Affects T_{LIM_MIN}

- Case 2: PSE Power Supply Voltage changes [1,2]
- PSE PS Voltage may change from 50V to 57V (802.3af) or from 44V to 57V (802.3at):
  - ➔ dV=7V max for 802.3af
  - ➔ dV=13V max for 802.3at
- At time constants affected by
  - PS output resistance/Capacitance : 0.08 Ω/300uF
  - Channel Resistance / Cpd, PD diodes
  - PSE output current limit circuitry.
    - Longest T_{LIM} if $I_{LIM} = I_{LIM\_MIN} = I_{CUT\_MAX}$
      - 802.3af : 0.4A
      - 802.3at : 0.828A (=1.15*0.72A)

Finding the Worst Case conditions

- Worst Case PSE PS voltage changes

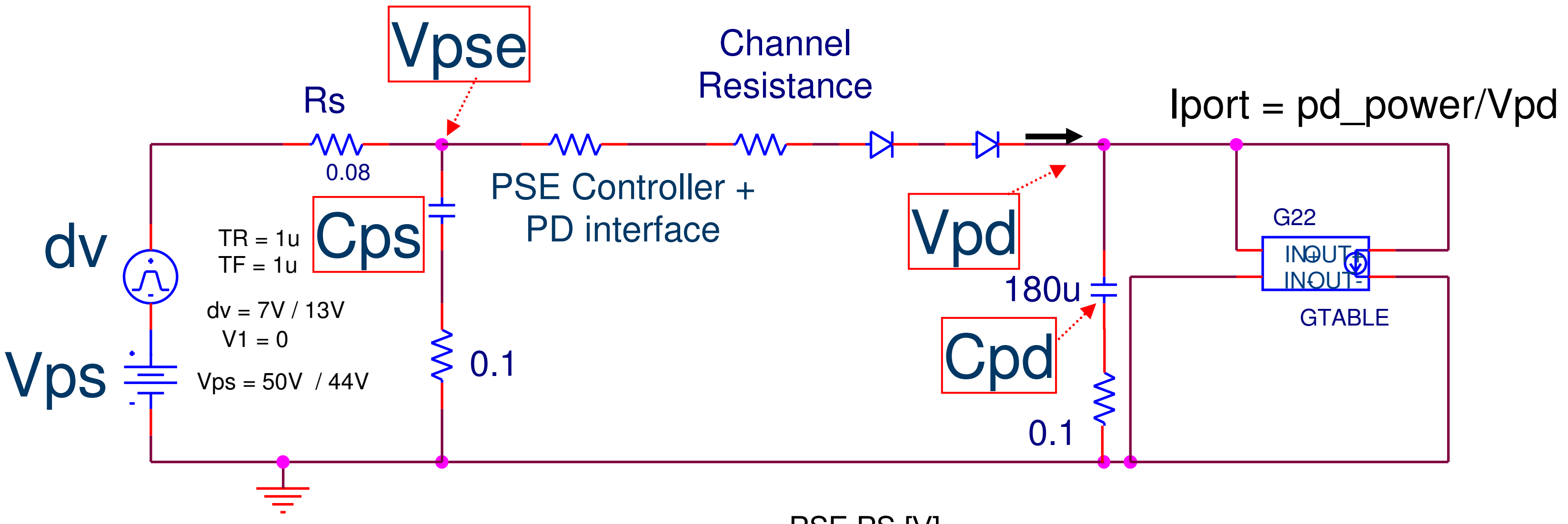
- By definition (load regulation), dV>dVcross hence the worst case is Case 2.

- Since in 802.3af , dV=13V hence the worst case is:

Case 2 (PSE Power Supply change) in 802.3af

- ➔ We can simplify the model to the single port model connected to a PSE PS.

Who Affects T_{LIM_MIN} – Simplified Model



From Vport Ad hoc data[1]:

Rs=60 – 80m Ω

PSE controller= 0.9 – 3.2 Ω

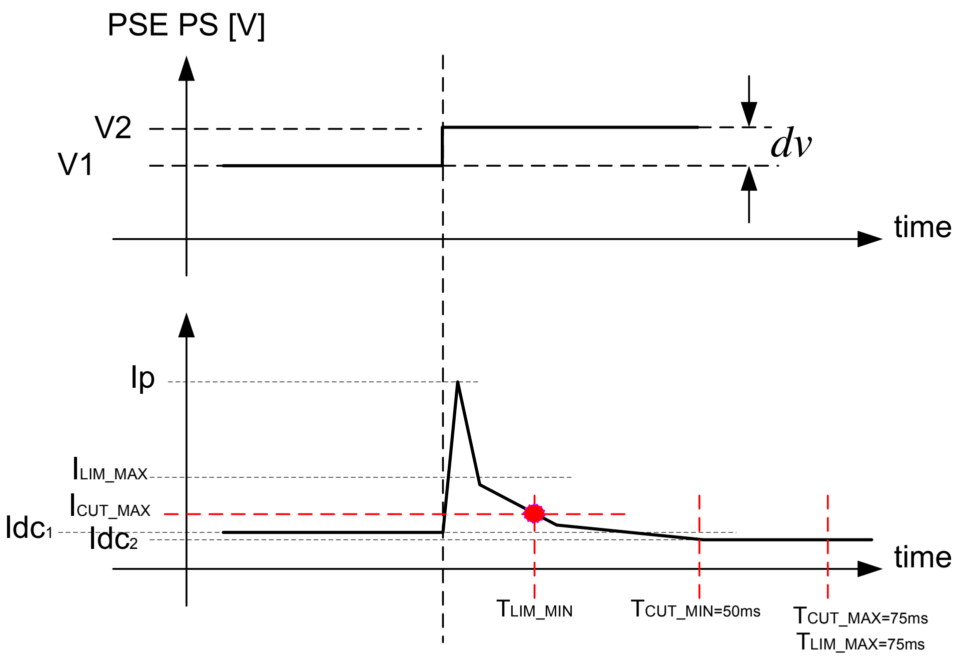
Channel Resistance=0 – 12.5Ω

Cpd=5 -180uF

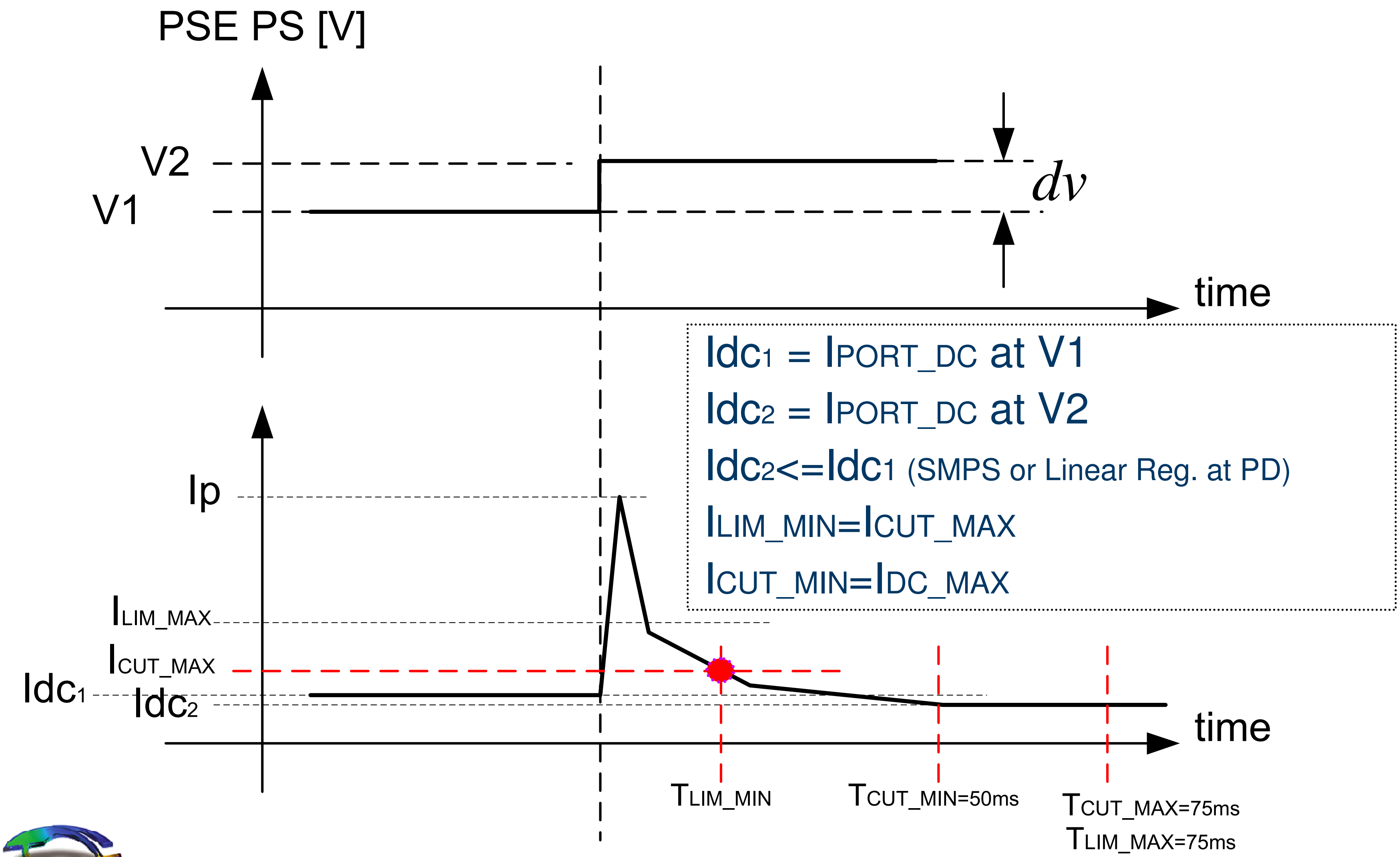
Additional data:

PD Interface: 0.5 – 1Ω

Cps=1uF/Watt=300uF/300Watts



Who Affects T_{LIM_MIN} – Simplified Model



Analytical Derivation of TLIM – w/o linear current limit

$$I(t=T_{LIM}) = I(t=\infty) - \left(I(t=\infty) - I(t=0)\right)\cdot \exp^{-t=T_{LIM}/\tau}$$

$$I(t=T_{LIM}) = Icut\_\max - Idc$$

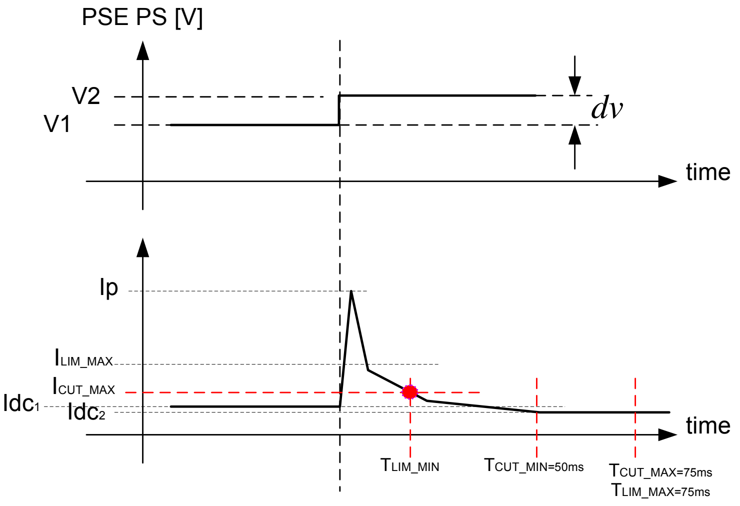
$$I(t=\infty) = Idc \;\; - Idc \;\; = 0$$

$$I(t=0) = Ip - Idc$$

$$Ip = \frac{dv - 2\cdot(Vdf_1 - Vdf_2)}{\sum R} + Idc$$

$$Vdf_i = PD\ diode\ voltage\ drop\ at\ Idc_i$$

$$\tau = Cpd\cdot\sum R$$



$$I(t) = I(t=\infty) - \left(I(t=\infty) - I(t=0)\right)\cdot \exp^{-t/\tau}$$

$$Icut\_\max - Idc \;\; = 0 - \left(0 - \left(Ip - Idc \;\;\right)\right)\cdot \exp^{-TLIM\_MIN/\tau}$$

$$\left(Icut\_\max - Idc \;\;\right) = \left(Ip - Idc \;\;\right)\cdot \exp^{-TLIM\_MIN/\tau}$$

$$T_{LIM\_MIN} = -\tau\cdot\ln\left[\frac{(Icut\_\max - Idc)}{(Ip - Idc)}\right]$$

Analytical Derivation of T_{LIM} – w/o linear current limit

- Since Idc is a superposition of Idc1 at V1 and Idc2 at V2 (negative load resistance) then the filtering effect of the Channel RC network is averaging the timing which results with:

$$T_{LIM\_MIN} \approx \frac{-\tau \cdot \ln\left[\frac{(Icut\_\max - Idc_1)}{(Ip - Idc_1)}\right] - \tau \cdot \ln\left[\frac{(Icut\_\max - Idc_2)}{(Ip - Idc_2)}\right]}{2}$$

Analytical Derivation of T_{LIM} – w/o linear current limit

Worst Case Ip:

$$Ip\_\max = \frac{dv - 2\cdot(Vdf_1 - Vdf_2)}{\min\left\{\sum R\right\}} = \frac{Vps\_\max - Vps\_\min - 2\cdot(Vdf_1 - Vdf_2)}{\min\left\{\sum R\right\}}$$

Worst Case Idc_i:

$$Idc_i = \frac{2\cdot Ppd}{Vpse_i + \sqrt{{Vpse_i}^2 - 4\cdot Ppd\cdot\sum R}}$$

$$Worst\ Case\ I_{CUT\_MAX} = 1.15\cdot Idc_{\max}$$

$$Worst\ Case\ Cpd = 180uF$$

$$Worst\ Case\ \tau = Cpd\cdot\max\left\{\sum R\right\}$$

Analytical Derivation of TLIM – w/o linear current limit

$$\max\left\{\sum R\right\} = Rchannel\_\max + Rcontroller\_\max + Rpd =$$

$$12.5\Omega + 3.2\Omega^{1} + 1\Omega = 16.7\Omega$$

$For\ 802.3at:$

$$Idc_1 = \frac{2\cdot Ppd}{Vpse1 + \sqrt{Vpse_1^{\,2} - 4\cdot Ppd\cdot\sum R}} = \frac{2\cdot 27.4}{50 + \sqrt{50^2 - 4\cdot 27.4\cdot 16.7}} = 0.722A$$

$$Idc_2 = \frac{2\cdot Ppd}{Vpse_2 + \sqrt{Vpse_2^{\,2} - 4\cdot Ppd\cdot\sum R}} = \frac{2\cdot 227.4}{57 + \sqrt{57^2 - 4\cdot 27.4\cdot 16.7}} = 0.579A$$

$For\ 802.3af:$

$$Idc_1 = \frac{2\cdot Ppd}{Vpse1 + \sqrt{Vpse_1^{\,2} - 4\cdot Ppd\cdot\sum R}} = \frac{2\cdot 12.7}{44 + \sqrt{44^2 - 4\cdot 12.7\cdot 16.7}} = 0.330A$$

$$Idc_2 = \frac{2\cdot Ppd}{Vpse_2 + \sqrt{Vpse_2^{\,2} - 4\cdot Ppd\cdot\sum R}} = \frac{2\cdot 12.7}{57 + \sqrt{57^2 - 4\cdot 12.7\cdot 16.7}} = 0.240A$$

$$T_{LIM\_MIN(at\ ,\ af)} \approx -\frac{\tau}{2}\cdot\left[\ln\left[\frac{(Icut\_\max - Idc_1)}{(Ip - Idc_1)}\right] + \ln\left[\frac{(Icut\_\max - Idc_2)}{(Ip - Idc_2)}\right]\right] = 2.7ms/6ms$$

Worst Case Analytical Results, w/o linear current limit – Summary

(Cps=0 for comparison purposes, Actual peak current is ~0.366*Ipeak due to Rs, Cps filter)

	802.3at		802.3af	
	$\sum R \to min.$	$\sum R \to max.$	$\sum R \to min.$	$\sum R \to max.$
PD diodes dynamic drop	0.4	0.4	0.17	0.17
Vpse_min	50	50	44	44
Vpse_max	57	57	57	57
Ppd	27.4	27.4	12.7	12.7
Rch	0	12.5	0	12.5
Rinteface PSE	0.9	3.2	0.9	3.2
Rinterface PD	1	1	1	1
Total R	1.9	16.7	1.9	16.7
Cpd	0.00018	0.00018	0.00018	0.00018
Icut_max	0.828	0.828	0.4	0.4
dV	6.6	6.6	12.83	12.83

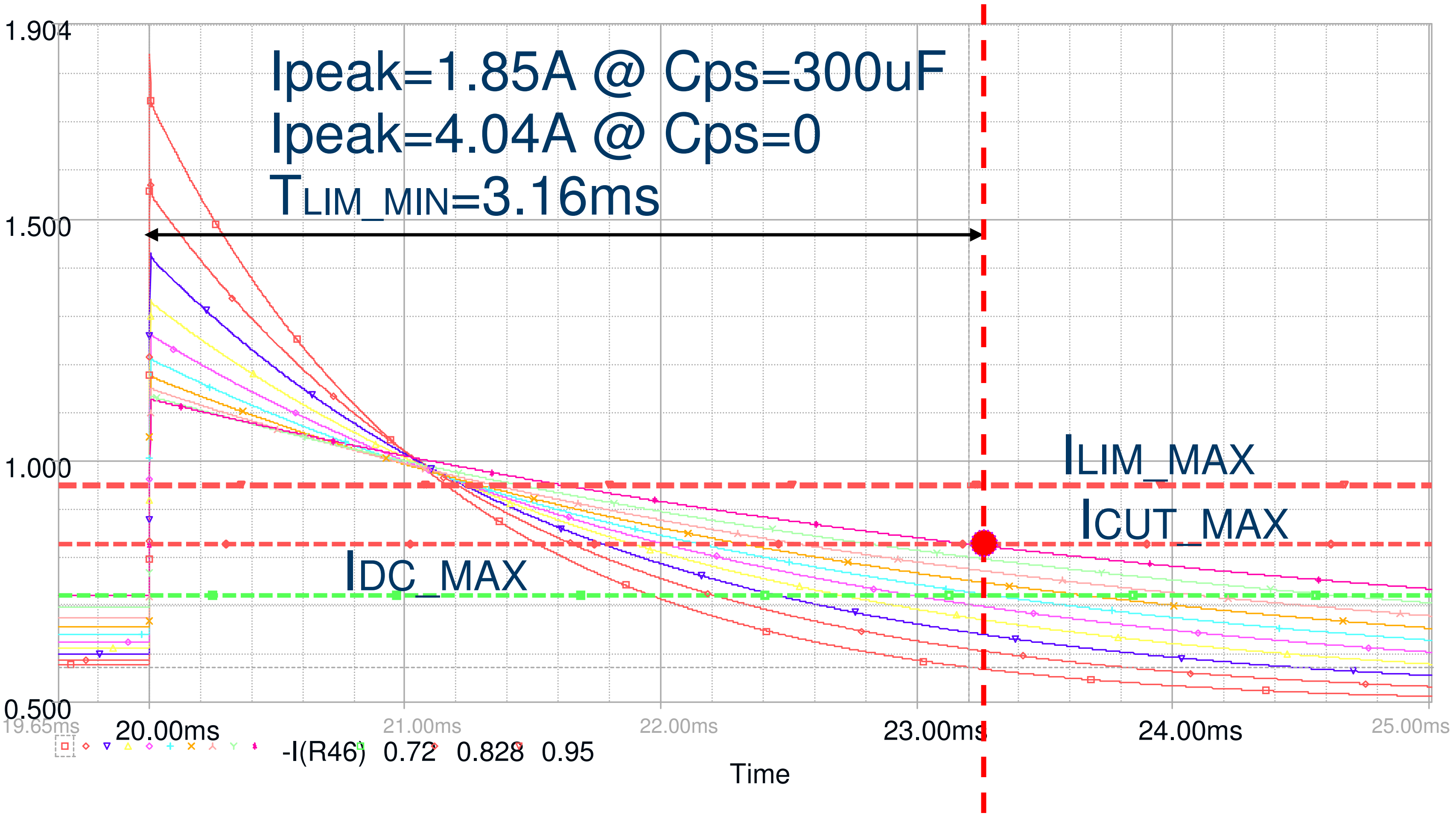
Worst Case Analytical/Simulation Results, w/o linear current limit – Summary

(Cps=0 for comparison purposes, Actual peak current is ~0.366*Ipeak due too Rs, Cps filter)

	802.3at		802.3af	
	$\sum R \rightarrow \min$	$\sum R \rightarrow \max$	$\sum R \rightarrow \min$	$\sum R \rightarrow \max$
Calculated Results				
Idc at Vpse_min [A]	0.560	0.722	0.292	0.330
Idc at Vpse_max [A]	0.489	0.579	0.224	0.240
di [A]	3.474	0.395	6.753	0.768
Ipeak [A]	4.034	1.117	7.045	1.098
Tlim_min [sec]	0.00084	0.0027	0.0013	0.0060
Simulation Results				
Idc at Vpse_min [A]	0.552	0.72	0.304	0.349
Idc at Vpse_max [A]	0.479	0.569	0.231	0.248
di [A]	3.487	0.416	6.522	0.774
Ipeak [A]	4.039	1.136	6.827	1.122
Tlim_min [sec]	0.000865	0.00316	0.00138	0.0059
Simulation/Calculation Ratio				
Idc at Vpse_min [A]	0.99	1.00	1.04	1.06
Idc at Vpse_max [A]	0.98	0.98	1.03	1.03
di [A]	1.00	1.05	0.97	1.01
Ipeak [A]	1.00	1.02	0.97	1.02
Tlim_min [sec]	1.03	1.18	1.04	0.99

Simulation Results:

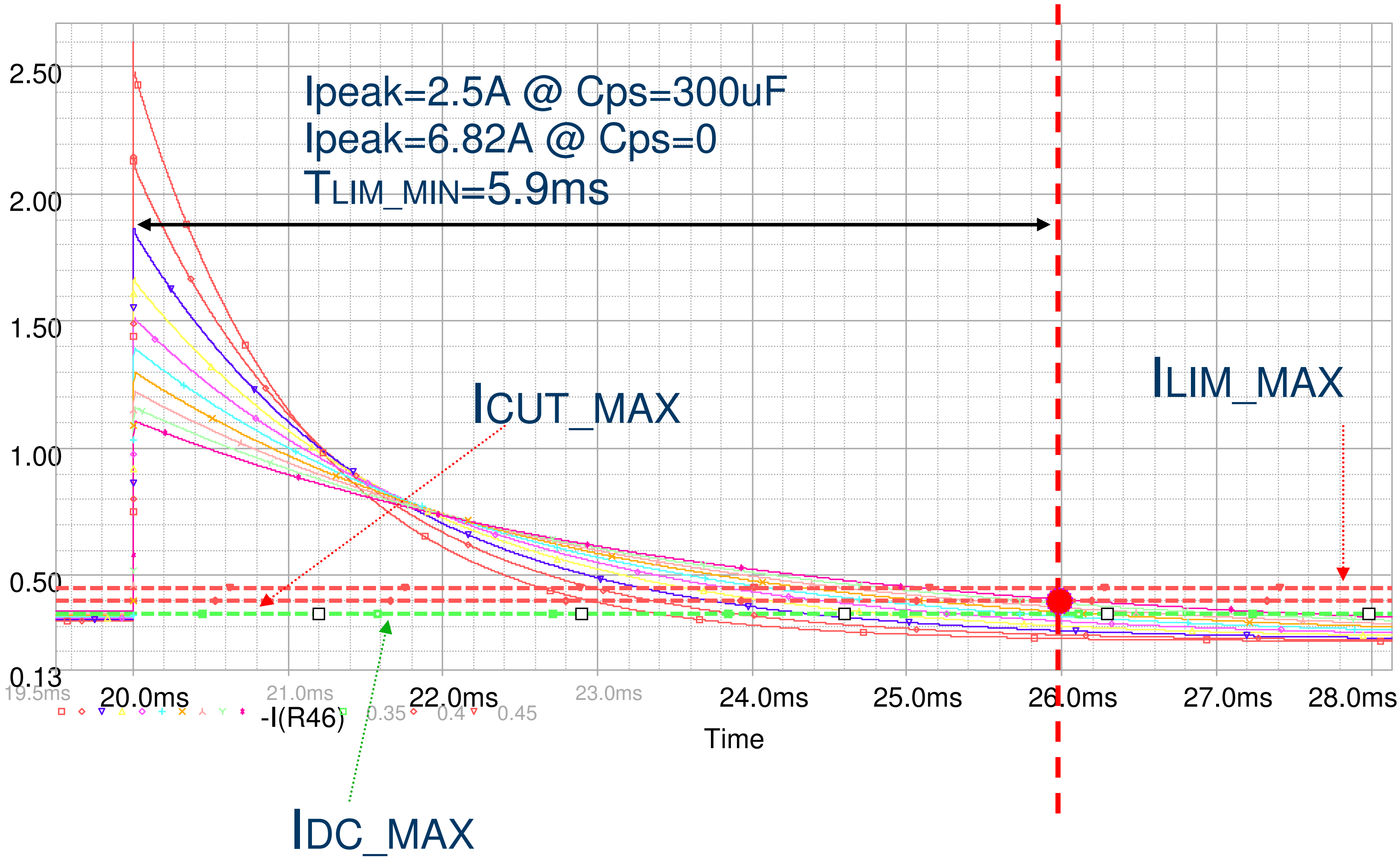
Cpd=180uF, dv=57V-50V=7V, PSE/PD interface at max. Resistance, Channel length varies 0 to 100m



(Tlim_min=2.7ms in analytical derivation)

Simulation Results:

Cpd=180uF, dv=57V-44V=13V, PSE/PD interface at max. Resistance, Channel length varies 0 to 100m



(Tlim_min=6ms in analytical derivation)

Worst Case Analytical Results, with linear current limit

$$di \cdot dt = Cpd \cdot dv$$

$$dt = \frac{Cpd \cdot dv}{di} = \frac{Cpd \cdot dv}{(I_{LIM\_MIN} - Ipd(t))}$$

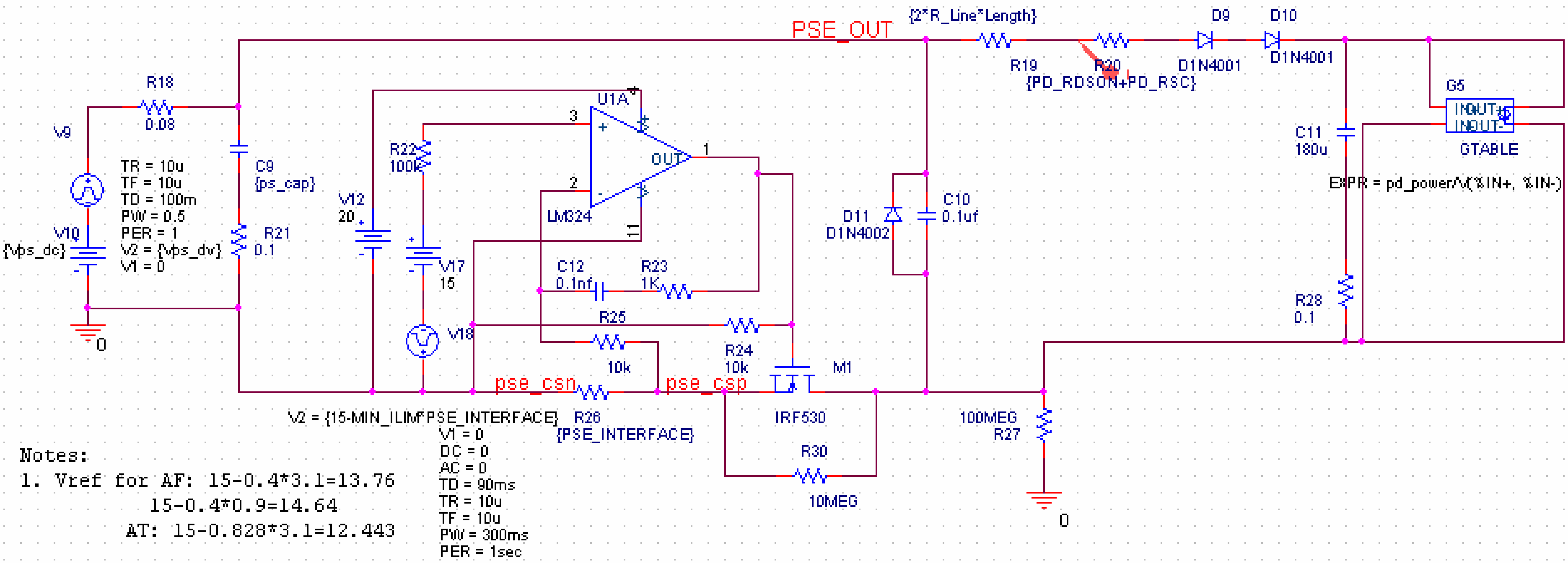
$$TLIM\_MIN = \int_{v1}^{v2} \left(\frac{Cpd \cdot dv}{di} \right) = \int_{v1}^{v2} \left(\frac{Cpd \cdot dv}{I_{LIM\_MIN} - \frac{Ppd}{Vpd(t)}} \right)$$

$$v1 = Vpse\_\min - ILIM\_MIN \cdot \sum R = 36V \ , \ 39.65V \ \ (af / at)$$

$$v2 = Vpse\_\max - ILIM\_MIN \cdot \sum R = 39V \ , \ 46.65V \ \ (af / at)$$

- Solving the above.. Or simulating it (easier) ends with the following results

TLIM_MIN with constant current limit

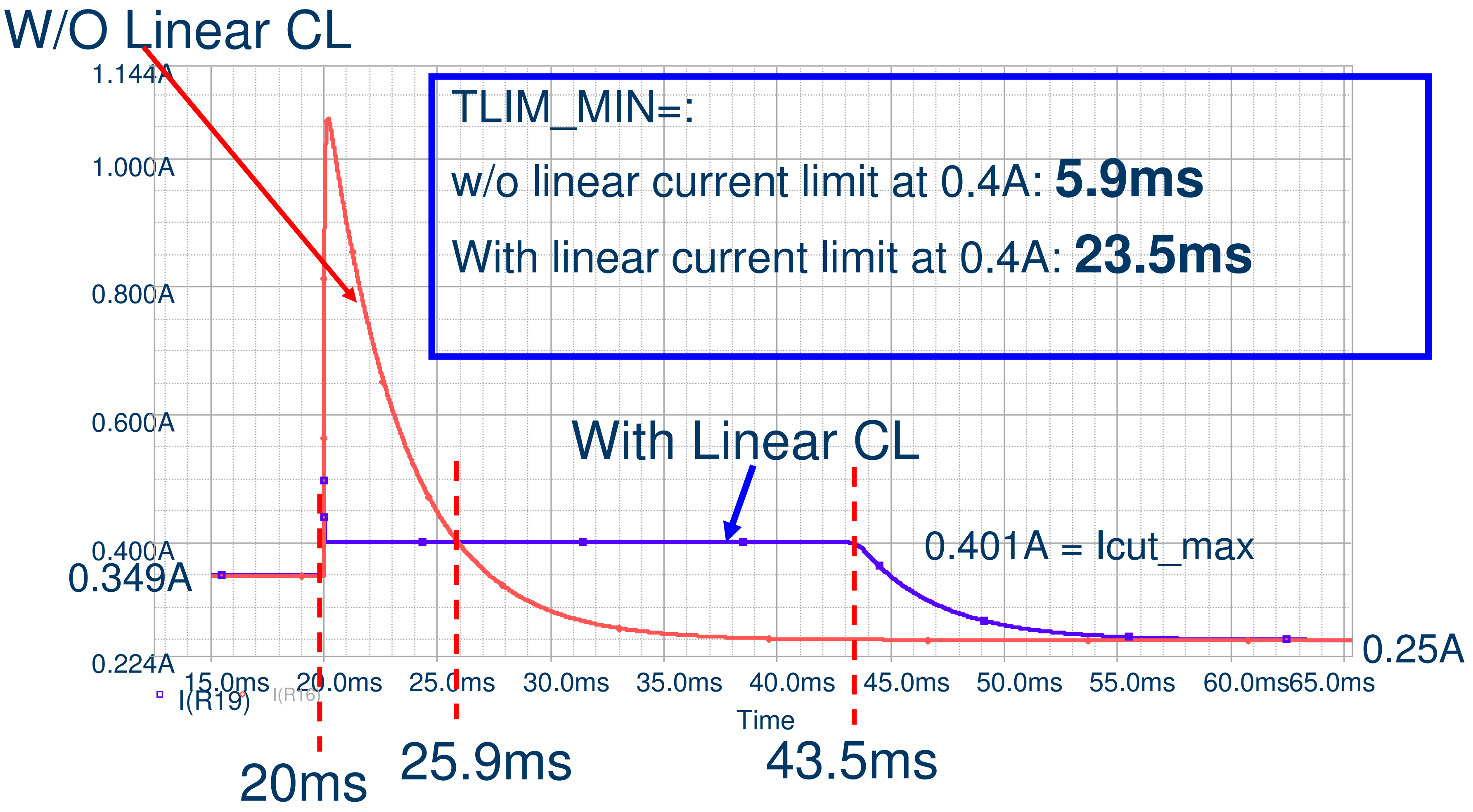


Notes:

1. Vref for AF: 15-0.4*3.1=13.76
15-0.4*0.9=14.64
AT: 15-0.828*3.1=12.443

802.3af: With and w/o Linear current limit

100m channel, + 4.2Ω PSE+PD interface resistance, 44V to 57V



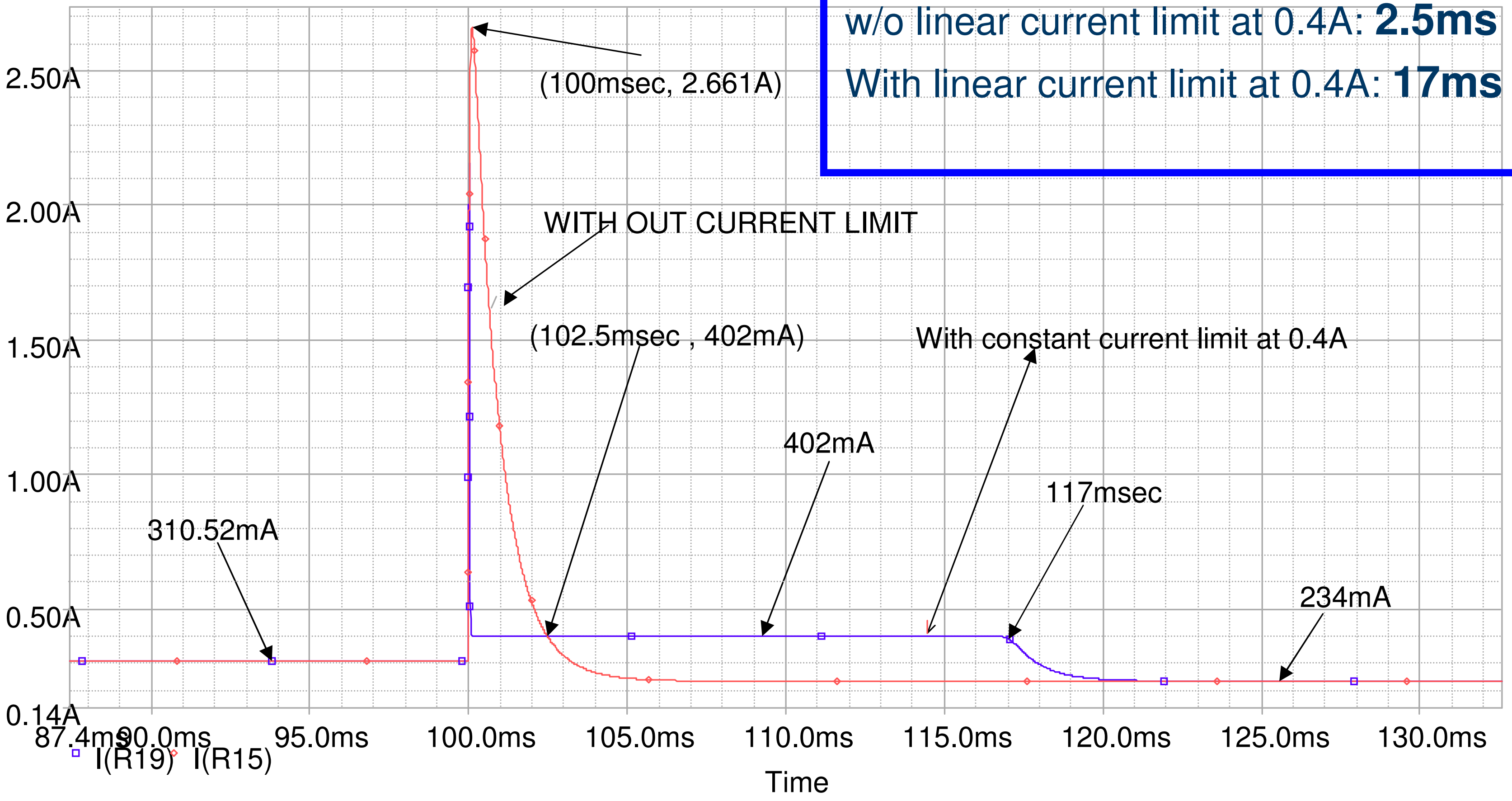
802.3af: With and w/o Linear current limit

1m channel, + 4.2Ω PSE+PD interface resistance, 44V to 57V

TLIM_MIN=:

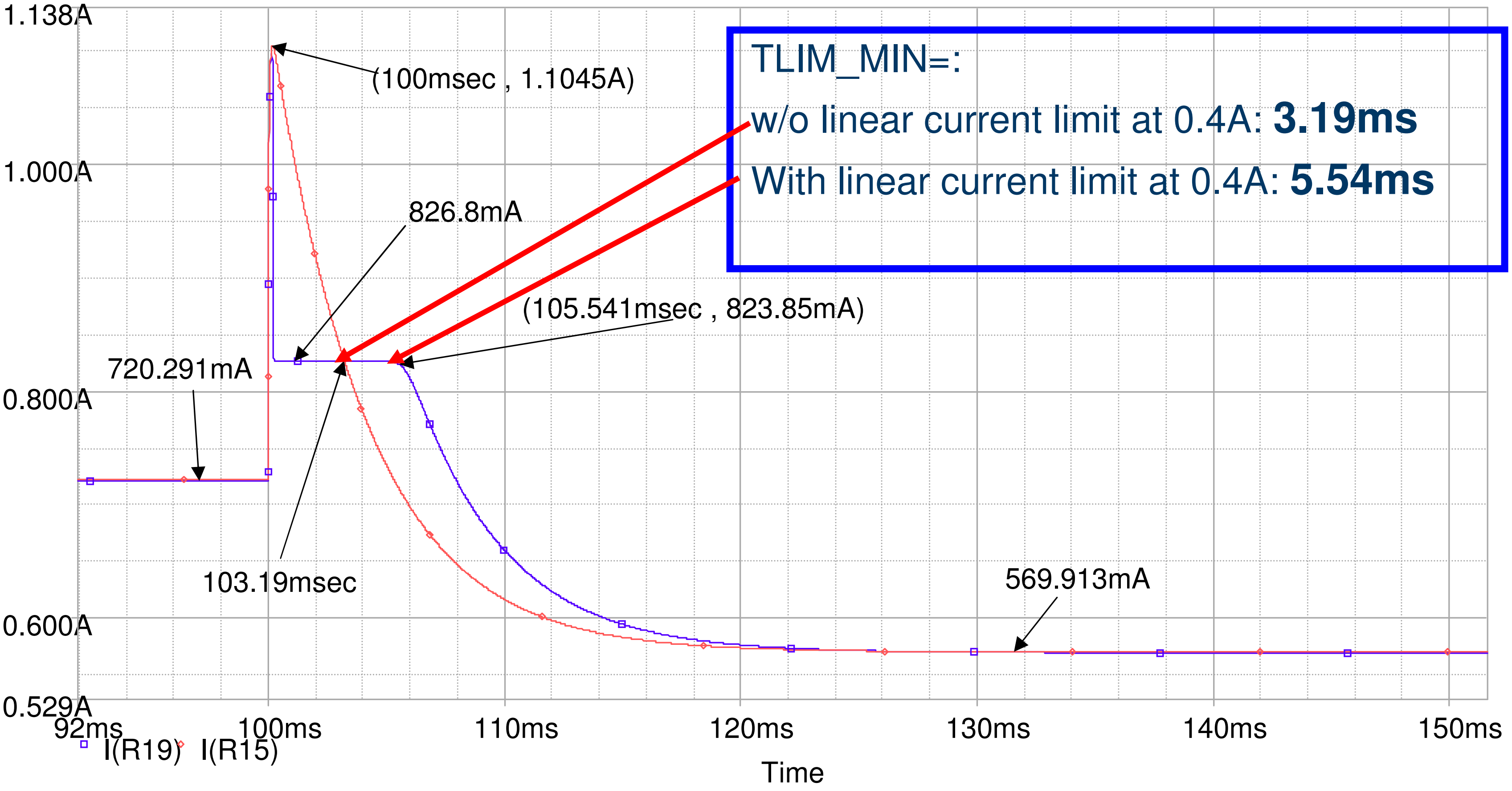
w/o linear current limit at 0.4A: **2.5ms**

With linear current limit at 0.4A: **17ms**



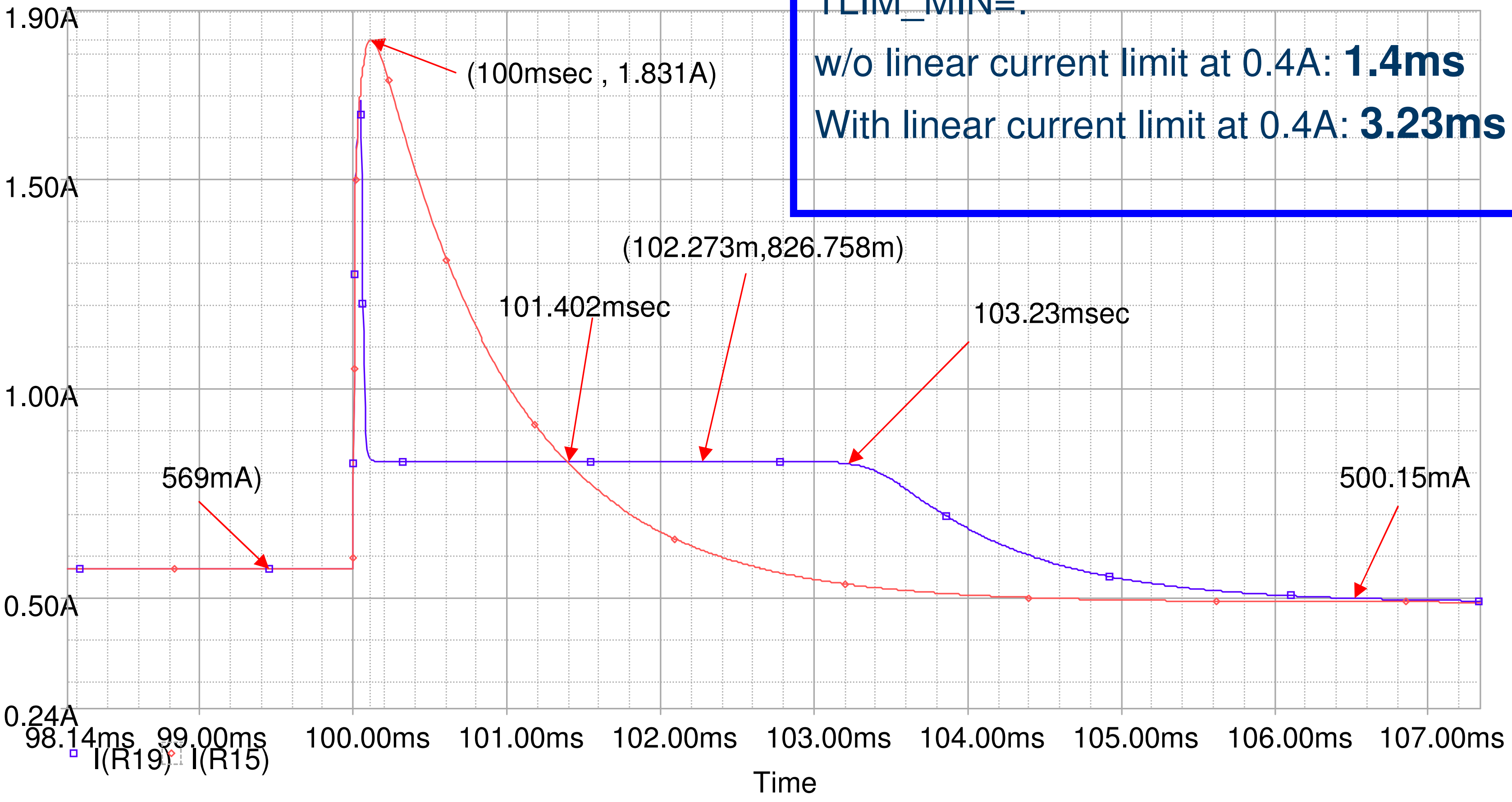
802.3at: With and w/o Linear current limit

100m channel, + 4.2Ω PSE+PD interface resistance, 50V to 57V



802.3at: With and w/o Linear current limit

1m channel, + 4.2Ω PSE+PD interface resistance, 50V to 57V

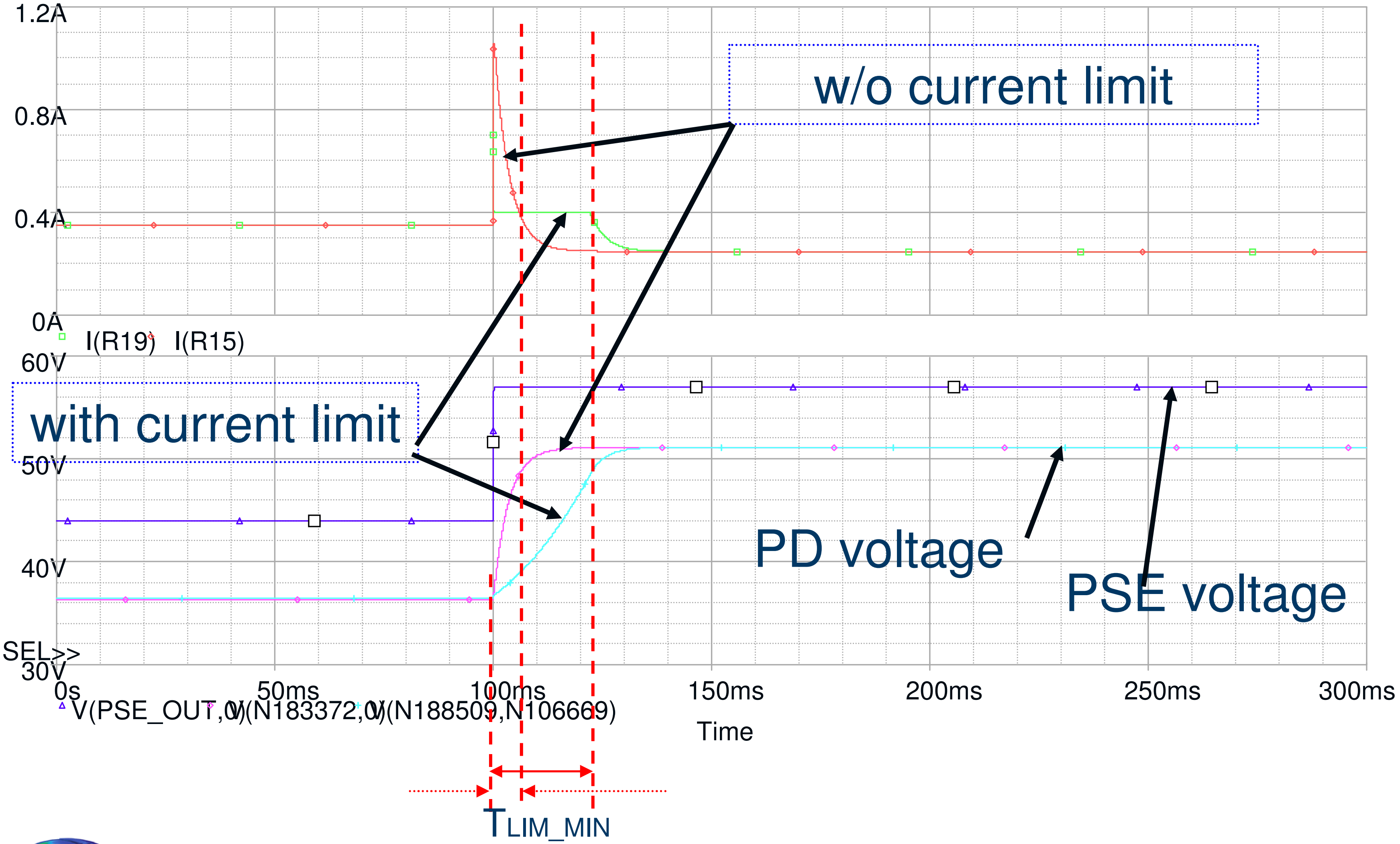


TLIM_MIN=:

w/o linear current limit at 0.4A: **1.4ms**

With linear current limit at 0.4A: **3.23ms**

The Big Picture: 802.3af, Long Cable, Max. PSE/PD Interface Resistance



T_{LIM_MIN} summary in all PSE implementations at $I_{LIM\_MIN}=I_{CUT\_MAX}$, Constant Power Model at PD

	With Constant Current limit at PSE. $I_{LIM\_MIN}=I_{CUT\_MAX}$=0.828A / 0.4A dV = 7V / 13V R_Interface (PSE+PD=3.2+1=4.2Ω)		W/O current limit T_{LIM_MIN} Crossing point: $I_{LIM\_MIN}=I_{CUT\_MAX}$=0.828A / 0.4A dV = 7V / 13V R_Interface (PSE+PD=3.2+1=4.2Ω)	
	802.3at [msec]	802.3af [msec]	802.3at [msec]	802.3af [msec]
Short Cable (1m)	3.23	17	0.87	1.38
Long Cable (100m)	5.54	23.5	3.16	5.9
Worst case	5.54	23.5 17.43 (R_interface=1.9 Ω)	3.16	5.9

Sanity Check

- In 802.3af dv=13V
- In 802.3atdv=7V
- ➔ Ipeak (AF) > Ipeak (AT) ➔ longer TLIM in 802.3af

- In 802.3af $I_{CUT\_MAX}=I_{LIM\_MIN}=0.4A$
- Max Idc=0.35A
- Initial Charging current = 0.4A - 0.35A=0.05A
- In 802.3at $I_{CUT\_MAX}=I_{LIM\_MIN}=0.828A$
- Max Idc=0.72A
- Initial Charging current = 0.828A - 0.72A=0.108A
- ➔ Charging current (AF) < Charging current (AT) ➔ longer TLIM in 802.3af
- ➔ It get's worse with longer channel and / or increased PSE/PD interface losses

Proposal – part 1

- TLIM_MIN = 5.9ms for 802.3at
- TLIM_MIN=23.5ms for 802.3af
- If t<TLIM_MIN port is still ON as long as PD is within operating voltage range. If not, Port can be OFF at any time but not later then 75ms.

- Supports worst case PSE PS voltage changes, losses etc.
- Covers both 802.3af and 802.3at

Proposal – part 2

$$ILIM\_MAX(0 < t \le 25uS) = 25A$$

$$ILIM\_MAX(25uS < t \le T_{LIM\_MIN}) = \sqrt{\frac{0.0225}{t}}$$

$$ILIM\_MAX(T_{LIM\_MIN} < t \le 75ms) = ILIM\_MAX$$

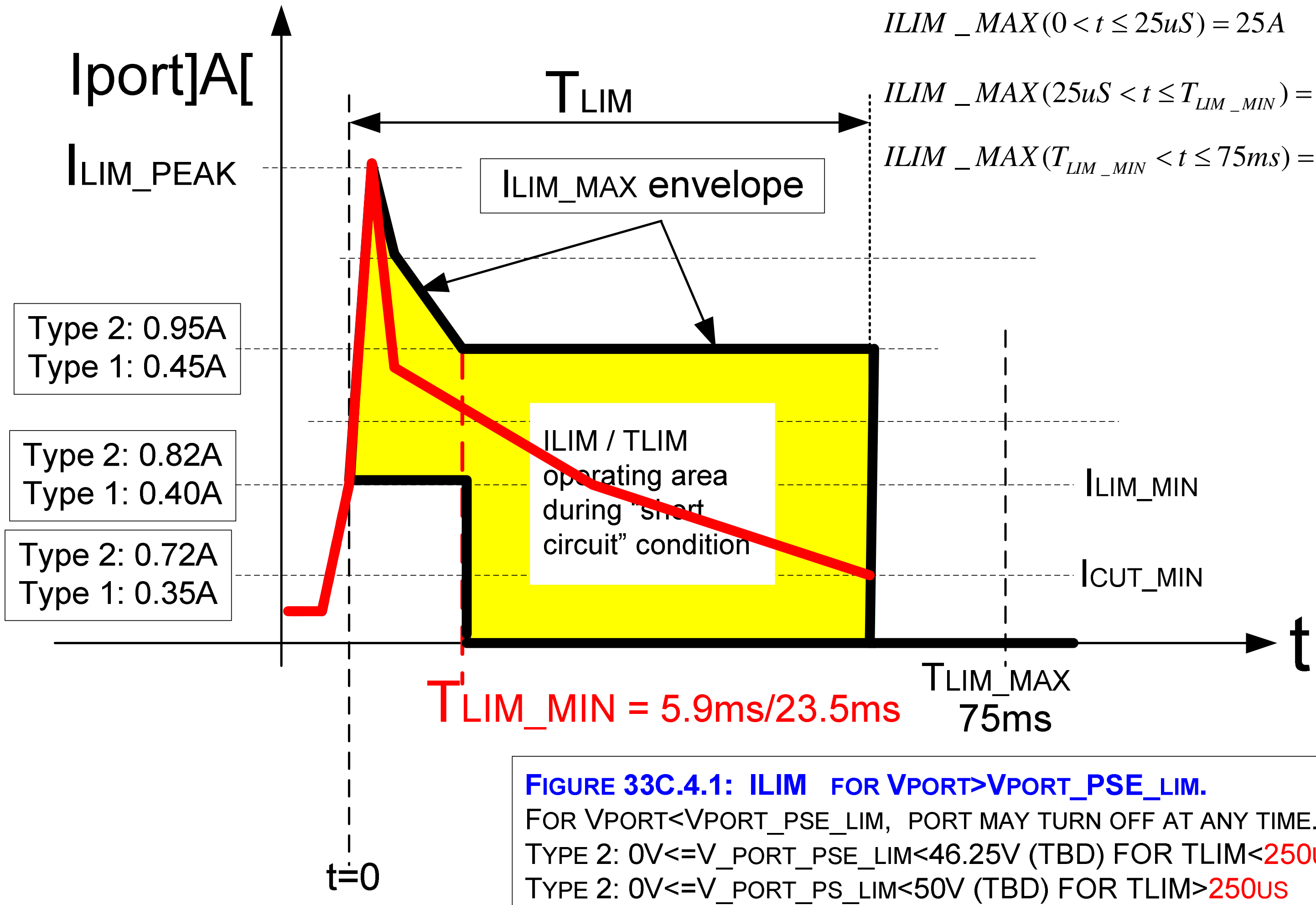


FIGURE 33C.4.1: ILIM FOR VPORT>VPORT_PSE_LIM.
FOR VPORT<VPORT_PSE_LIM, PORT MAY TURN OFF AT ANY TIME.
TYPE 2: 0V<=V_PORT_PSE_LIM<46.25V (TBD) FOR TLIM<250US
TYPE 2: 0V<=V_PORT_PS_LIM<50V (TBD) FOR TLIM>250US
TYPE 1: 0V<=VPORT_PSE_LIM<44V (TBD)
SEE 33C.4 FOR IEEE802.3AF/AT INRUSH CURRENT

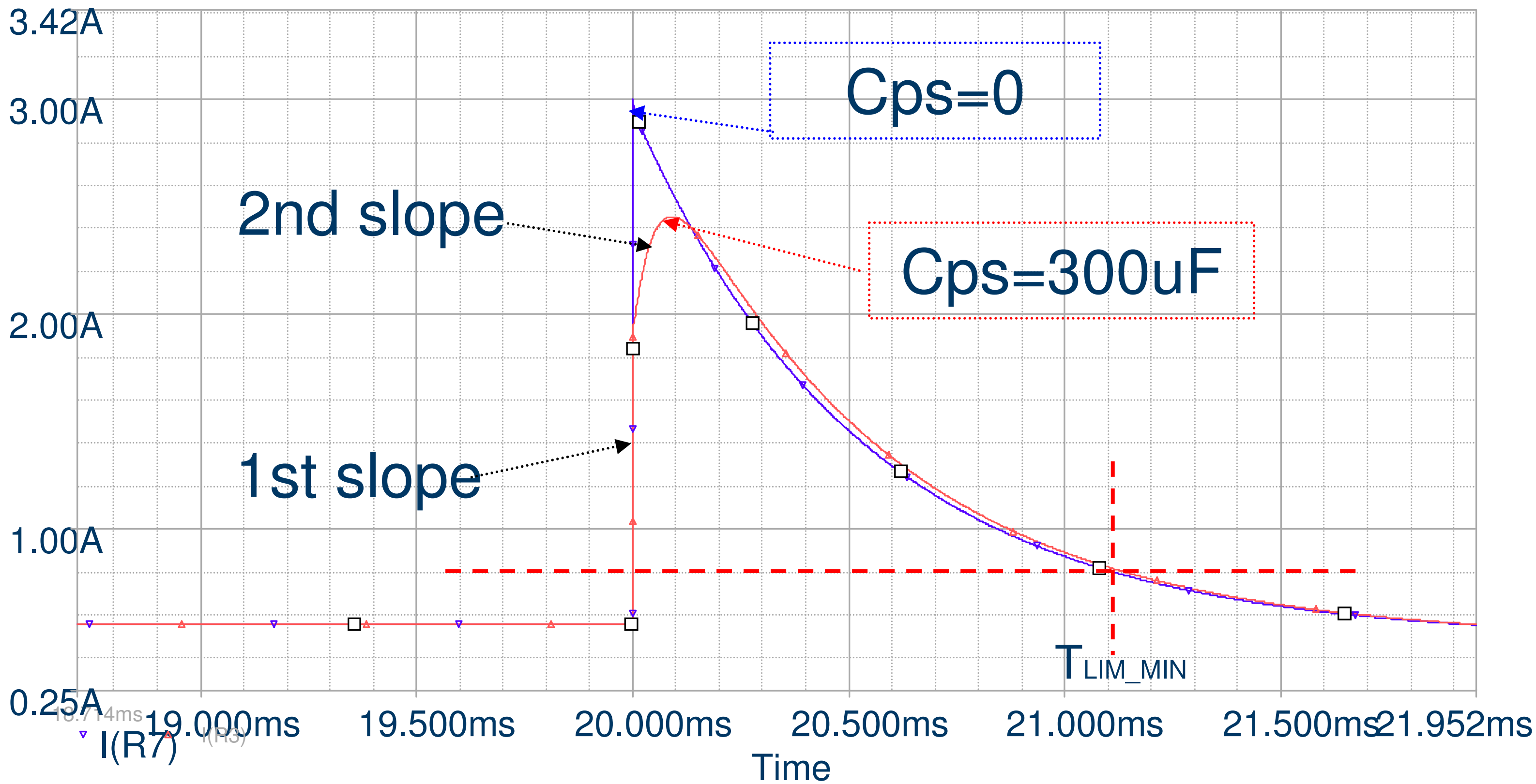
Questions/Discussion

References

- 1. http://www.ieee802.org/3/at/public/mar07/schindler_2_0307.pdf
- 2. http://www.ieee802.org/3/af/public/jul01/darshan_2_0701.pdf
- 2.1. http://www.ieee802.org/3/af/public/documents/proposal_for_Startup_line_load_cross.pdf
- 2.2. http://www.ieee802.org/3/af/public/documents/Port_to_Port_Cross_Reg.pdf
- 3. http://www.ieee802.org/3/at/public/mar07/darshan_1_0307.pdf

Additional Reference Material

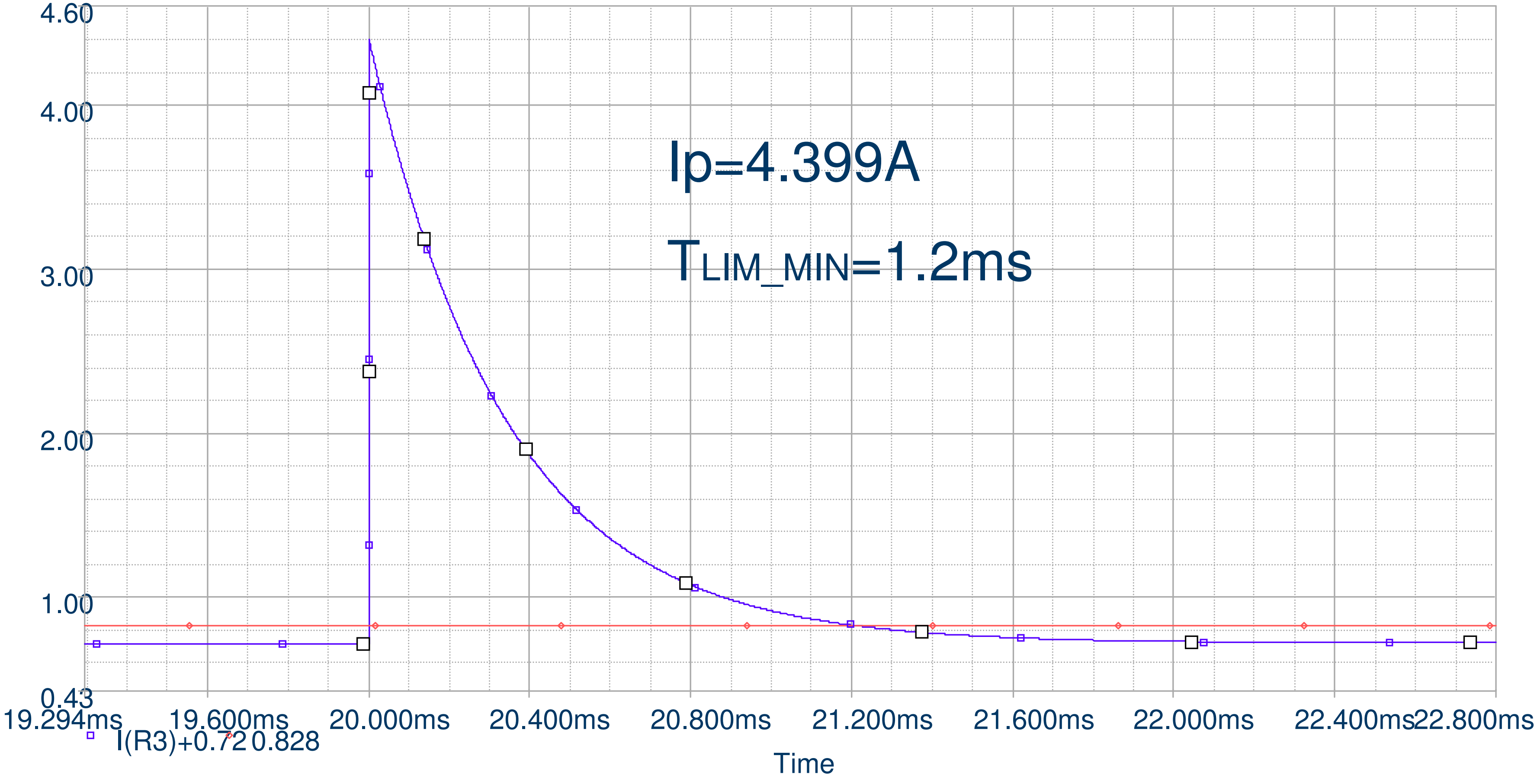
How Cps affects results



Cps affects only the peak current (at the first 150uS @ Cps=300uF)

and not affect T_{LIM_MIN}

Testing SIM vs Equation



PSE PS output capacitance value

$$I = \frac{P}{V}, \quad dv << V$$

$$I \cdot t_{CL} \approx C \cdot dv$$

$$\frac{P}{V} \cdot t_{CL} \approx C \cdot dv$$

$$\frac{t_{CL}}{V \cdot dv} \approx \frac{C}{P}$$

$$dv = 2$$

$$t_{CL} = 100u\sec$$

$$V = 50V$$

$$\frac{C}{P} \approx \frac{100u\sec}{2V \cdot 50V} = \frac{1uF}{1Watt}$$

Effects of transient Current on 1206 resistor – Discussion

- Work is not done yet.
- It looks that 1206 can work under the limitations of 33C.4.
  - Starting point (from 1206 data sheet):
  - At 6ms, Ppeak=5W. ➔ I=(5W/1Ω)^0.5
  - Ipeak =~ 2*I (average of transient)
  - Using 2 resistors in parallel allows 4*I=8.9A
  - According to 33C.4:
  - I=(0.025/0.006)^0.5=2.04A < 8.9A ➔ we are good.
- Up to 25us we need to limit peak power to 40W. We need more work to verify it.
- <u>Do we have info regarding damaged 1206 in PDs?</u>