# Vport ad hoc Current Limits
# May 2007

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| **James Blanc** | **Indep. VC investigation** | **Youhoa Xi** | **National Semiconductor** |
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Four ad hocs with an average attendance of 16 people since the last IEEE meeting.
People that attended since the last IEEE meeting are shown in **bold.**

# Agenda

- **SELV correction.**
- **Current limits.**
- **Next step.**

# SELV Correction

- **IEC 60950, 3rd edition, 1999-04**

  **1.2.13.4 DC VOLTAGE: The average value of a voltage (as measured by a moving coil meter) having a peak-to-peak ripple not exceeding 10 % of the average value.**

- **IEEE 802.3-2005, Table 33-6 PSE PI parameters**

  **V_open; Vpp; Min: 1.9 V;**
  **Max: 10% of the average value of $V_{Port}$, 44V < $V_{Port}$ < 60V.**

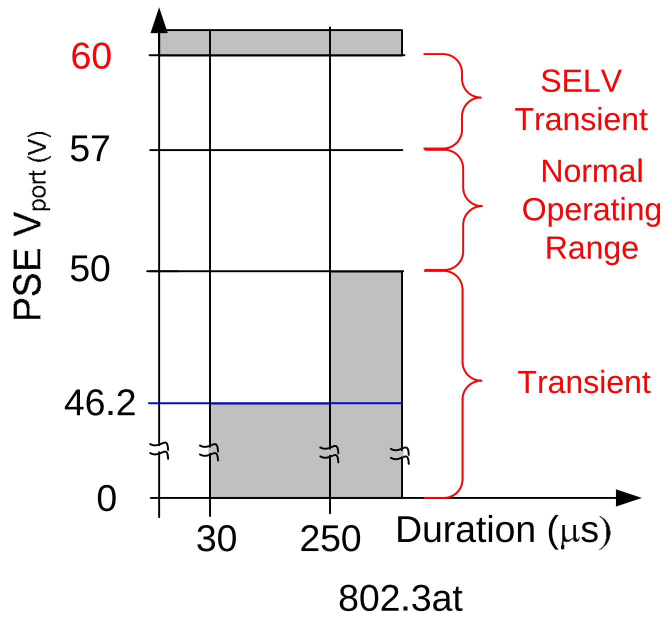
- **57 V x 10% = 5.7 Vpp, 57 V + 2.85sin($\omega$t)**

  **57 + 2.85 = 59.85 V, ~ 60 $V_{peak\_value}$**

# Proposal corrected for SELV

- **Propose a PSE PI voltage limit, for transients present more than 30 µs, of 7.6% below the PSE $V_{port\_min}$ level for less than a period of 250 µs ~~and 10% above the $V_{port\_max}$ level.~~**

**Remove this text and continue using existing SELV guidance.**



# Motion

**Move that:**

**The IEEE 802.3at Task Force adopt presentation schindler_5_28_07.pdf slides 4 to be incorporated in  the next P802.3at draft.**

**M: Fred Schindler**

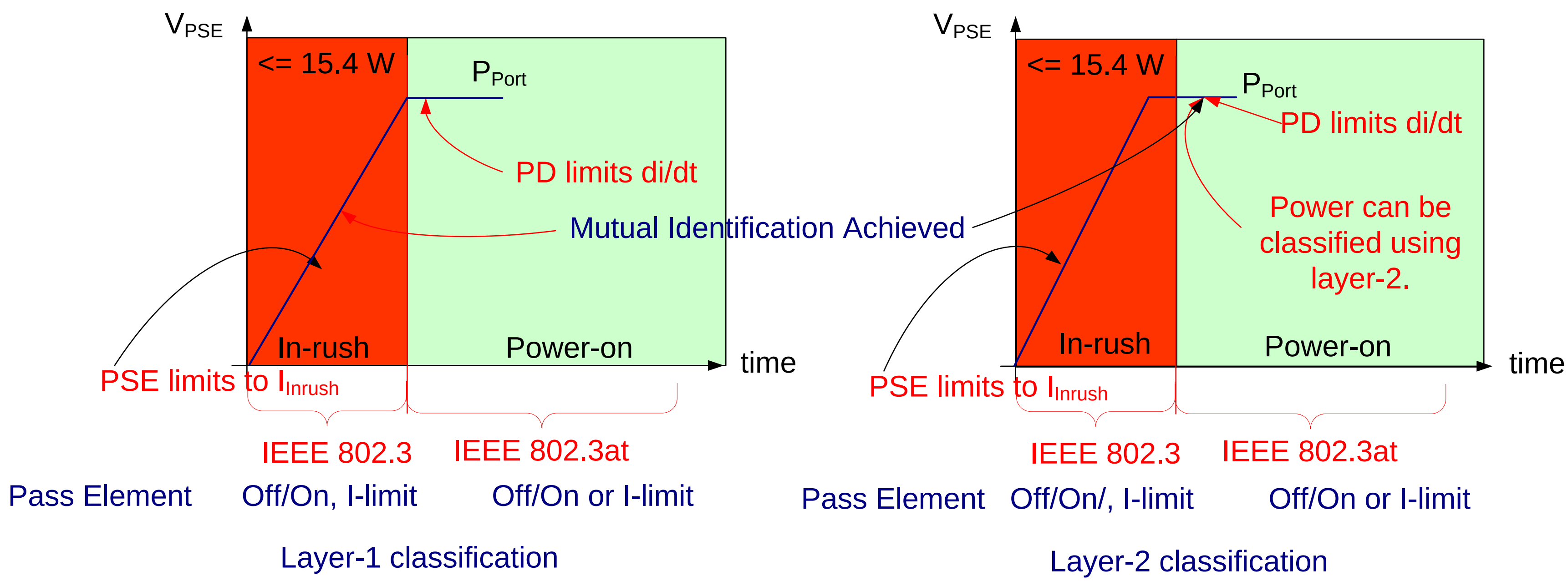
**S: Yair Darshan**

| **All Present** | **802.3 Voters** |
|---|---|
| **For:** | **For:** |
| **Against:** | **Against:** |
| **Abstain:** | **Abstain:** |

# IEEE 802.3 vs IEEE 802.3at

- **The legacy standard reused the in-rush current limits to address the power-on current limits.**
- **The proposed IEEE 802.3at standard:**
  - **Reuses the legacy in-rush current limits.**
  - **Raises power-on currents.**
  - **Limits PD di/dt rates during power-on.**
  - **Opens up the design space to allow:**
    - **Scaled legacy current thresholds**
    - **Aggressive fold back**
    - **An energy based limit**

# System In-rush and Power-on




| Parameter | | 802.3 | 802.3at |
|---|---|---|---|
| $I_{LIM}$ | max. | $\frac{450}{400}\ \frac{400}{350}\ \frac{P_{Port}}{V_{Port}}$ | New |
| | min. | $\frac{400}{350}\ \frac{P_{Port}}{V_{Port}}$ | |
| $I_{CUT}$ | max. | | |
| | min. | $\frac{P_{Port}}{V_{Port}}$ | |

# System Concerns being addressed by $I_{LIM}$

- **Situations that lead to a PSE dv/dt rate that causes excess PD current demand.**

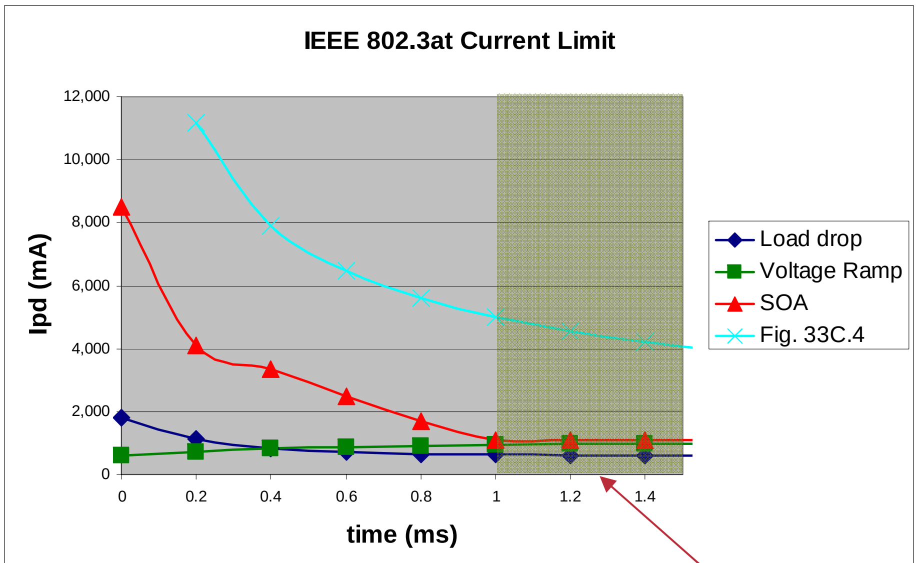
    **Multiple PDs reducing their load.**

    **A PSE supply voltage change.  ex/ Switching in a new power supply to deal with a power supply failure.**

# Collected Worst-case Current Limits

**Load drop: 47/48 ports, short channel 5 μF, 29.5 W PD.**

**PSE voltage ramp: short channel 180 μF, 29.5 W PD.**



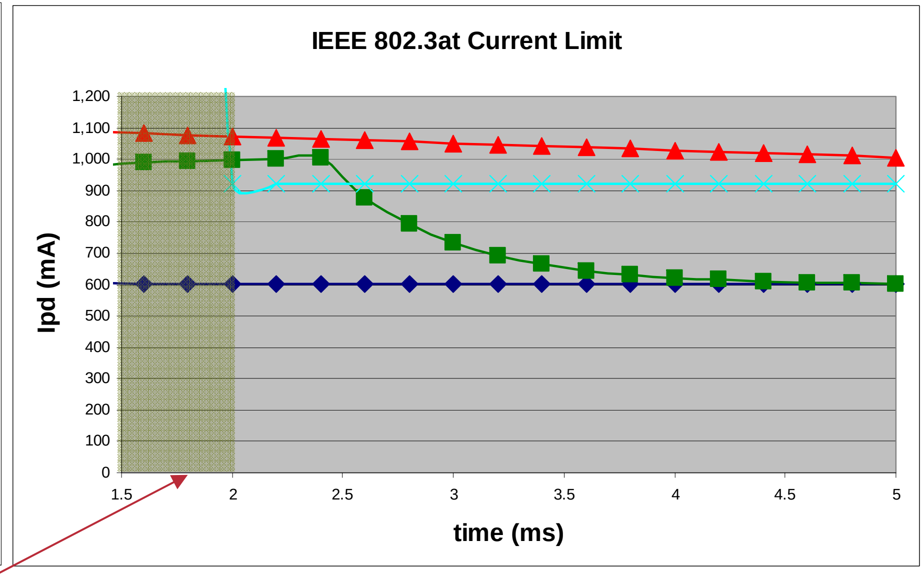
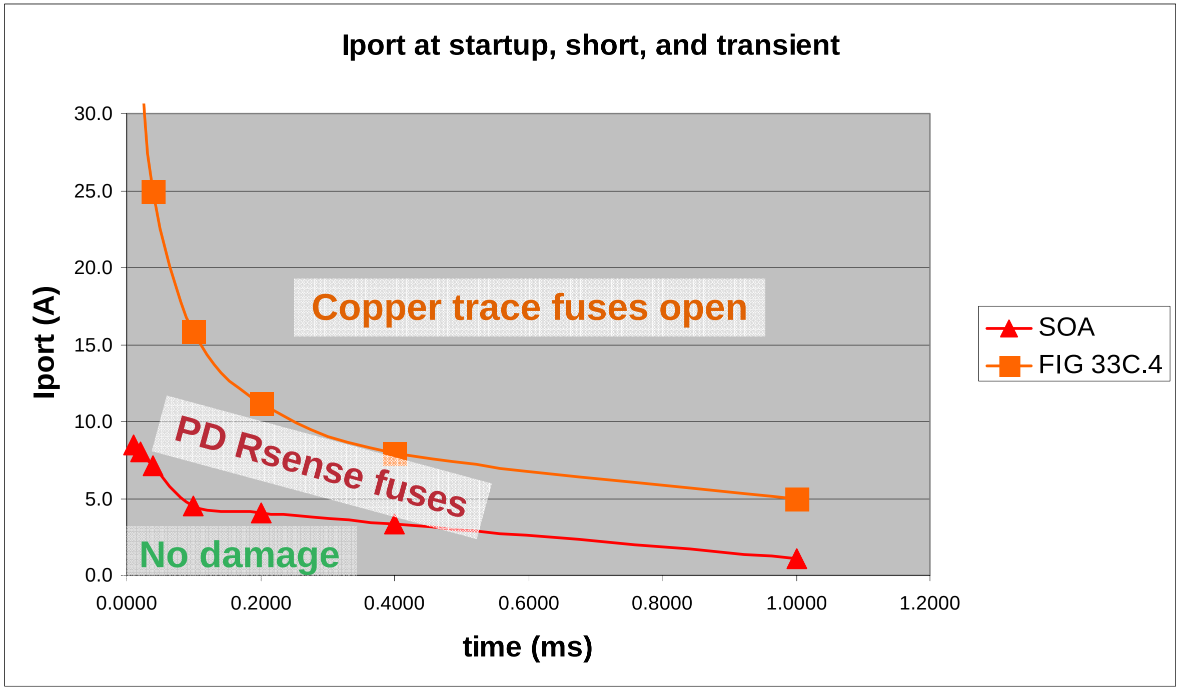




**Fig. 33C.4 undefined, 1 ms < t < 2 ms**

**48 ports, $R_{distribution}$ = 80 mΩ, Rport = 0.9 Ω, $R_{channel}$ = 0.8 Ω (short),**
**$C_{PD\_ON}$ = 5 μF (no ESR), SOA for 805 size resistor 1 Ω in parallel with 1 Ω,**
**1 A fuse (1.98 $A^2$s), Generic NCH MOSFET, $V_{DS}$ = 10 V @ $I_D$ = 14 A**

# The SOA Curve is for a PD

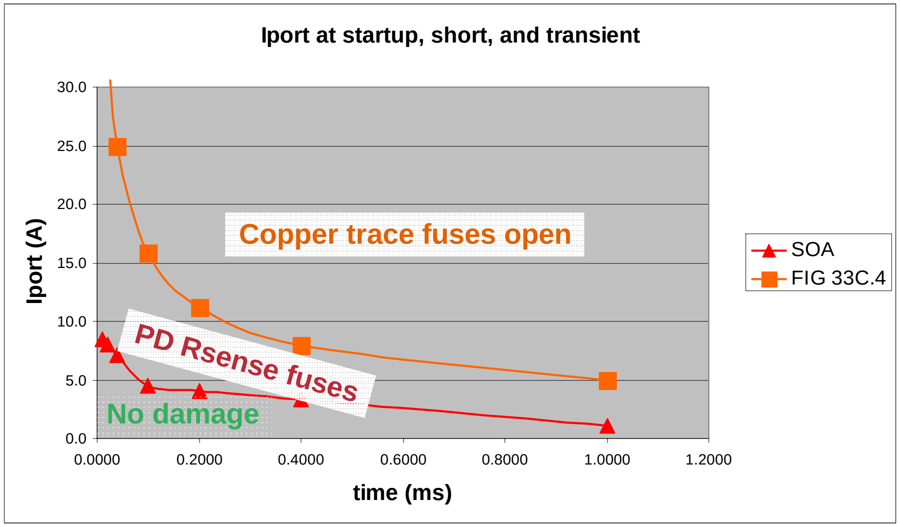
- **Assumes a straw man PD.**
  - **This PD does not exist but could be created.**
  - **Using two 1 Ω resistors in parallel to sense current.**
- **Most PD silicon vendors limit current at the PD.**
  - **Freescale**
  - **Linear**
  - **Maxim**
  - **National**
  - **Power Integration**
  - **Silicon Labs**
  - **ST**
  - **TI**
  - **Others?**



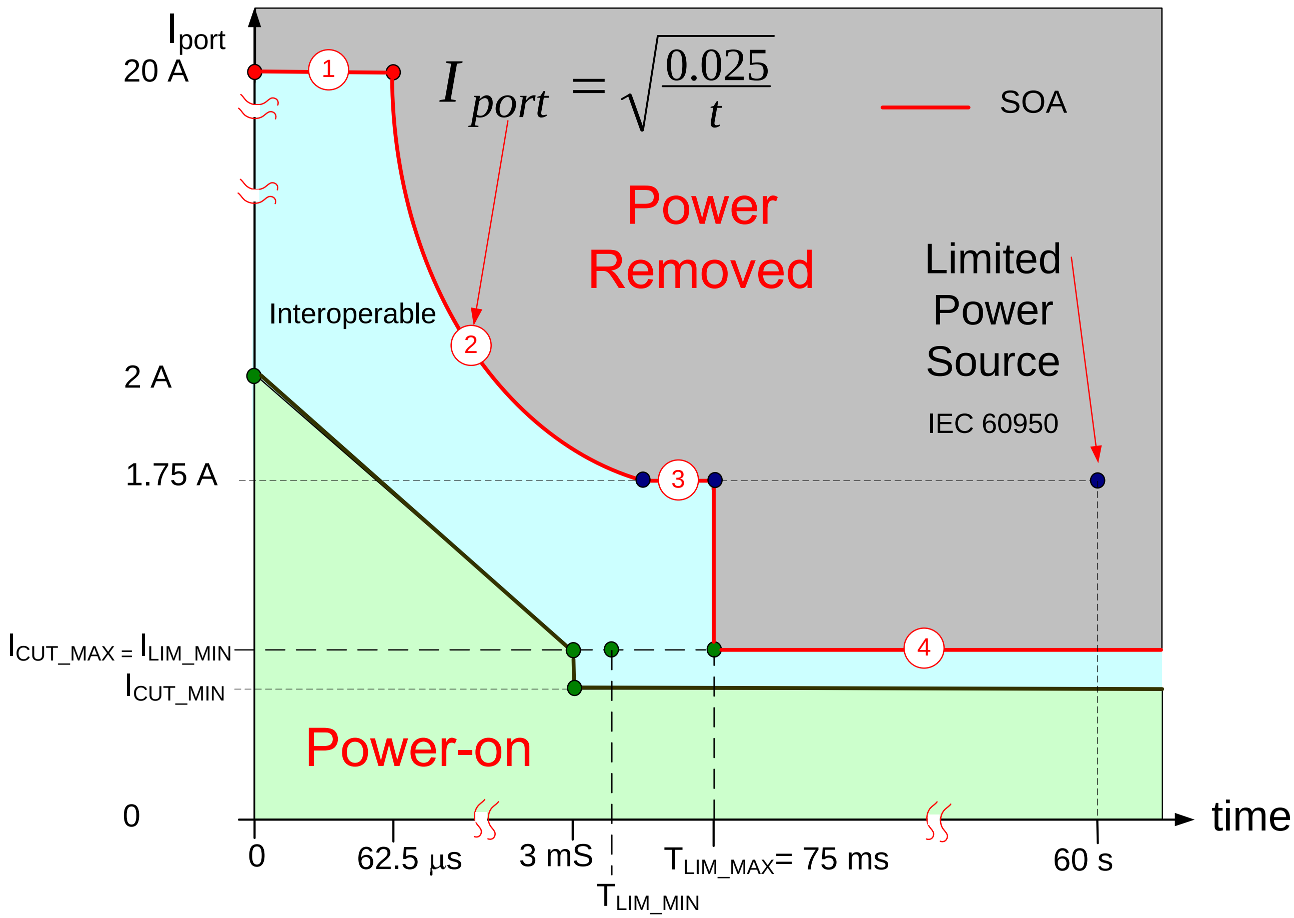
# What Current Limit Should be used?

- **Figure 33C.4?**
  **+ Shorter peak current time.**
  **+ A larger range of values supports the standard.**
  **- Could damage a PD we are not aware of.**
- **PD Rsense SOA?**
  **+ Interoperability with out damage.**
  **- Longer time to transition the PD voltage.**
  **- Tighter tolerances.**
- **33.2.8.8 Output Current**

  **Measurement after 1 ms ….**
  **See Figure 33C.4**
- **Ad hoc 100% ok with Figure 33C.4 limit.**
  **19 people**



# Power-on proposed compliance curve




**On Curve-2, 1.6 A @ t = 10.4 mS; 920 mA @ t = 29.5 ms.**

# Understanding the Current Limit Curve

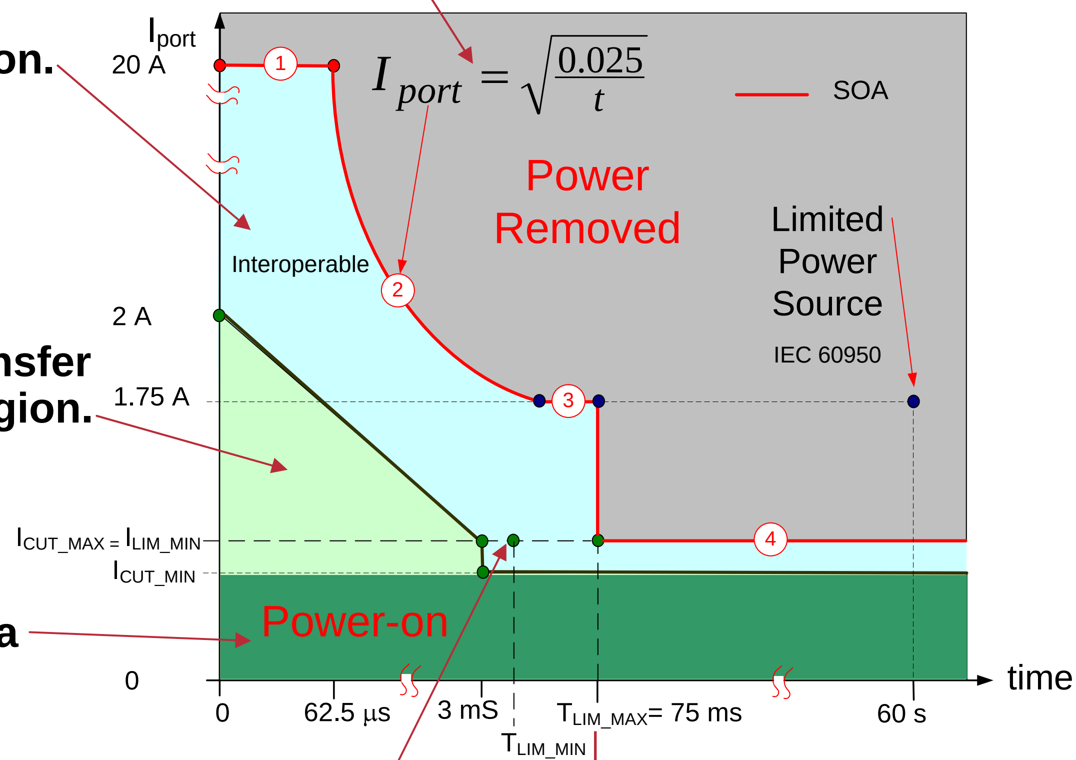
**PSEs shall turn-off power before this region is entered.**

**PSEs can turn-off power in this region.**

**PDs may operate in this region.**

**PSEs using energy based power transfer methods shall operate within this region.**

**PDs shall operate in this region with a static PSE voltage.**

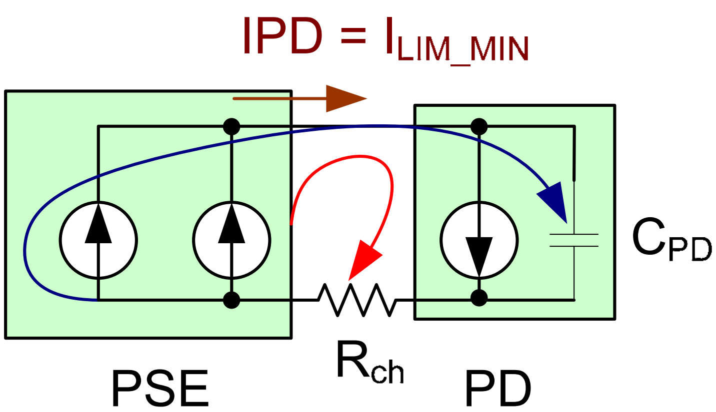



**Same as 802.3**

**PSEs may supply a constant current of $I_{LIM}$ to this point to ensure interoperability.**
**PSEs supplying a constant current of $I_{LIM}$ shall operate to at least $T_{LIM\_MIN}$.**

**The light green boundary has 45% average margin above the simulated system needs.**

# Simplified System in Current Limit

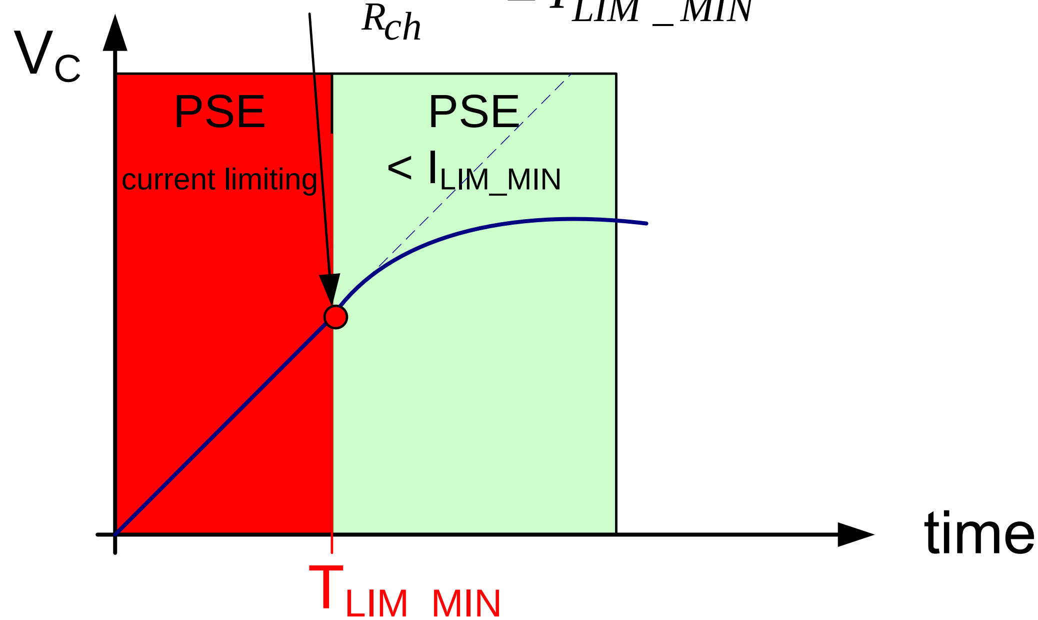



$I_{CPD} = I_{LIM\_MIN} - I_{CUT\_MIN}$

$$C_{PD}\frac{dv}{dt} < I_C$$

$$dt > C_{PD}\frac{dv}{I_C}$$

$$\frac{V_{PSE} - V_{PD}}{R_{ch}} = I_{LIM\_MIN}$$




**Short channel**

**Rch = 0, Constant $I_{PD}$**

**IEEE 802.3 $T_{LIM}$ = 47 ms**

**IEEE 802.3at, $T_{LIM}$ = 12.6 ms**

**Long channel**

**Rch = 20 or 12.5 Ω, Constant $I_{PD}$**

**IEEE 802.3 $T_{LIM}$ = 43 ms**

**IEEE 802.3at, $T_{LIM}$ = 10.4 ms**

**This simplified case assumes the PD always draws ICUT_MIN.**

# Simplified System in Current Limit

## Short channel

**Rch = 0, Constant $I_{PD}$**
**IEEE 802.3 $T_{LIM}$ = 47 ms**
**IEEE 802.3at, $T_{LIM}$ = 12.6 ms**

**IEEE 802.3**

$$T_{LIM} > C_{PD} \frac{dv}{I_C}$$

$$T_{LIM} > 180\mu F \frac{57-44}{400-350}$$

$$T_{LIM} > 47ms$$

**IEEE 802.3at**

$$T_{LIM} > 180\mu F \frac{57-50}{820-720}$$

$$T_{LIM} > 12.6ms$$

## Long channel

**Rch = 20 or 12.5 Ω, Constant $I_{PD}$**
**IEEE 802.3 $T_{LIM}$ = 43 ms**
**IEEE 802.3at, $T_{LIM}$ = 10.4 ms**

$$dv_{MIN} > R_{ch} I_{LIM}$$

$$dv_{MIN} > 20\Omega \times 400mA$$

$$dv_{MIN} > 8V$$

$$V_{PSE} = 57V, V_{PD} = 57 - 350mA \times 20\Omega V = 49$$

$$T_{LIM} > 180\mu F \frac{49-44-8}{400-350}$$

$$T_{LIM} > 43ms$$

$$dv_{MIN} > 12.5\Omega \times 820mA$$

$$dv_{MIN} > 10.3V$$

$$V_{PSE} = 50V, V_{PD} = 41V @ 720mA$$

$$V_{PSE} = 57V, V_{PD} = 48V @ 720mA$$

$$T_{LIM} > 180\mu F \frac{57-41-10.3}{820-720}$$

$$T_{LIM} > 10.4ms$$

**93% of ad hoc okay this model (13/14).**

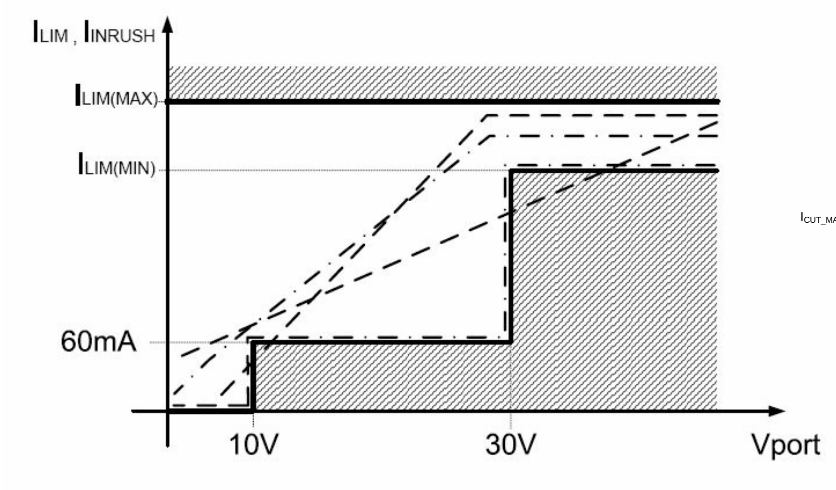
# IEEE 802.3 Concern

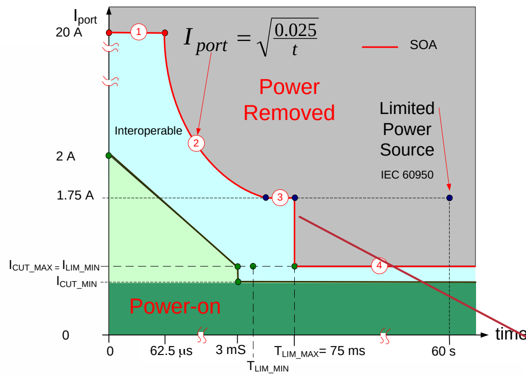
- **A PD can legally draw 400 mA for 50 ms.**
  **Table 33-12, Item 4.**
- **A system permitting this will not ensure interoperability when the PD is drawing its maximum allowable current and a PSE voltage transient occurs.**
- **Proposed Solution:**
  **Recommend that no more than $I_{CUT\_MIN}$ be drawn by a PD with a static port voltage.**

  **IEEE 802.3at will use the correct value to begin with.**

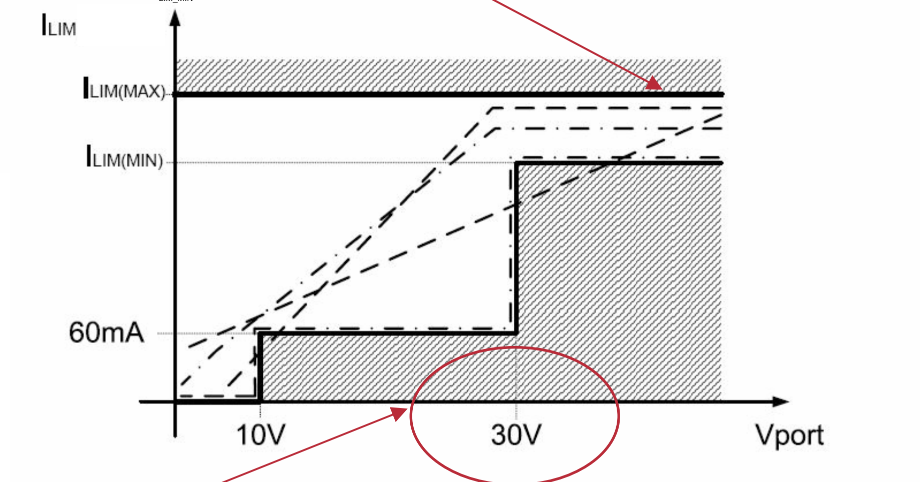
**The previous IEEE Task Force may have allowed $I_{CUT\_MAX}$ (PSE) to ensure circuits could accommodated this current value, but expected no more than $I_{CUT\_MIN}$ to be drawn normally by the PD.**

# PSE SOA




**Upper limit changes**




**In-rush & Power-on**
**IEEE 802.3**

**Power-on**
**IEEE 802.3at**

**A maximum change of 7V for a duration of > 250 µs is possible for an interoperable system.**
**Change the focus from $V_{PSE}$ to the voltage drop across the PSE pass element.**

# Next Step

- The task force should review this proposal.
- Final ad hoc clean up.
- Motion to set this baseline will be made at the July Plenary.

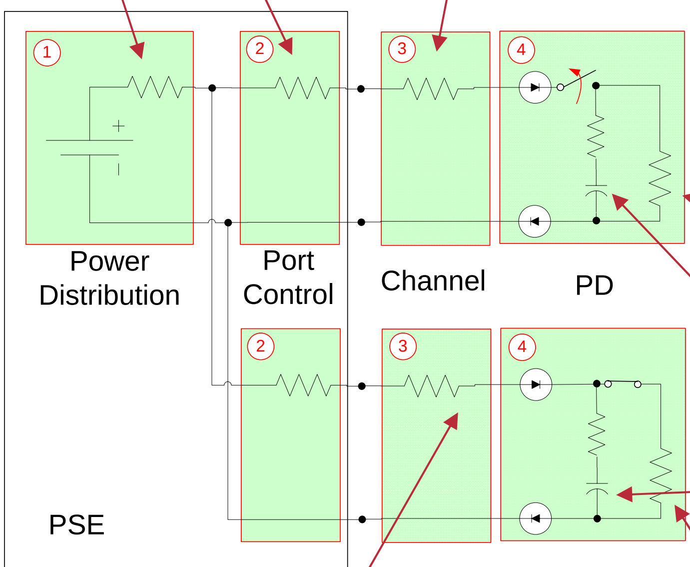
**Based on V14 Spreadsheet.**

# Use Case: PSE load drop

60 – 80 mΩ

$\frac{0.9 - 3.2\Omega}{n}$

$\frac{0.8 - 12.5\Omega}{n}$




0.8 – 12.5Ω

1. All PDs draw maximum power.
2. All but one PD reduces power demand to zero.
3. The PSE distribution voltage ramps up.
4. The remaining on PD has current injected into it.

$\frac{(49.3)^2\ \Omega}{29.5n}$

This is a don't care when the load is dropped.

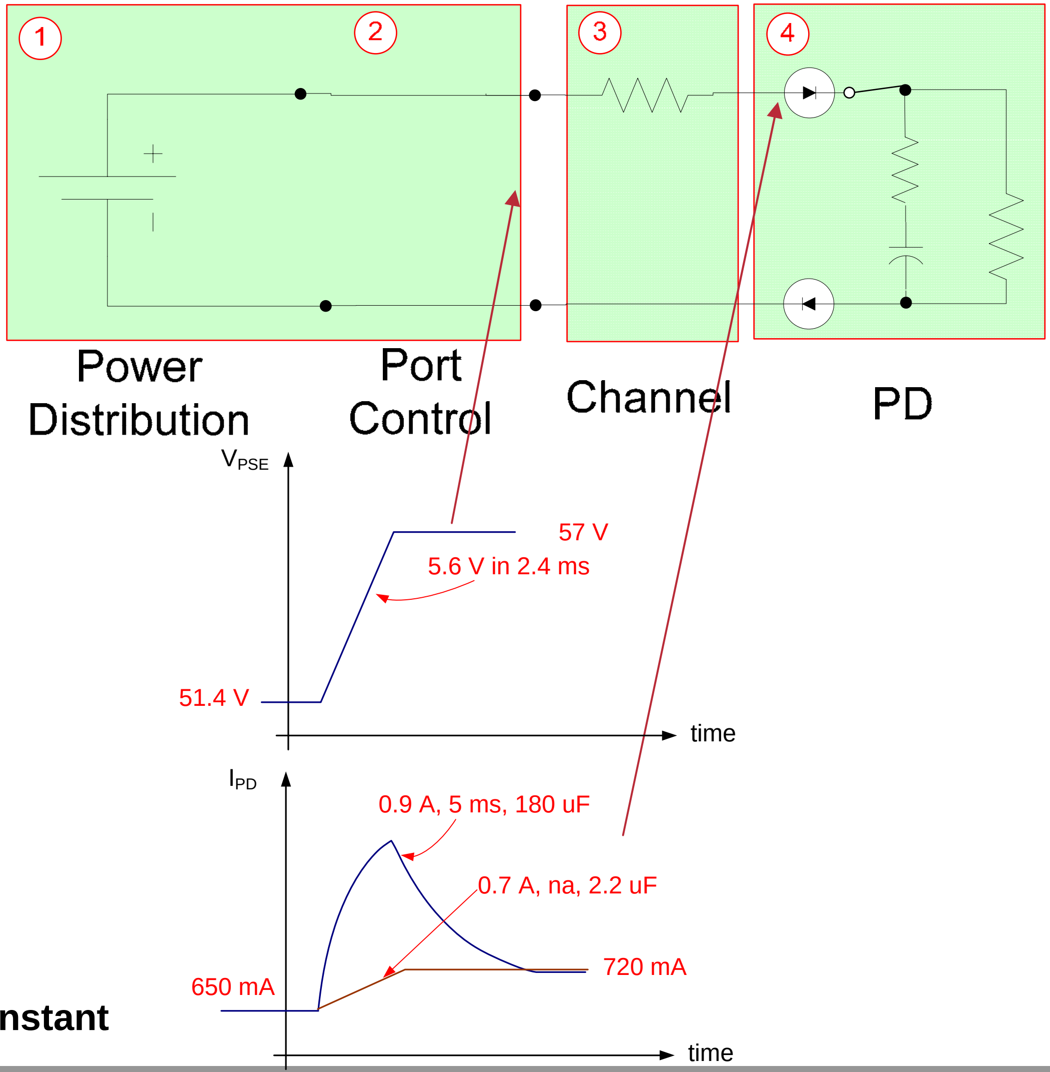
(5 – 180 μF)

$\frac{(49.3)^2\ \Omega}{29.5}$

Worst-case: 5 μF (no ESR), load dropped.

A PSE providing 50 V at 600 mA with PDs consuming 29.5 W.

# Use Case: PSE power supply backup




**Current, time constant**

**Worst-case: 180 µF.**