

Suggested Remedy for comment #183 and 184

Changes from the original Draft0.9 text are marked with RED color.

Deletions are marked with ~~Strikethrough~~.

Notes to the group or to the Editor are *Italic*

Make the following changes at the subclasses below:

1. Table 33-12 Item 1

Change Item 1 to be:

Item	Parameter	Symbol	Unit	Min	Max	Applicable PD Type	Additional Information
1	Input Voltage during overload per item 4	Vport	Vdc	36	57	1	See 33.3.5.1
1a	Input Voltage during normal load per item 5			37	57	1	
1b	Input Voltage during PD overload per item 4			39.713	57	2	
1c	Input Voltage during PSE voltage transient per Table 33-5 item 2a			36	57	2	
1d	Input Voltage during normal load per item 5			41	57	2	

2. Table 33-12 item 4: Change symbol from "Iport" to "**Iport_peak**"
3. Table 33-12 item 4: Replace TBD for Type 2 PD with "**0.823**" (*Scan all "0.82" and replace with "0.823" (=0.4/0.35) or leave "0.82" and change ration to 1.139 instead of 1.143 for Class 4 only*)
(*See below that 33.3.5.4 was updated to reflect the dependence of Ipeak with Pclass and Vport.*)

4. Make the following changes in 33.3.5.4 Peak operating current.

"At any operating condition the peak current shall not exceed $\frac{P_{port_max}}{V_{port}}$ I_{port_peak} as defined by Table 33-12 item 4 for more than 50ms max and 5% duty cycle max.

I_{port_peak} is defined by $I_{port_peak} = K_{i_class} \cdot I_{port} = \frac{I_{port_peak_max}}{I_{port_avg_max}} \cdot I_{port}$

I_{port} is the average value of the port current during normal operation.

$K_{i_class} = \frac{I_{port_peak_max}}{I_{port_avg_max}}$ which is a constant for each classification power range.

$I_{port_peak_max}$ is defined by Table 33-12 item 4.

$I_{port_avg_max}$ is approximated by $I_{port_avg_max} = \frac{V_{pse_min} - (V_{pse_min}^2 - 4 \cdot Ppd_{class_max} \cdot Rc)}{2 \cdot Rc}$

V_{pse_min} is the PSE port voltage, V_{port} , as defined by Table 33-5 item 1

Ppd_{class_max} is the upper value of the classification range as defined by Table 33-10.

Rc is the maximum channel loop resistance as defined in 33.3.5.2.

I_{port_peak} for any Pd power and PSE output voltage is approximated by $I_{port_peak} = K_{i_class} \cdot \left[\frac{V_{pse} - (V_{pse}^2 - 4 \cdot Ppd_{class} \cdot Rc)}{2 \cdot Rc} \right]$

Ppd_{class} is any PD power level indicated by layer 1 or layer 2 classification method.

Table 33-12 item 4 defines $I_{port_peak_max}$ for maximum class power at minimum PSE port voltage.

I_{port_avg} for any PSE port voltage specified in table 33-5 and any PD power level indicated by layer 1 or layer 2 classification method is

approximated by $I_{port_avg} = \frac{V_{pse} - (V_{pse}^2 - 4 \cdot Ppd_{class} \cdot Rc)}{2 \cdot Rc}$

The PD input voltage during normal operation as defined by Table 33-12 items 1a and 1d is approximated by

$V_{port} = \frac{V_{pse} + (V_{pse}^2 - 4 \cdot Ppd_{class} \cdot Rc)}{2}$ Or by $V_{port} = \frac{Ppd_{class}}{I_{port_avg}}$

Informative Notes:

1. The values of I_{peak} are determined by the specification according to design constrains such cable maximum current, design accuracy, PD dynamic load changes, PSE power supply costs and others. Once I_{peak} is selected, Ki_{class} can be set and as a result, I_{port_peak} and I_{port_avg} for any PSE port voltage and PD power.

2. PD peak input power is defined by $Ppd_peak = (Vpse - Iport_peak \cdot Rc) \cdot Iport_peak$

Modified Table 33-10

Class	Usage	Range of maximum average power used by the PD,	Ki_{CLASS}
0	Default, Type 1	0.44W to 12.95W	1.143
1	Type 1	0.44W to 3.84W	1.318
2	Type 1	3.84W to 6.49W	1.321
3	Type 1	6.49W to 12.95W	1.143
4	Type 2	12.95W to 29.5W	1.143

(Note for the group: Ki may be the same number for all classes i.e. $1.143=0.4/0.35$ but in this case which is simplifying the specification a bit we need to allow higher average current than permitted by I_{port_avg} equation for class 1 and 2 for compensating the low efficiency of this cases. See presentation that explains it.

In this option the specification became simpler:

- 1. Ki is constant for any power level.*
- 2. The additional column in Table 33-10 can be removed.*
- 3. We need to allow $\sim 1.321/1.143$ more DC current at classes 1, 2 which is OK and not violating legacy devices. In addition this is actually what happens. In lower power the dc current is abit higher then predicted by the equation of I_{port_avg} due too low efficiency of the PD DC/DC.)*

4.1 Make the additional changes to 33.3.5.4 as follows:

Lines 8-13: Replace with:

The maximum IPort_dc and IPort_rms values for all operating VPort range shall be defined for Type 1 and Type 2 PDs by the Iport_avg equation above. (Editor: To assign reference numbers for the equations e.g. Eq-1 , Eq-2 ETC.)
the following equation: $I_{Port_max} [mA] = 12950/V_{Port}$.

4.2 Delete lines 11 to 26.

5. Table 33-5 Item 8, Icut_max: Replace TBD with 0.82.
(See below that 33.2.8.6 was updated to reflect the dependence of Ipeak with Pclass and Vport.)

6. Change 33.2.8.4 to be:

33.2.8.4 Type 1 PSE max output current in normal powering mode at min output voltage

For VPort > 44 V, the minimum value for IPort_max in Table 33–5 shall be 15.4 W/VPort.

The current IPort_max ensures 15.4 W minimum output power for Class 0 and 3. For Iport_max at Class 1 and 2 see equations in 33.3.5.4.

The PSE shall support the following AC current waveform parameters:

- a) For Vport=44V: Ipeak = 0.4A minimum for 50ms minimum and 5% duty cycle minimum.
- b) For VPort > 44V: ~~Ipeak=17.6W/Vport~~ Ipeak_max is defined by 33.3.5.4.

7. Change 33.2.8.4a to be:

Insert section 33.2.8.4a:

33.2.8.4a Type 2 PSE max output current in normal powering mode at min output voltage

For $V_{Port} > 50$ V, the minimum value for I_{Port_max} in Table 33–5 shall be 36 W/ V_{Port} .

The current I_{Port_max} ensures 36 W min output power for Class 4. For I_{port_max} at lower power as a result of L2 PSE-PD negotiation or other additional information, see equations in 33.3.5.4.

The PSE shall support the following AC current waveform parameters:

a) For $V_{port}=50$ V: $I_{peak} = 0.82$ A minimum for 50ms minimum and 5% duty cycle minimum.

b) For $V_{Port} > 50$ V: ~~$I_{peak}=TBD$ W/ V_{port}~~ I_{peak_max} is defined by 33.3.5.4.

8. Change 33.2.8.6 to be:

33.2.8.6 Overload current detection range

If I_{Port} in Table 33–5 exceeds I_{CUT} for longer than T_{ovld} , the PSE shall remove power from the PI. See Figure 33C.6.

In a PSE that supports a classification function (33.2.7 and/or 33.6.4), the minimum value of I_{CUT} may optionally be as described by I_{peak_max} equation in 33.3.5.4.

~~$(P_{class}*1000/V_{portmin},$~~

where

~~P_{class} is the minimum power level at the output of the PSE (as specified by Table 33–3)~~

~~$V_{portmin}$ is V_{Port_min} in Table 33–5~~