

IEEE P802.3at Task Force Power Via MDI Enhancements Midspan Adhoc

Midspan/Channel Requirements below 1MHz
New Material +Updates
May 7, 2008
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Add names



New material- Ad Hoc meeting May 8,2008

- BER tests results w/o BLW tracking function
- Finalizing Operating Bandwidth
- Final results of SCM with and w/o Midspan
- Worst case analysis results
- Evaluating the design margins in the system
- Midspan TF including test setup for compliance.
- Q&A



BER test sensitivity analysis

■ Setup:

- A standard 100BT system tested at 100BT w/o Midspan by using 100BT standard equipment generator.
- Generator Transmitter inductance reduced to 350uH by adding external parallel inductance for total equivalent inductance of 350uH. Test equipment is not using BLW tracking.

■ Results:

- BER tests results showed ZERO lost packets with and w/o Midspan ALT A when BLW data were inserted.
- Two Midspan devices were tested

■ Conclusions:

- The above results together with the other two UNH tests confirms that the addition of 3rd Inductance (that meets the requirements) in parallel is not affecting the data integrity under BLW conditions.
- *See transfer function derivation for understanding why it is not affecting the results from mathematical/physical point of view .*



Finalizing Operating Bandwidth

- The reason for our work was the fact that 350uH was defined only for 100BT.
- BLW effects are relevant only for 100BT
- The 350uH was defined at lower frequency (100KHz) then the data bandwidth minimum frequency (1MHz) which imply that the relevancy of the operating worst case bandwidth under BLW conditions is not lower then 100KHz.
- Hence there is no need to address lower frequencies then 100KHz in the System Channel Model with or without Midspan according to the current specifications (ANSI X3.263-1995 (TP-PMD) subclause 9.1.7).
- As a result
 - Operating frequency range of TF: $100\text{KHz} \leq f < 1\text{MHz}$.
 - Confirmed by PHY experts (Dan Dove and others)



Analysis Model Parameters

	Parameter	Units	Min	Max	Comments
	Transformer				
1	Inductance	uH	350		At Ibias maximum
2	Rwp	Ω	0.27	0.5	
3	Rws	Ω	0.47	0.55	
4	Connectors Rdc	Ω		0.2	
5	Total Channel Resistance	Ω		25	For 100m
6	100BT transmitter signal	Vpp	2		Data from Dan Dove
7	100BT receiver minimum signal to detect at worst case	Vpp	0.045		Data from Dan Dove
8	Source and Load Terminations	Ω	95	105	Data from Steve Sedio, Dan Dove and Randy Rannow
9	Test Equipment Gain Measurements errors	dB		0.1	Test equipment vendors to comment
10	Switch Design Margin	dB		>20	See detailed calculations in separate slide
11	Midspan Design Margin	dB		<1	See detailed calculations in separate slide



Termination min/max value considerations

- Inputs from Steve Sedio, Dan Dove and Randy Rannow
- Source and load accuracy: $\pm 5\%$.
- The spec is driven by the Return Loss criteria. With an 85-110 ohm line impedance, we have to meet return loss.
- This limits the capacitance and resistance of the port. Typically some use 100ohms with $\pm 1\%$, but many IC vendors are implementing internal terminations which may not be as tightly specified.
- **Conclusions:**
- **Model: Using $\pm 5\%$ is practical than using $\pm 1\%$.**
- **Test setup: Use $\pm 1\%$ resistors.**



Worst Case Analysis conditions

- Worst Case Gain Attenuation operating conditions in the System Channel Model w/o Midspan.
 - $R_L \rightarrow \text{Min}$ (RL=Termination at the Receiver side)
 - $R_S \rightarrow \text{Max}$ (RS=Termination at the Transmitter side)
 - $R_{wp}, R_{ws} \rightarrow \text{Max}$ (Primary and Secondary Transformer windings)
 - Connector $\rightarrow \text{Max}$ (Connector contact resistance)
 - $LM \rightarrow \text{Min}$ (=350uH, Happen at I_{bias} max.)
 - $R_c \rightarrow \text{Max} \rightarrow$ (length=100m, Cable resistance)
 - Number of connectors $\rightarrow \text{Max}=6$, i.e. Channel= 4, Equipment= 2



Acceptable System Channel w.c Gain=Insertion Loss=Attenuation at 100MHz for 100m.

	Parameter	Units	Value	Source	Comments
1	Transmitter Minimum output	Vpp/dB	2 / 6	Dan Dove and others	
2	Channel Insertion Loss	dB	24	ANSI/TIA/EIA-568-B.1-2001	
3	Source Load termination attenuation	dB	6.02	$100/(100+100)=0.5=6.02\text{dB}$	
4	Data Transformer worst case insertion loss	dB	2	In reality the number is lower	Two Data transformers
5	Minimum signal at Receiver input	dB/Vpp	$6-24-6.02-2=-25.97\text{dB}$ $=0.05\text{Vpp}$	Calculated based on the data in this table	Dan Dove: 0.045Vpp.
6	PHY to PHY minimum requirement to support 100BT at worst case conditions at 100MHz.	(V/V)/dB	$0.05/2=0.025$ -32	Calculated based on the data in this table	



Acceptable System Channel w.c Gain=Insertion Loss=Attenuation at 1MHz for 100m.

	Parameter	Units	Value	Source	Comments
1	Transmitter Minimum output	Vpp/dB	2 / 6	Dan Dove	
2	Channel Insertion Loss	dB	2.2	-ANSI/TIA/EIA-568-B.1-2001	
			4	ISO/IEC 11801:2002	
3	Source Load termination attenuation	dB	6.02	$100/(100+100)=0.5=6.02\text{dB}$	
4	Data Transformer worst case insertion loss	dB	~1		Two Data transformers
5	Minimum signal at Receiver input	Db/Vpp	$6-4-6.02-1=-4.97\text{dB}$ $=0.563\text{Vpp}$	Calculated based on the data in this table	
6	PHY to PHY minimum requirement to support 100BT at worst case conditions at 1MHz.	(V/V)/dB	$0.563/2=0.281$ -11	Calculated based on the data in this table	

Our interest is frequencies below 1MHz.

Hence we have **21dB design margin** (0.05Vpp @100MHz/0.563Vpp @ 1MHz)

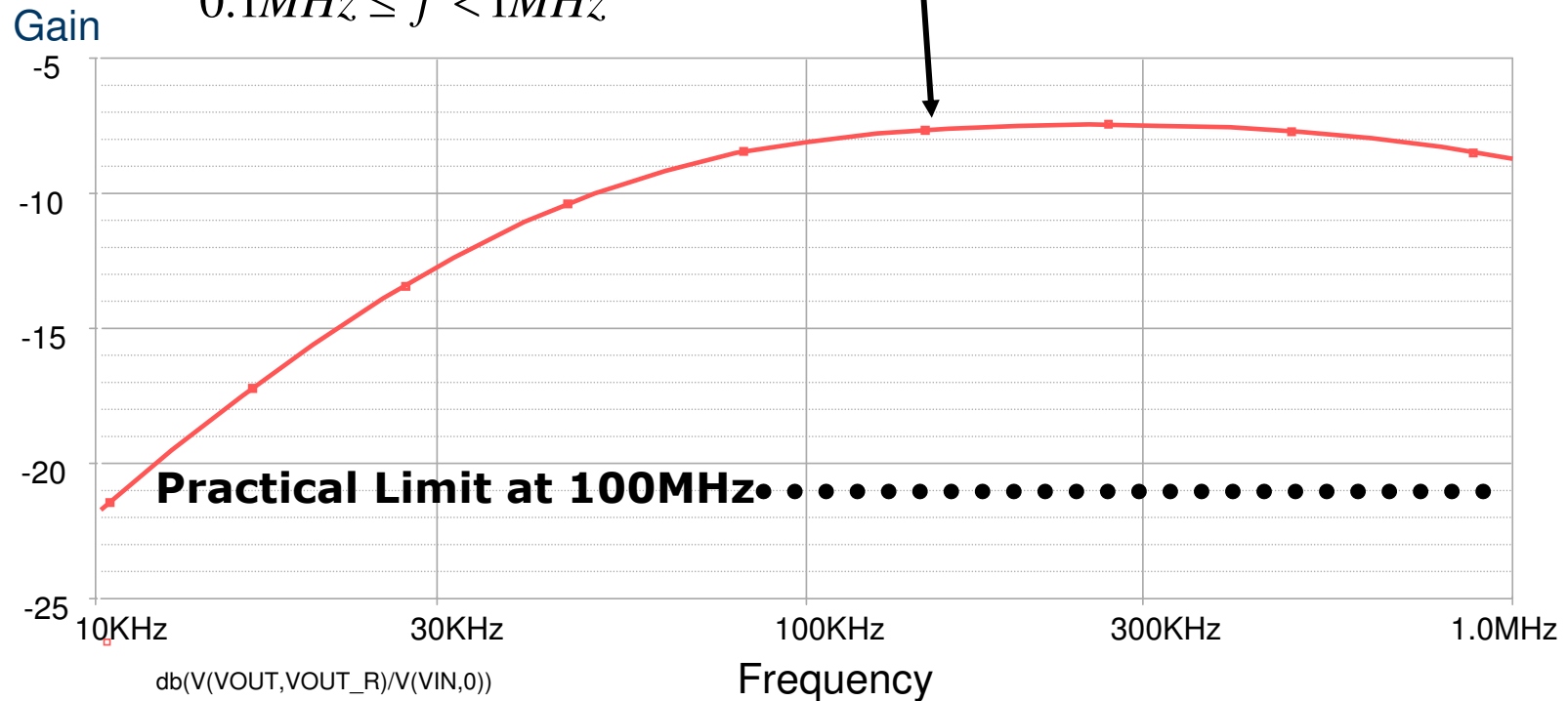


SCM: without Midspan at 350uH, 100m. W.C analysis

- A compliant System Channel Model Gain w/o Midspan, must be higher than this curve per current standards and standard components specifications

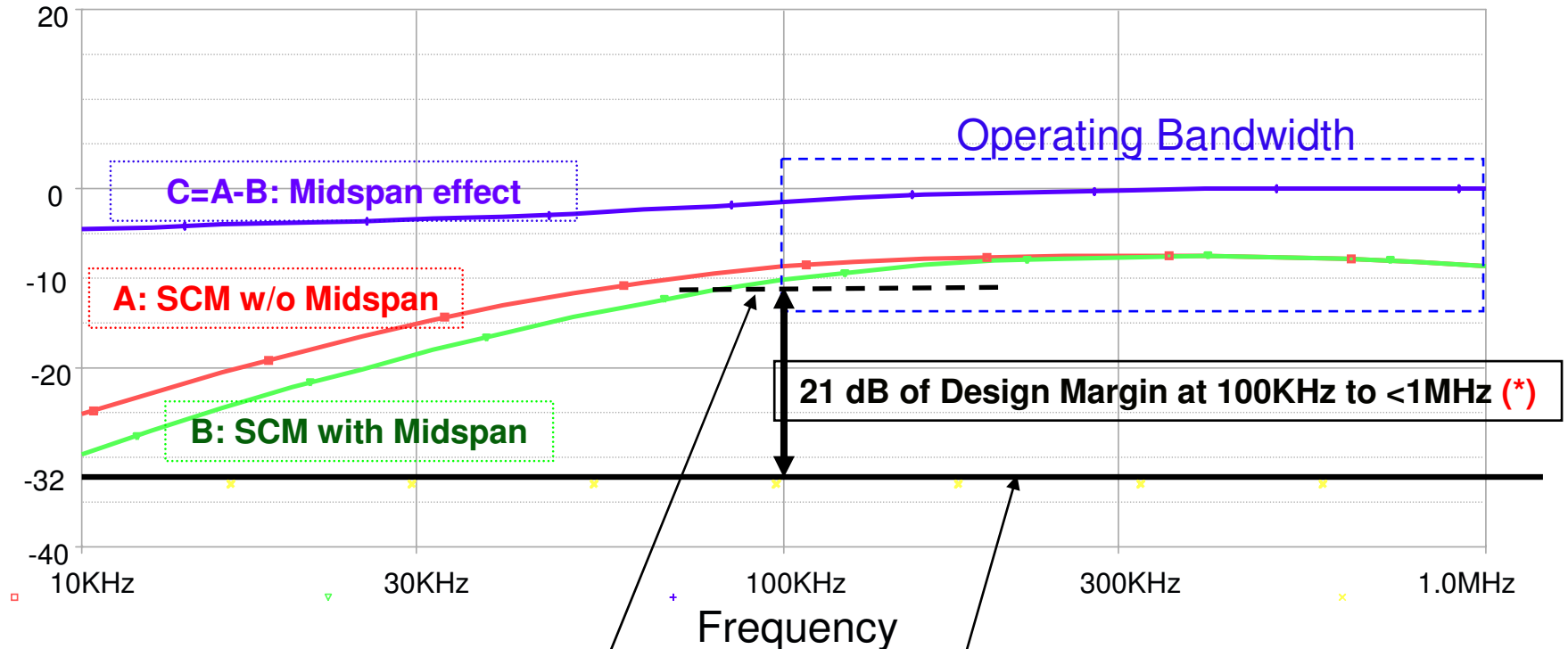
$$\text{Gain} = -9.075 + 14.419 \cdot f - 41.781 \cdot f^2 + 45.759 \cdot f^3 - 18.075 \cdot f^4$$

$$0.1\text{MHz} \leq f < 1\text{MHz}$$



SCM: with and without Midspan at 350uH, 100m. W.C analysis

Gain[dB]



E: D at 1MHz. Gain/ Attenuation/ Insertion Loss = -11dB

D: SCM PHY to PHY minimum Gain/ Attenuation/ Insertion Loss requirements at 100MHz= -32dB

(*) Actually margin is higher BY ADDITIONAL 3dB due to the fact that Channel IL is ~1dB at f<1MHz and not 4dB



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Midspan / Channel Requirements below 1MHz, New material +Updates. Yair Darshan, May , 2008

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How to distribute the design margins that we have in the system at frequencies below 1MHz?

- At 100KHz, the system gain is:
 - ~-8dB w/o Midspan (-8.7dB at 1MHz, -7.5dB at 300KHz)
 - ~ -9dB with Midspan (-8.7dB at 1MHz, -7.5dB at 300KHz)
 - Which is practically negligible difference.
- The SCM is required by various system components specifications to work with gain as low as
 - -32dB at 100MHz
 - -11dB at 1MHz
 - Hence the PHY is capable to work with Gain as low as -32dB
 - But the inductance issue is relevant at the low frequency range which is 21dB higher than the worst case conditions.
- Since the Midspan has negligible effect on the SCM it is recommended to assign most of the Margin to the Switch according to the following ratio:
 - Midspan: 1dB max. as function of frequency from 100KHz to 1MHz
 - Switch: 20dB max. as function of frequency from 100KHz to 1MHz



Generating Midspan TF

- Steps:
- 1. Generating System Model w/o Midspan, **SCM**. Done.
- 2. Generating System Model with Midspan ALT A, **SCMM**. Done.
- 3. Finding w.c analysis results and update the model. Done.
- 4. Finding Midspan TF=SCM -SCMM (Gain[db] vs Frequency plot)
- 5. Finding the best regression function structure to build the TF.
(3, 4 and 5 order polynomial regression vs. Logarithmic regression were evaluated.)
- 6. Logarithmic structure showed best accuracy for the operating bandwidth under discussion (100KHz to 1MHz) for Midspan.
- 7. Adding margin function to cover Test Equipment errors and design.
- 8. Getting Final Equation.



Midspan TF and test setup for compliance.

Including w.c analysis

$$\left\{ -c + 37.46 \cdot \text{LOG}_{10} \left(\frac{a \cdot f}{\sqrt{1 + b \cdot f^2}} \right) \right\}$$

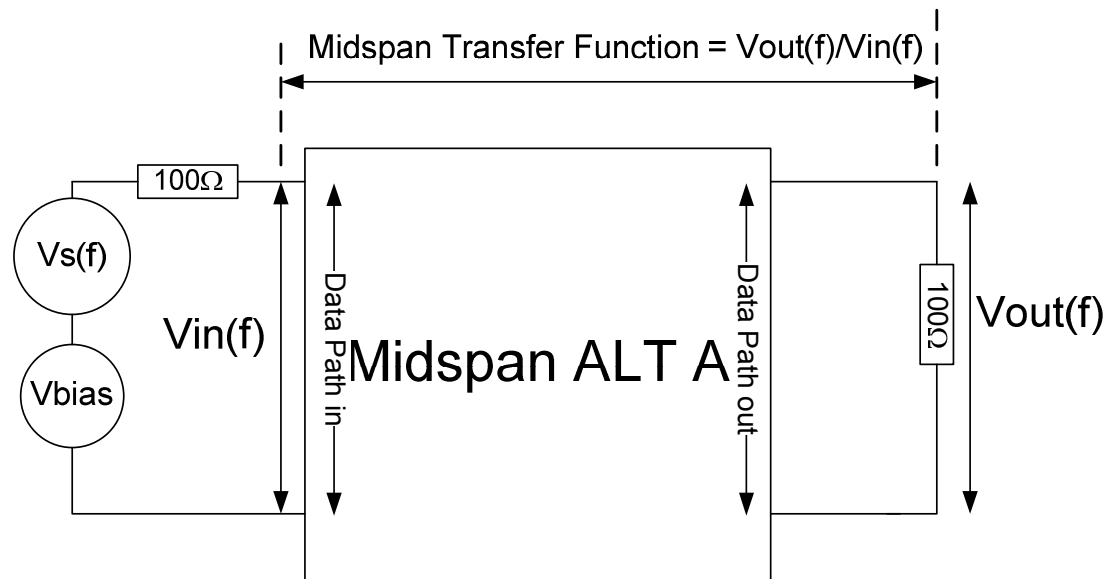
Updated Equation 33-14

$$a = 22.41$$

$$b = 520.48$$

$$c = 0.1$$

$$0.1\text{MHz} \leq f < 1\text{MHz}$$



- $V_{in}(f)$ is the Sine wave signal to be used to measure the Midspan TF.
- V_{bias} is the DC offset voltage to be superimposed on the Sine wave in order to generate I_{bias} . $I_{bias} = \text{TBD} (8\text{mA}?) + I_{unb}/2$. I_{unb} is specified in Table 33-9.
- $V_{out}(f)$ is the Midspan response to $V_{in}(f)$



Q&A

■ Discussion

