IEEE P802.3at Power via MDI Enhancements 350uH Ad Hoc report

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Ad hocs held with an average attendance of about 10. Aggregate attendance from all meetings listed.

Agenda

- Recap of issue
- Proposal 1 – RX based
    - Midspan issues
- Proposal 2 – TX based
- Summary
    - Consensus items
    - Options

Issue

- Clause 25 incorporates TP-PMD by reference

  25.2 Functional specifications

  The 100BASE-TX PMD (and MDI) is specified by incorporating the FDDI TP-PMD standard, ANSI X3.263: 1995 (TP-PMD), by reference, with the modifications noted below.

- Subclause 9.1.7 of ANSI X3.263: 1995
  - Specifies a worst case droop of transformer
    - Minimum 350 uH with any DC bias between 0 mA and +8 mA

- Normative for 100BASE-T PHYs
  - Not listed in 25.2 modifications to X3.263

- PoE+ increases DC current imbalance in transformer
  - This in combination with the 350 uH minimum is an issue
    - See DC Current Imbalance - Steve Ellsworth
      http://www.ieee802.org/3/poep_study/public/mar05/ellsworth_1_0305.pdf#Page=7

ANSI X3.263-1995 (TP-PMD)

9.1.7 Worst case droop of transformer

Baseline Wander tracking by the receiver is dependent on the worst case droop that can be produced by a transmitter. Droop is directly related to the Open Circuit Inductance (OCL) which varies with temperature, manufacturing tolerance, and bias current.

Worst case Baseline Wander Frames vary the transformer bias which causes the droop to change with data content. This variation must be accounted for by the receiver to track the Baseline Wander over long frames. Variation in inductance caused by bias of the transformer can be on the order of 2:1.

The minimum inductance measured at the transmit pins of the AOI shall be greater than or equal to 350 uH with any DC bias current between 0 mA and +8 mA injected as shown in figure 13.
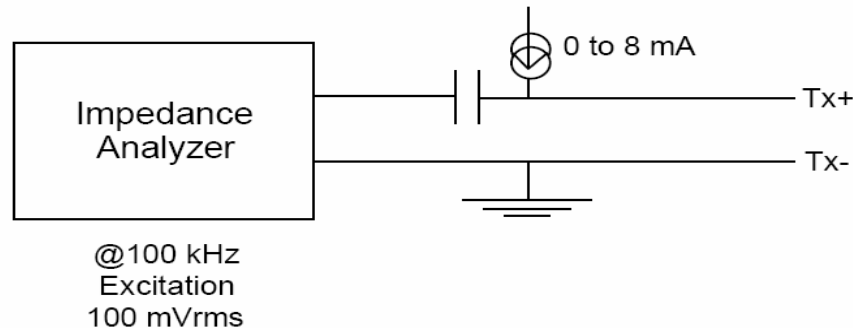
Figure 13

Problem

- Baseline wander can cause bit errors
  - Inductance requirement is one fix
    - But this is an implementation approach
  - Other approaches may now be available
    - But due to standard inductance still has to be met
- BER performance is actual requirement
  - And meeting BER is all that should matter
    - Implementation to achieve this not of interest
   - Should not be mandated by standard

But if only it was that easy …

- High inductance is specified for Transmit side
  - This is what we want to remove need for
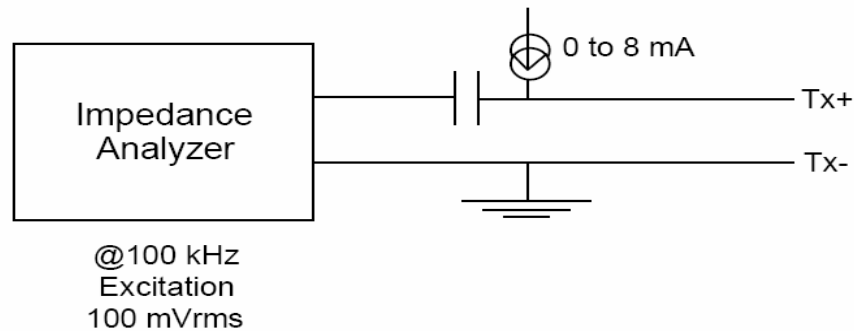
- BER is usually specified for Receiver
  - Using complaint transmitter, and worse case channel
- Compensation for BLW implemented in receiver
  - Such an implementation will likely expect 350uH OCL at TX
    - Since this is what is specified
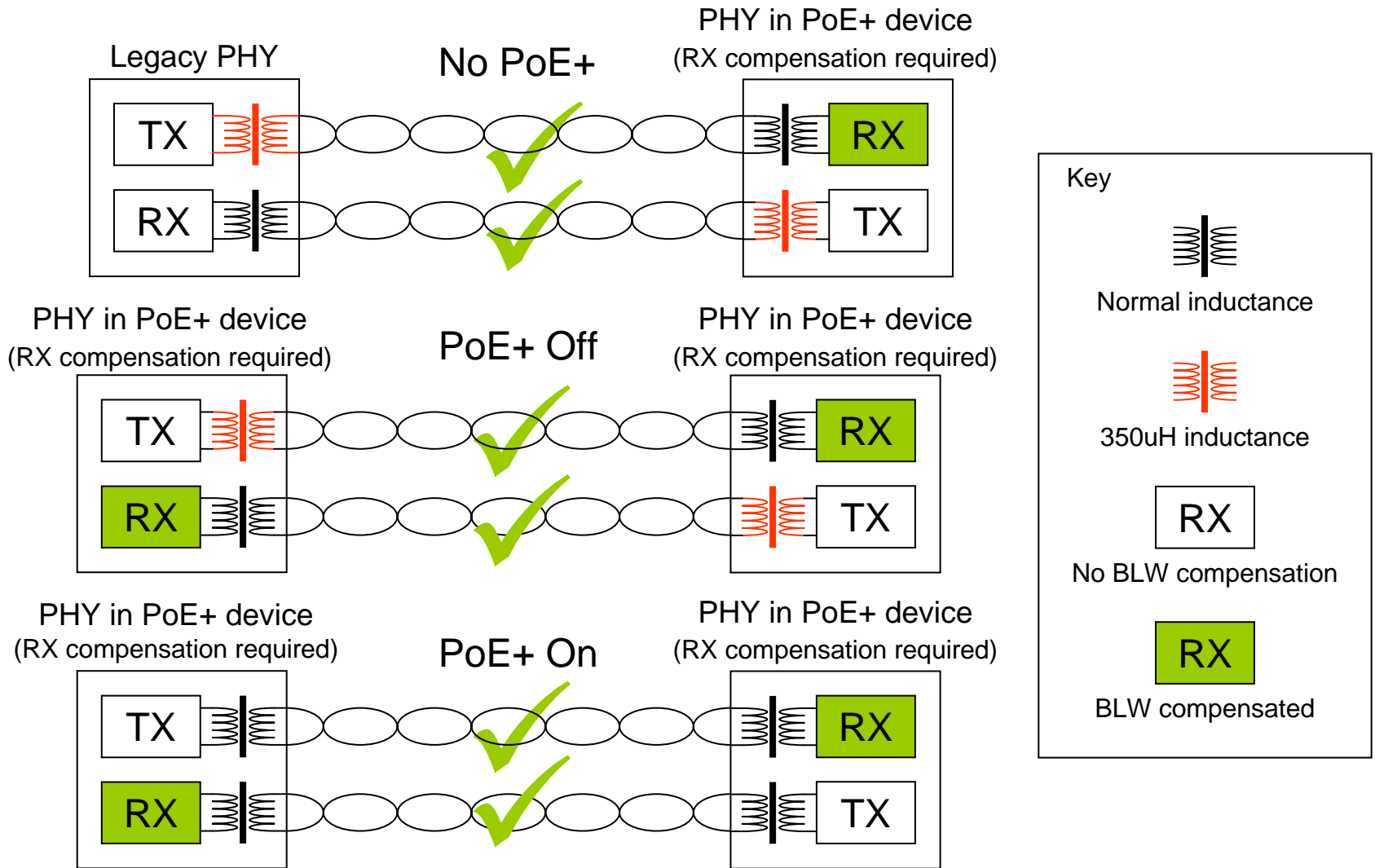
Problem is mixed configuration
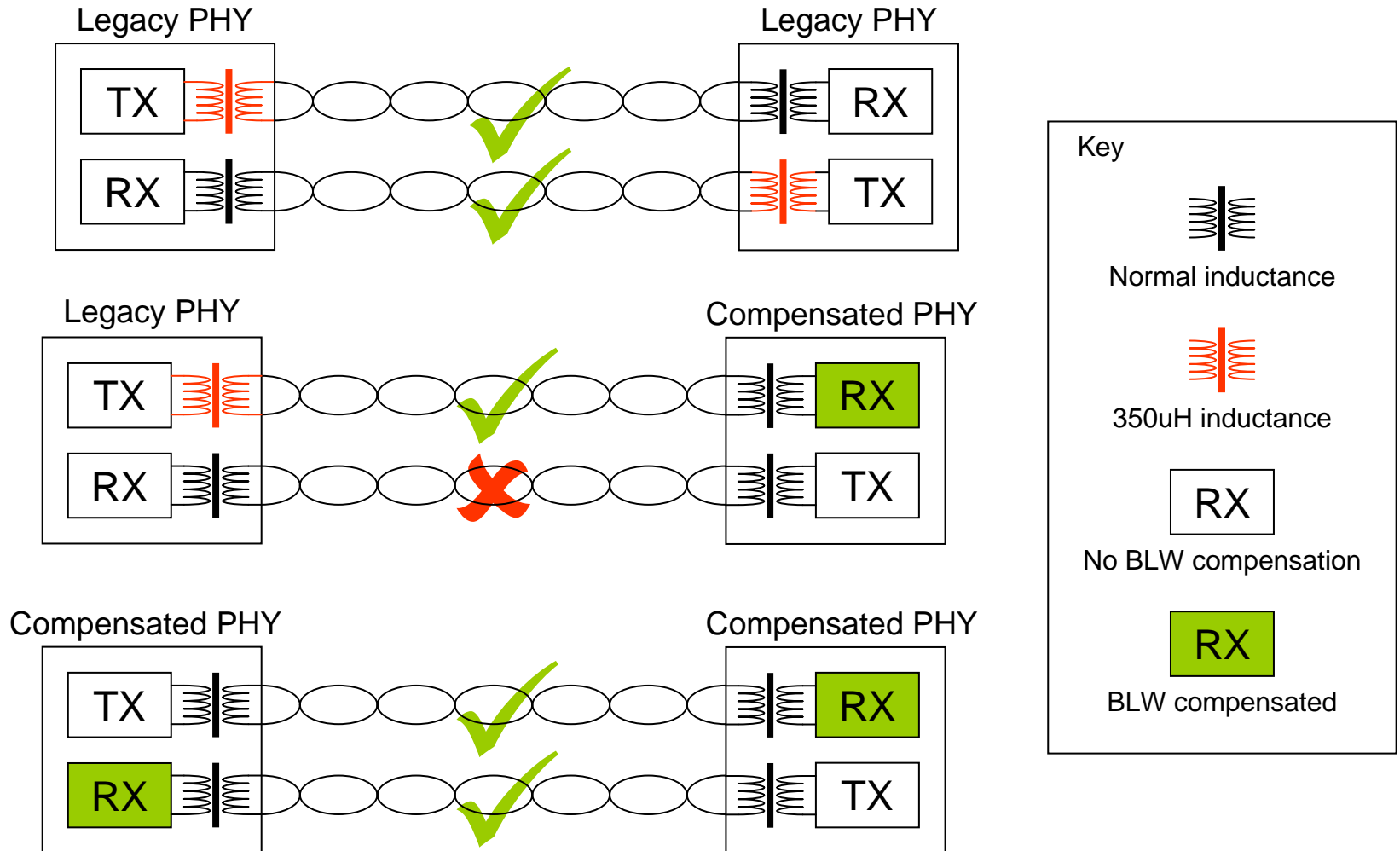
Proposal 1 – RX based

- Specify that PHY RX has meet BER with worse case channel under worse case BLW conditions
  - But can't just remove specification for 350uH OCL and replace with new RX BER specification
    - Legacy PHY to compensated PHY problem
- Could we limit this solution to PoE+ ?
  - Use PoE+ operation as detection mechanism
  - Specify the PHY used in PoE+ has to:
    - Meet new RX BER specification
    - Meet 350uH OCL specification when not supplying power
  - Specify the PHY used in POE+ doesn't need to:
    - Meet 350uH OCL specification when supplying power
      - This is when imbalance current reduces OCL

RX based - Mixed configuration

Legacy PHY

No PoE+

PHY in PoE+ device
(RX compensation required)

TX

RX

PHY in PoE+ device
(RX compensation required)

PoE+ Off

PHY in PoE+ device
(RX compensation required)

TX

RX

RX

TX

PHY in PoE+ device
(RX compensation required)

PoE+ On

PHY in PoE+ device
(RX compensation required)

TX

RX

RX

TX

Key

Normal inductance

350uH inductance

RX
No BLW compensation

RX
BLW compensated

Alternative A midspan problem

PoE+ On

Legacy device

Alternative A
PoE+ Midspan PSE

PoE+ PD

TX RX

RX TX

✓

✗

TX path from PoE+ PD to Midspan lacks both
350uH and RX compensation

Proposal that as PoE+
is on, TX doesn't
need to meet 350uH
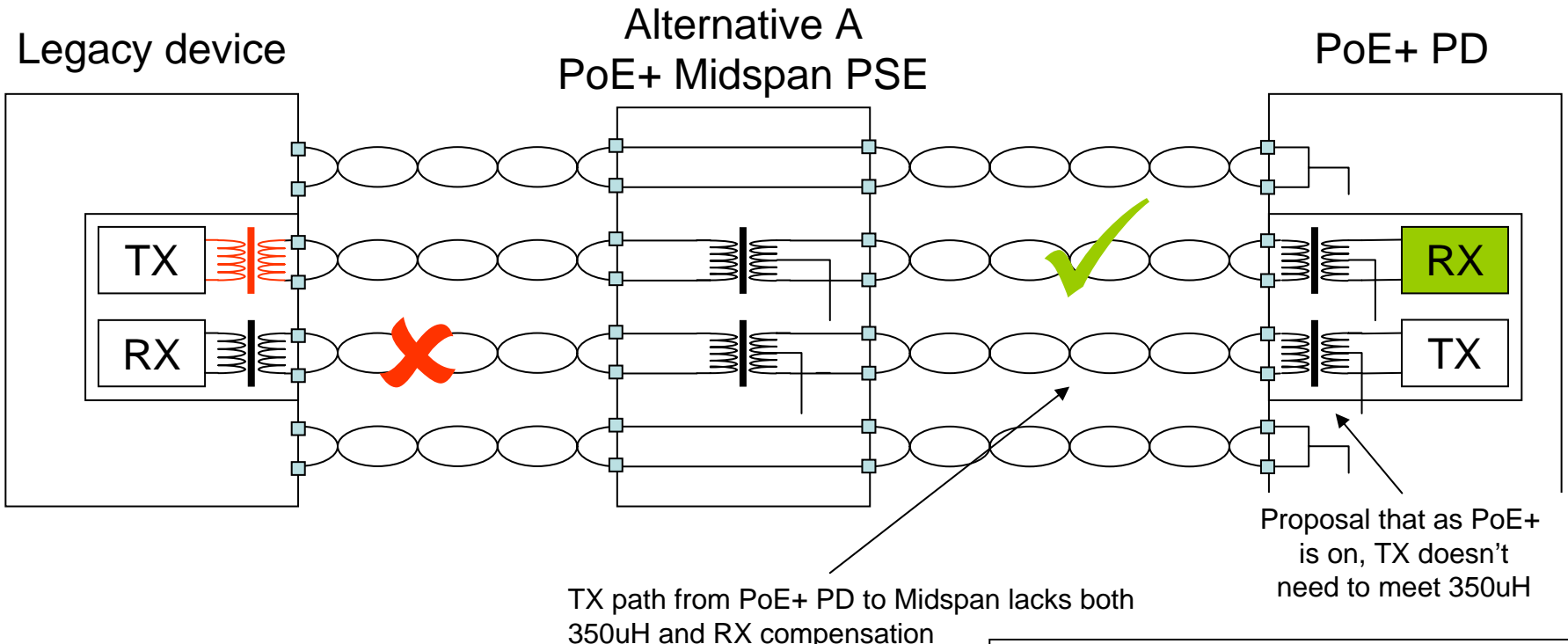
Approach: Require MidSpan to provide ballast resistors
so imbalance current does not exceed 8mA.

Key

Normal inductance   350uH inductance
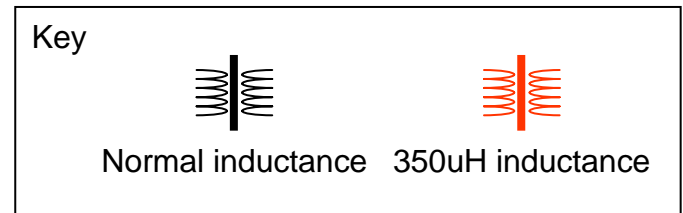
Proposal 1 - Alternative A problem

- PoE+ operation used as detection mechanism
  - PoE+ present so PD doesn't meet 350uH OCL
  - Assumption PSE RX meets new BER specification
    - PSE is actually Alternative A MidSpan
    - Far end PHY is a legacy device
  - Path from PD TX to far end RX lacks both 350uH OCL and conformance to new BER specification
- Need either 350uH OCL or new BER performance
  - Mandate ballast resistors in Midspan to limit imbalance current
    - Ensures 350uH OCL will be maintained
    - Not really practical due to heat and inefficiency
  - Require back to back PHYs in Midspan
    - RX path from PD would meet new BER specification
    - TX path to legacy device would meet 350uH OCL
    - Not really a practical solution due to complexity
    - MidSpan would become a two-port relay

Proposal 2 – TX based

- ## New 100BASE-T transmitter specification
  - Alternative to meeting 350uH OCL
    - Needs to mirror existing behaviour
  - Allows alternatives TX implementations
    - But a 350uH OCL implementation would still meet
  - Possible approach for this specification
    - Maximum Output Droop specification
- ## General solution
  - Applies to all 100BASE-T ports
  - Implementers can choose to meet either:
    - Existing 350uH OCL specification
    - New Maximum output droop specification
  - For PoE+ devices chosen specification has to be met under maximum imbalance current

Summary

- ## Consensus items

  ### [1] 100BASE-T Open Circuit Inductance

    - Issue with meeting specification above 8mA

- ## Options for 100BASE-T Open Circuit Inductance

  - Default option
    - Extend 350uH requirement to apply above 8mA
  - Other options
    - [1] RX Based
      - » Relax OCL specification above 8mA when PoE+ present
      - » Require PoE+ devices meet a new BER specification
      - » Problem with Alternative A Midspans
    - [2] TX Based
      - » New Transmitter specification