Transformer and Channel ad hoc

September 2008

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2 ad hoc with an average attendance of 14 people since the last report.

Agenda

- **Approaches Considered**
- **Update on low OCL System**
- **Q & A**
- **Next step.**

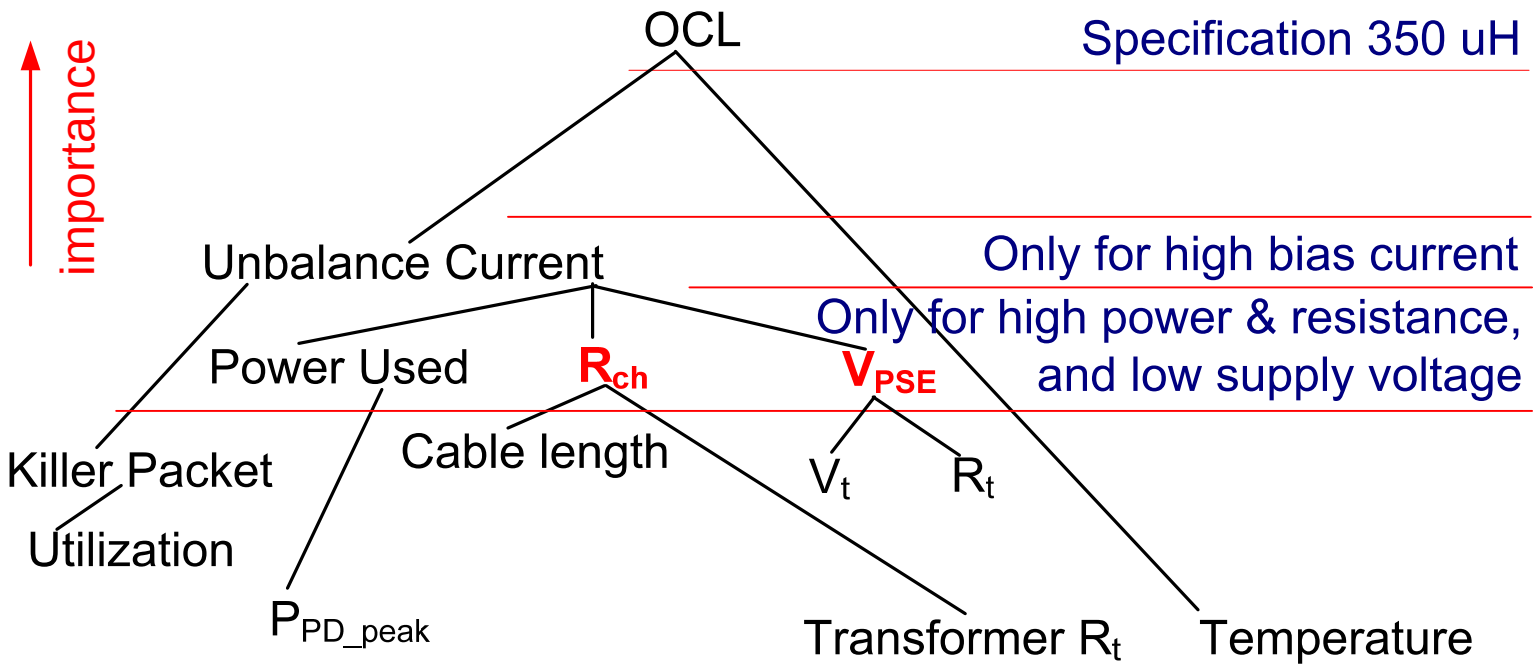
Approaches Taken

1. **Accept IEEE 802.3at D3.0 values.**
   Y: 13 N: 7
2. **Determine an OCL value for economically feasible magnetics using the same or smaller form factor as legacy solutions. Then have PHY vendors confirm whether recent baseline wander correct methods will ensure interoperation at all required data rates.**
   Y: 18 N: 2
   Use a Modern PHY
3. **Use statistics to determine the likelihood that the transformer OCL is below 350 uH and if that value is below ??? consider the system interoperable at the parameter levels selected.**
   Y: 16 N: 2
   Statistics Method
4. **Alternative A Midspan PSEs continue to be out of scope.**
   Y: 2 N: 13

The Task Force supports options 2 and 3.

The age of the universe is generally considered to be 14B years.

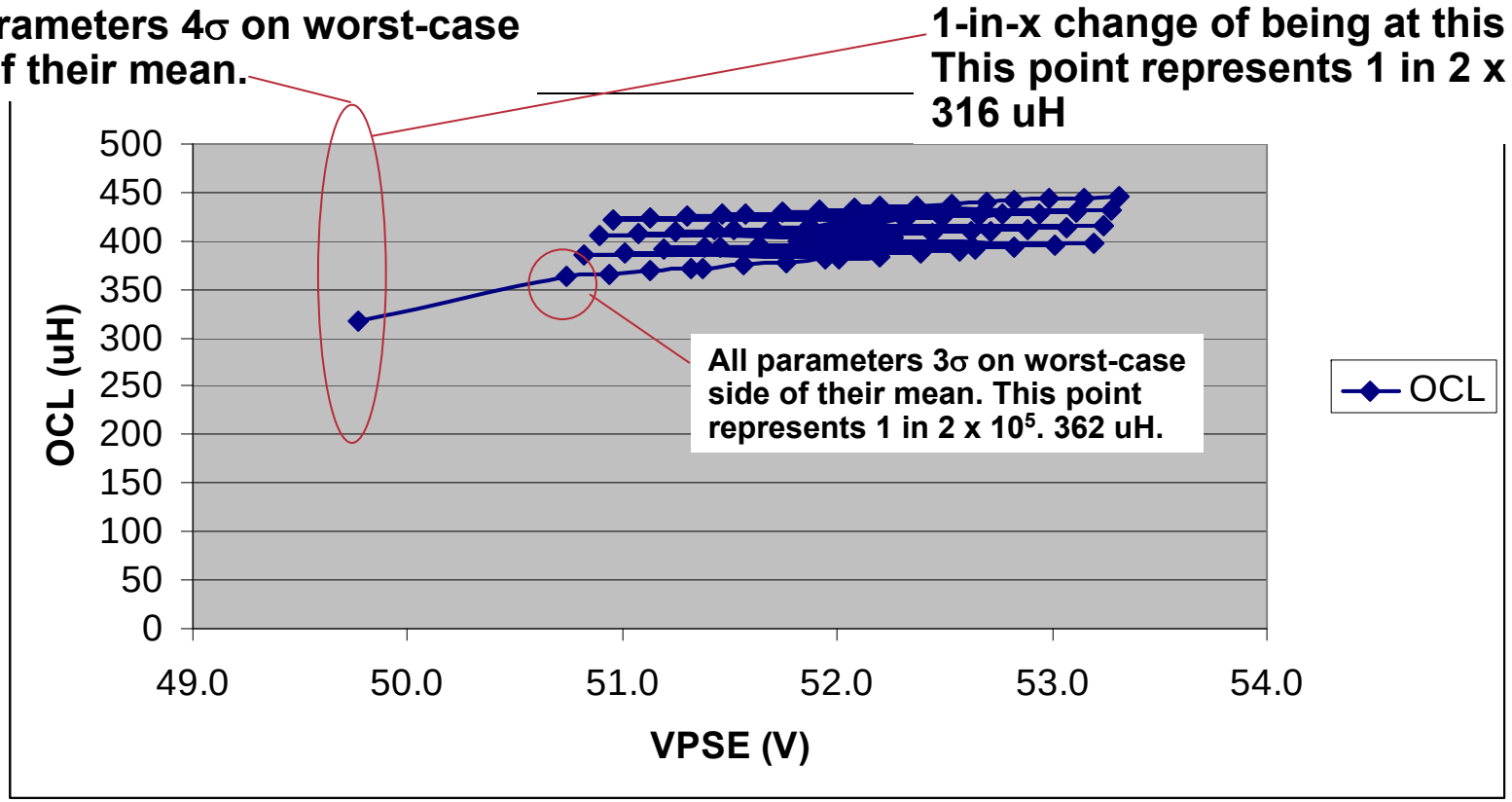
OCL Affecting Parameters



The next few pages will focus on R_{ch} and V_{pse} only.

OCL = Open Circuit Inductance of the Ethernet transformer.

OCL vs V_{PSE} for Legacy Transformers

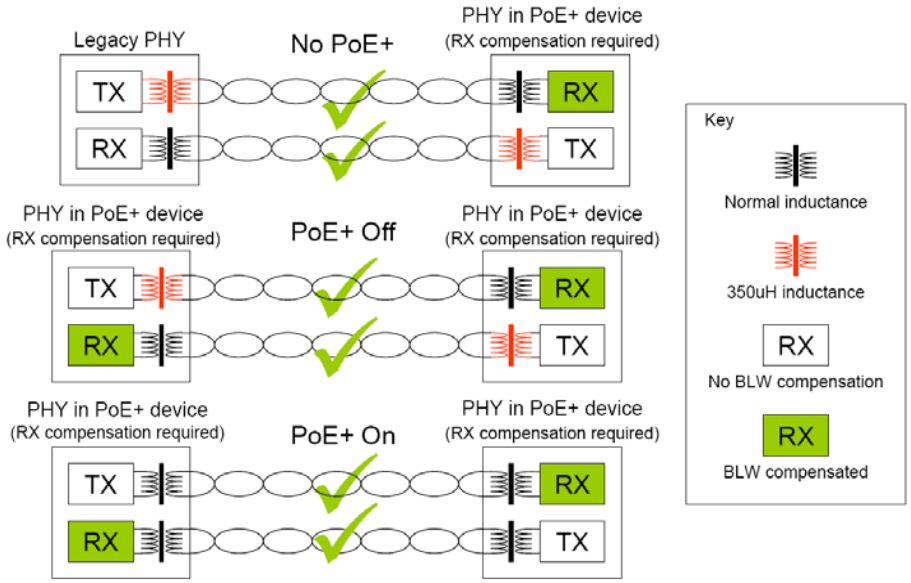


V_{PSE} and R_{ch} distribution with a 28.4 W PD peak load for an IEEE 802.3at system. This encompasses a cable reach from 0 to 115 m, and assumes a worst-case 3% channel resistance unbalance. No allowance for BLW induced bias current. Worst-case temperature.

Next step for the statistical method

- **Obtain data on channel resistance unbalance distribution.**
- **Obtain BLW probability.**
- **Refine OCL calculation to take into account the above two additional parameters.**
- **Refine proposed text.**
- **Make a motion for acceptance if required.**

Use a Modern PHY Method

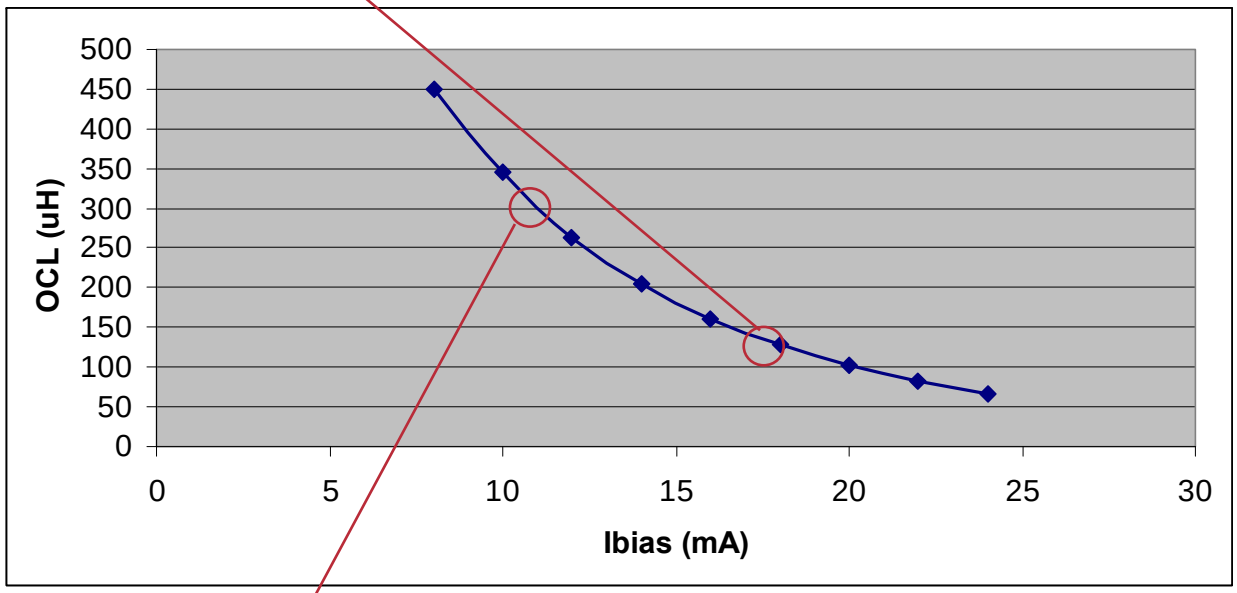


- **Determine an OCL value for economically feasible magnetics using the same or smaller form factor as legacy solutions. Then have PHY vendors confirm whether recent baseline wander correct methods will ensure interoperation at all required data rates.**
- **Require a a modern PHY that has BLW compensation.**

http://grouper.ieee.org/groups/802/3/at/public/nov07/law_1_1107.pdf

The equivalent worst-case OCL

Three parameters 4σ or more on worst-case side of their mean and BLW.
Ibias = 18.8 mA, OCL = 120 uH. Ibias = Iunbal/2 + 8 mA



The OCL is 320 uH when no BLW component is present and Ibias = 10.8 mA.
Three parameters are 4σ on the worst-case side of their mean.

This model produce 350 uH OCL at 10.2 mA bias current.

PHY Vendor Feedback

- **PHY vendors confirm 10BASE-T/100BASE-TXX/1000BASE-T PHYs released since June 2003 will interoperate and achieve a 10-8 or better BER while transmitting data with BLW with a transmitter (TX) open circuit inductance (OCL) of 120 uH.**

Anonymous

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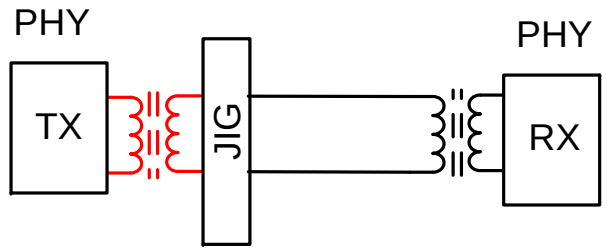
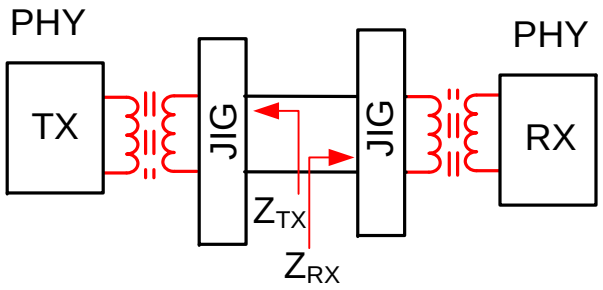
PHY Vendor Testing Continued

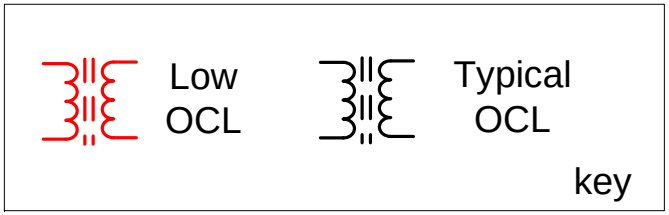
- Cable length short (> 0) and long (120 – 140 m).
- Annex A.2 DDJ and various internal and UNH BLW packets used. Unidirection, and bidirectional wander tested.
- OCL was made < 120 uH during BLW testing[1].
- > 10^{12}, 10^{13} bits transmitted without errors.
- BLW events on some patterns tested repeated about every 4 seconds.
- Different PHY generations and process geometries were tested.

[1] This test shows that PHYs operate at OCL less than is required, ~50 uH. 320 uH is required before BLW is present.

PHY vendor setup



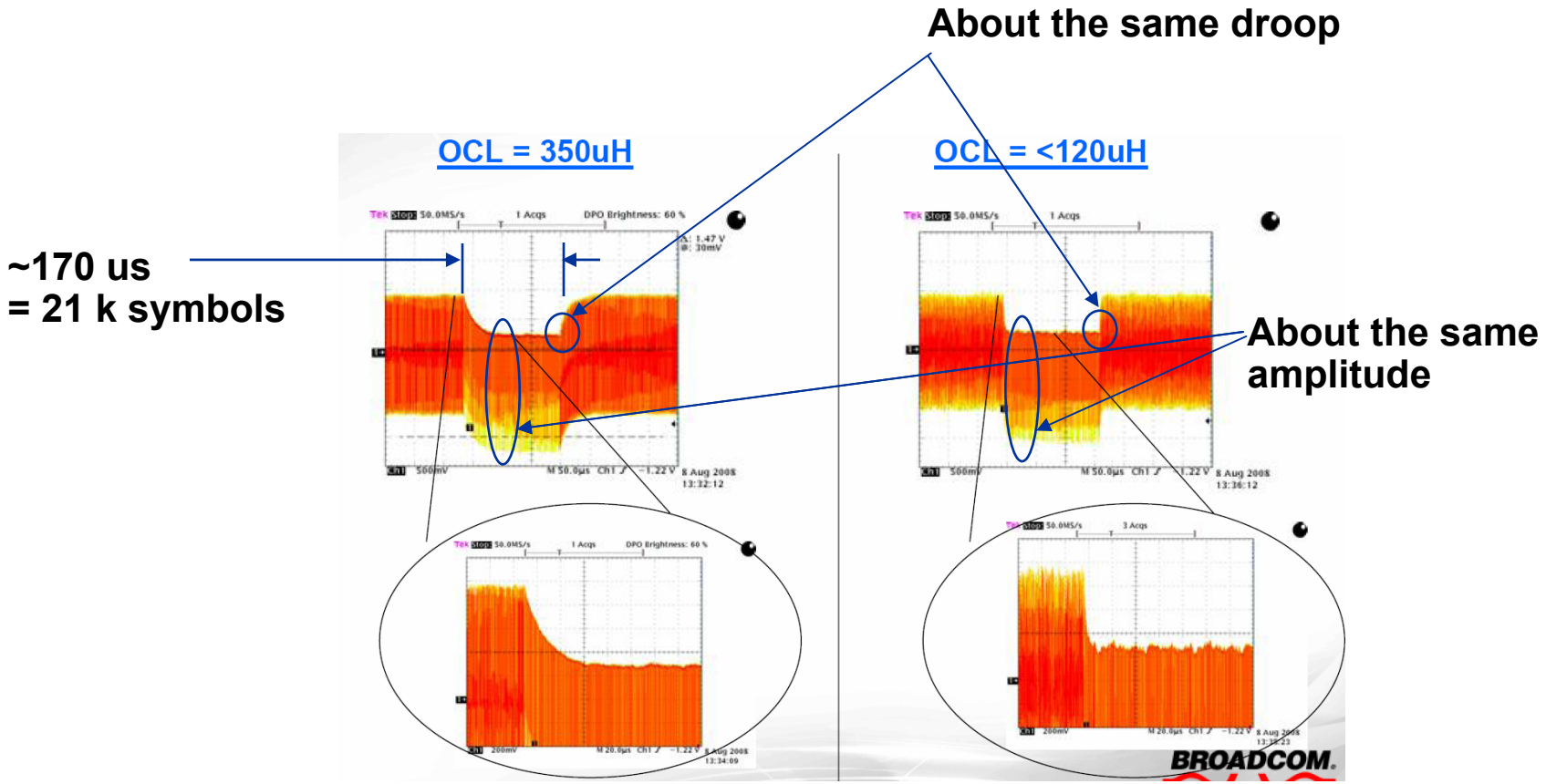




- **The OCL is dependent on the bias current.**
- **With peak PD load of 28.4 W the OCL is 316 uH.**
- **With a peak PD load and BLW the OCL is 120 uH.**
- **When the test jig sets the OCL to 120 uH, the OCL will drop more when BLW is present. OCL would be ~50 uH.**
- **Both setups were used and transferred data without errors.**

100BASE-TX BLW Scope Shots

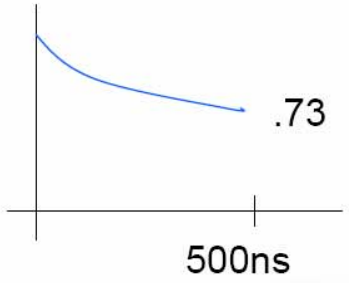
Modern PHYs look at differences between adjacent symbols to evaluate the current symbol.
=> TX OCL has little impact on data recovery.



What about Gigabit ?

40.6.1.2.2 Maximum output droop

The magnitude of the negative peak value of the waveform at point G, as defined in Figure 40–19, shall be greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. These measurements are to be made for each pair while in test mode 1 and observing the differential signal output at the MDI using transmit test fixture 2 with no intervening cable. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches its minimum value at the location indicated in Figure 40–19. Additionally, the magnitude of the peak value of the waveform at point J as defined in Figure 40–19 shall be greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches its maximum value at the location indicated in Figure 40–19.



$e^{-500ns/\tau} = 0.73$

$\tau = 1.6us \rightarrow$ OCL = 80uH

Gigabit already designed to tolerate low OCL

$\tau = L/R = L/50$

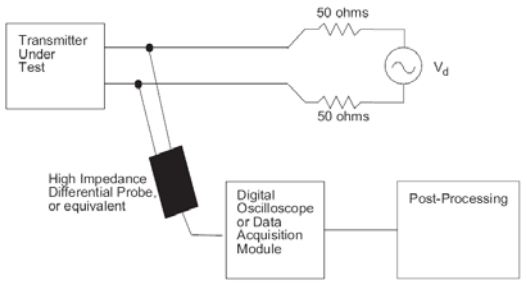


Figure 40–23—Transmitter test fixture 2 for droop measurement

Lower OCL Text Changes—Review

25.4.4a Change to 9.1.7, "Worst case droop of transformer"

A PHY in a Type 2 Endpoint PSE or Type 2 PD shall meet the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD or have an equivalent system time constant that exceeds 2.4 µs (for the PSE) or 7.0 µs (for the PD) when transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2.

Type 2 Endpoint PSEs shall meet the requirements of sublause 25.4.4a in the presence of (I_{unbal} / 2).

Type 2 PDs shall meet the requirements of 25.4.4a in the presence of (I_{unbal} / 2).

21	Current unbalance	I_{unb}	mA		3 % × I_{Cable}	1, 2	See 33.2.9.13

Parameter	Symbol	Units	Type 1 value	Type 2 value
Maximum DC cable current	I_{Cable}	A	0.35	0.6

Open Issues

- **Correct typo lunbal should be lunb.**
- **Should we require lunb = 3% x Ipeak for a type 2 system?**
  AdHoc YES

  Use the highest peak value.
  3% x 600 x 400/350 = 20.6 mA
  Therefore, lunb/2 = 20.6/2 = 10.3 mA.
  At 10.3 mA, OCL = 320 uH.
  At 10.3 + 8 = 18.3 mA, OCL = 120 uH

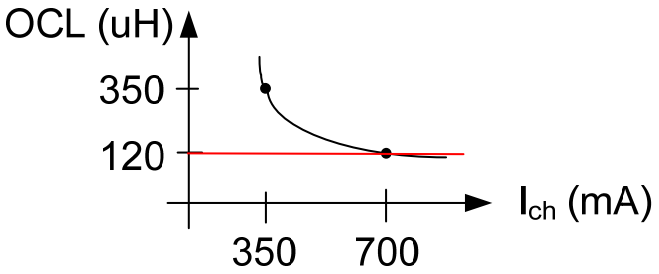
Instruct the Editor to Modify Table 33-11, item 21, PSE type field, reference 33.2.9.13.

Add new line item 21, Max field "3% x Ipeak", PSE type field, Type 2. Remove Type 2 from the preexisting item 21.

See comment 113, part of resolution.

Open Issues Continued

- **Plug "specsmanship hole."**
  A PHY in a system consisting of a Type 2 Endpoint PSE and ~~or~~ a Type 2 PD, delivering more than 12.95W average power, shall either meet the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD or have an equivalent system time constant that exceeds 2.4 µs (for the PSE) or 7.0 µs (for the PD) when transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2. AdHoc YES



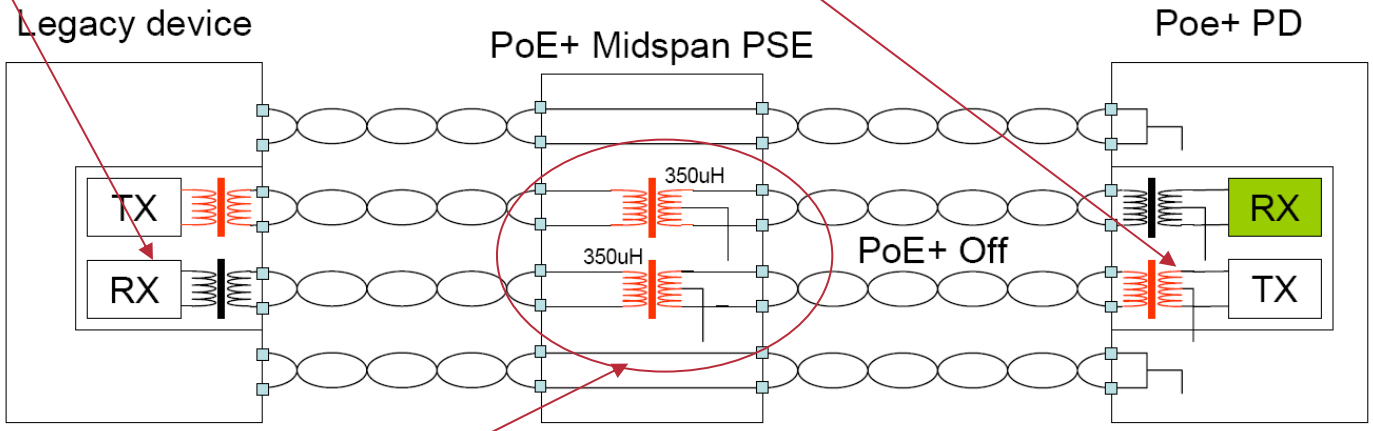
Open Issues Continued

- **How to enable low cost PDs?**
  A PHY in a system consisting of a Type 2 Endpoint PSE and a Type 2 PD, delivering more than 12.95 W average power, shall meet the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD or have an equivalent system time constant that exceeds 2.4 µs ~~(for the PSE) or 7.0 µs (for the PD)~~ when transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2.

  More PD ports are expected to ship than midspan ports. Requiring PDs to add cost to support midspans is the incorrect tradeoff.

Midspan with Legacy PHY Issue

Problem Statement: A midspan using signal pairs to power can create a 100BASE-TX system where a legacy PHY without BLW correction is connected to a PHY that transmits using a low OCL transformer.



Midspan on 100 MBPS signal path.

http://grouper.ieee.org/groups/802/3/at/public/nov07/law_1_1107.pdf

How to enable low cost PDs?

Ensure interoperability by:

a) Using the work of the Transformer and Channel ad hoc to show that interoperability is probable and therefore.

If this solution is accepted then no additional text is required.

b) Require Type 2 midspans that provide power on the data pairs of a 100BASE-TX systems to reduce the current unbalance to legacy levels (3% of 350 mA).

If this solution is required, the Editor should insert the following text in the appropriate place:

"Type 2 midspans that provide power on the data pairs of a 100BASE-TX system shall regulate channel unbalance currents to less than or equal to 10.5 mA."

c) Use a combination of a and b above. This would permit higher unbalance currents and lower than OCL.

If this solution is required, the Editor should insert the following text in the appropriate place:

"Type 2 midspans that provide power on the data pairs of a 100BASE-TX system shall regulate channel unbalance currents to less than or equal to TBD mA. "

How to enable low cost PDs?

d) Create a channel specification for Type 2 midspans that provide power on the data pairs of a 100BASE-TX system. If this solution is required, the Editor should insert the following text in the appropriate place:

Modify Table 33-11, item 21, PSE type field, reference 33.2.9.13.

Add new line item 21, Max field 1.75%, PSE type field, reference 33.2.9.13.

Add text to 33.2.9.13 after the last line: "Type 2 endpoint PSEs, "Type 2 midspan PSE that are not supply power on signal pairs of a 100BASE-TX system and Type 2 PDs shall operate using the larger unbalance specified in Table 33-11, item 21. Type 2 midspans that provide power on the data pairs of a 100BASE-TX system shall operate using the smallest unbalance specified in Table 33-11, item 21."

Channels with type 2 midspans supplying power on signal pairs for a 100 MPBS system shall have an unbalance factor of 1.75%. [3% x 350/600 = 1.75%]

How to enable low cost PDs?

e) Create a rebalancer cable that reduces a 3% channel resistance unbalance to 1.75%. Then neither the midspan or PD need to do anything extra.

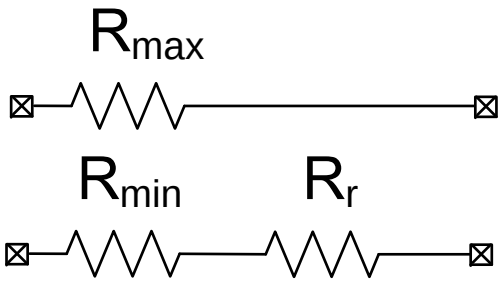
If this solution is required, the Editor should insert the following text in the appropriate place:

Modify Table 33-11, item 21, PSE type field, reference 33.2.9.13.

Add new line item 21, Max field 1.75%, PSE type field, reference 33.2.9.13.

Add text to 33.2.9.13 after the last line: "Type 2 endpoint PSEs, Type 2 midspan PSE that are not supply power on signal pairs of a 100BASE-TX system and Type 2 PDs shall operate using the larger unbalance specified in Table 33-11, item 21. Type 2 midspans that provide power on the data pairs of a 100BASE-TX system shall operate using the smallest unbalance specified in Table 33-11, item 21. A rebalancer cable may be used in place of a patch-cord/jumper-cable, see Figure 33-26, to adjust the channel unbalance resistance to less than or equal to the smallest unbalance specified in Table 33-11, item 21."

Rebalancer Cable



$$2R_{ch} = R_{\max} + R_{\min}$$

$$\frac{R_{\max} - R_{\min}}{R_{\max} + R_{\min}} \leq Unbalance\ \mathrm{Re}\ sis\ \tan\ ce$$

$$\frac{R_{\max} - R_{\min} + R_r}{R_{\max} + R_{\min}} \leq Unbalance\ \mathrm{Re}\ sis\ \tan\ ce$$

Rr >= 0.3125/2 ohm = 0.1563 ohms

Each 100 m signal pair has one Rr.

Length_max >= 0.6 m (reduced channel length)

Change in Rchan ~0.08 ohms

Additional power loss at 600 mA
29 mW

This assumes a 3% unbalance resistance that will be reduced to 1.75% when the correct rebalancer is added. The value of Rr would be adjusted to support different cable lengths.

Signal Powered 100BASE-TX Midspan Options

a) **Statistics show that interoperability is not probable.** 12 for 1 against

b) **Require PoE plus midspans to adjust unbalance current to PoE levels.** 10 for 4 against

c) **Use concepts in "a" and "b" to reduce the adjusted current levels.** 8 for 3 against

d) **Require midspan channels meet a tighter tolerance.** 14 for 2 against

Signal Powered 100BASE-TX Midspan Options

e) **Create a rebalancer patch cord to enable the tighter channel requirement.** 13 for 3 against

f) **Disallow this midspan option.** 8 for 3 against

g) **Adjust channel unbalance in the PD.** 3 for 11 against

h) **Require midspans that operate with PHYs with have no BLW correction to meet channel requirements.** 16 for 0 against

Proposed Solution to Enable Low Cost PDs

Instruct the Editor to place the following text in the appropriate place:

100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to PHY transmitter with 350 uH open circuit inductance (OCL). Alt-A Type 2 midspans that support 100BASE-TX shall ensure channel unbalance currents less than or equal to Type 1 Iunb, see Table 33-11, item 21.

See comment #112

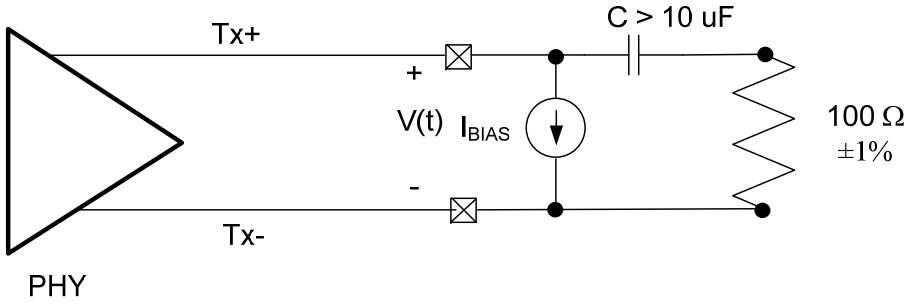
Add, additional information pointer to this from Table 33-11, item 21.

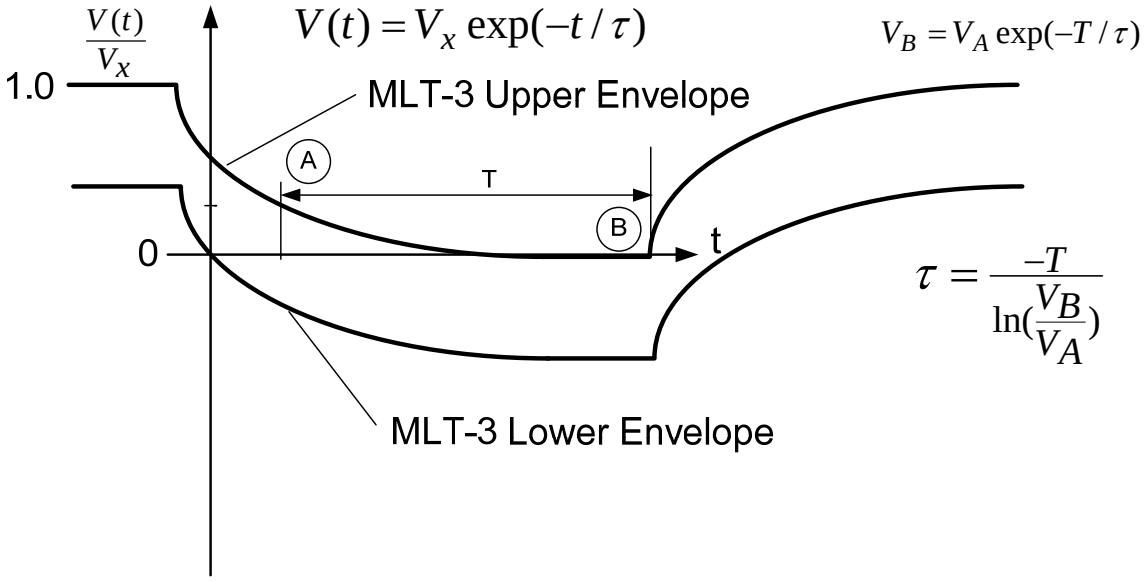
Open Issues Continued

- **Correct the system time constant:**
  A receiver in a Type 2 device shall meet the requirements of 25.4.4b. A transmitter in a Type 2 device delivering or accepting more than 12.95 W average power, shall either meet the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or the requirements of clause 25.4.4a.1.

See comment #112.

Open Issues Continued





Editor to grey the region between upper and lower MLT-3 envelope to represent MLT-3 transitions, and use their discretion to select the subclause in clause 25 to place the text and figures.

See comment #112.

Open Issues Continued

25.4.4a.1 Equivalent System Time Constant

While transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2, using the fixture shown in Figure 25-???, the equivalent system time constant, τ, shall be greater than 2.4 us, when calculated using measurement points A and B as defined in Figure 25-???. Point B is defined as the point of maximum baseline wander droop. Point A is defined as the point 150 us earlier in time from point B. These measurements are to be made for the transmitter pair and observing the differential signal output at the MDI with no intervening cable.

See comment #112.

Open Issues Continued

25.4.4b Addition to 10.1, 'Receiver'

A 100BASE-TX PMD in a Type 2 Endpoint PSE or Type 2 PD shall meet the following requirement. Differential voltage signals received at the MDI that were transmitted from a remote transmitter within the specifications of Clause 25 and have passed through a link specified in 25.4.6 are translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion.

This is the similar to the 1000BASE-T text:

40.6.1.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 40.6.1.2 and have passed through a link specified in 40.7 are translated into one of the PMA_UNITDATA.indication messages with a bit error ratio less than 10-10 and sent to the PCS after link reset completion. Since the 4-D symbols are not accessible, this specification shall be satisfied by a frame error ratio less than 10-7 for 125 octet frames.

See comment #112.

Open Issues Continued

Instruct the Editor to (Modified comment 234):

Suggest this information be moved to a new subclause of 33.4 'Additional electrical

specifications'. To do this:

[1] Delete page 57, line 44.

[2] Delete page 76, line 31.

[3] Add a new subclause as follows:

33.4.X 100BASE-TX transformer droop

100BASE-TX Type 2 Endpoint PSEs and 100BASE-TX Type 2 PDs shall meet the requirements of clause 25 in the presence of (Iunb / 2).

See comment #234

Next Step

- **Review low OCL proposal agreements.**
- **Determine if the statistical method should continue to be pursued.**
- **Make a motion for acceptance or resolved comments with ad hoc proposal.**