Comment Type: T  Comment Status: X
Clause 85.11.1.1. Style 1 Hardware Contact Definitions Table 85-12
This table requires that the current low speed electrical specification for the QSFP+ cable as defined by SFF8436 be violated. It should be a goal of IEEE802.3ba to facilitate the use of industry standard cables that are defined in other documents. SFF8436 includes an EEPROM cable management interface with a detailed memory map. The functional requirements of Table 85-12 have been addressed in the SFF8436 memory map.

Suggested Remedy
Table 85-12 should be deleted.

Proposed Response

Response Status: O

---

Comment Type: TR  Comment Status: X
Hardware contact definitions in Table 85-12 violate the QSFP connector specification of SFF-8436: the table requires that contact 27 be open in the case of a copper module, while the QSFP spec defines this contact as module presence pin and requires it to be grounded in the module. As a result of this discrepancy, passive QSFP copper cables created for all other standards using SFF-8436 will not be interoperable with 40GE. Conversely, if the connector is pinned out per table 85.11, the cable will not as a general rule be able to be used in Infiniband and other equipment already deployed in the field. While not strictly a problem from IEEE point of view, I believe this incompatibility will have negative impact on the broad market potential and future adoption of this standard. In addition, electronic keying is also required for CR10 and is currently missing, and defining it along the lines of table 85-12 causes even more severe discrepancy with the CXP specification (see my next comment).

Suggested Remedy
The entire section 85.11.1.1.1 as currently written needs to be deleted. There does not appear to be a way to define electronic keying without violating the QSFP spec. The reasonable solution is to use the SFF-8436 management interface, which has provisions for identifying the module as a copper or an optical module. Also, it is obvious that everyone will end up using the management interface anyway, because it is de facto industry standard and it does the job. If management interface definition is beyond the scope of the project, then we could either make an informative statement referencing the SFF-8436 management interface; or we could make a statement along the lines of “Electronic keying shall be used in order to enable detection of Style-1 plug connector versus fiber module or no module present. The details of implementation of such keying are beyond the scope of this standard”. This would prompt people to use the management interface without calling it out, or it would enable proprietary/custom designs along the lines of table 85-12.

Proposed Response

Response Status: O
Electronic keying needs to be defined for CR10 as well, in order to enable distinction of copper from fiber modules by the host. However, there does not appear to be a way to do this via hardware keys without violating the CXP spec, particularly as it is defined in the InfiniBand Architecture Specification. The only way to do this along the lines of Table 85-12 would be to have contact C20 open, and contact C21 pulled low. But C20 is the module presence pin that is required to be grounded in all cases by the CXP spec, and C21 is a shared interrupt/reset pin, so pulling it low will disrupt the operation of InfiniBand equipment. As a result, passive cables designed for Infiniband will not interoperate with CR10.

**Suggested Remedy**

Add an Electronic Keying section, stating: "Electronic keying shall be used in order to enable detection of CR10 plug connector versus fiber module or no module present. The details of implementation of such keying are beyond the scope of this standard."

**Proposed Response**

Response Status: O

---

The equation (83B-3) has an inequality sign for the [SDD21] Host Compliance Board insertion loss. Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

**Suggested Remedy**

Replace the inequality sign with an equal sign "=".

**Proposed Response**

Response Status: O

---

The equation (83B-4) has an inequality sign for the [SDD21] Module Compliance Board insertion loss. Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

**Suggested Remedy**

Replace the inequality sign with an equal sign "=".

**Proposed Response**

Response Status: O

---

unnecessary hyphen

**Suggested Remedy**

Change 'The-' to 'The'

**Proposed Response**

Response Status: O

---

unnecessary hyphen

**Suggested Remedy**

Change 'that packaged' to 'that is packaged'

**Proposed Response**

Response Status: O
Comment ID: 8

**Comment Type:** E
**Comment Status:** X

Proposed Response: 
Change 'Register_1.174' to 'Register 1.174'

Comment ID: 9

**Comment Type:** T
**Comment Status:** X

Proposed Response: 
Change 74.8.4.1 and 74.8.4.2 need to be updated for multi-lane operation

Proposed Response: 
Change to:

FEC_corrected_blocks_counter and FEC_corrected_blocks_counter_i count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC再说_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.87 (1.172, 1.173) and 45.2.1.89 (1.176 to 1.215).

FEC_uncorrected_blocks_counter and FEC_uncorrected_blocks_counter_i count once for each uncorrected FEC block processed when FEC SIGNAL.indication or FEC再说 SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.88 (1.174, 1.175) and 45.2.1.90 (1.216 to 1.255).

Comment ID: 10

**Comment Type:** T
**Comment Status:** X

Proposed Response: 
Change DME_receive_idle to an_receive_idle
also do the same for mr_parallel_detection_fault variable

Comment ID: 11

**Comment Type:** T
**Comment Status:** X

Proposed Response: 
Delete '(IEEE)'

Comment ID: 12

**Comment Type:** T
**Comment Status:** X

Proposed Response: 
Delete '(IEEE)'

**Comment Type:** TR/technical required
**Comment Status:** D/dispatched
**Response Status:** C/closed

**Comment Type:** ER/editorial required
**Comment Status:** A/accepted
**Response Status:** W/written
13. In the equations within the draft, the use of "\times" to signify multiplication is inconsistent. According to the style manual, a multiplication sign "\times" should only be used to indicate multiplication of two numbers (e.g., "1 \times 10^4" or "3 \text{cm} \times 4 \text{cm}"). Some equations do not use "\times" e.g. "10\log" or "2f" and others use "10 \times \log" or "2 \times f"

**Suggested Remedy**


Note there is another comment against equation 85A-4

- Remove all but the first "\times" from equation 85-16
- Change equation 85-23 from "= -0.7 - 0.2\times10^{-9}(f\times10^6)" to "= -0.7 - 0.2\times10^{-3}f"
- Change equation 85-24 from "= -0.7 + 0.2\times10^{-9}(f\times10^6)" to "= -0.7 + 0.2\times10^{-3}f"
- Remove the first two "\times"s from equations 85-31 and 85-32
- Remove the "\times" between "20" and "\log" in equations 85-35, 85A-1 and 85A-2

**Response Status**: O

14. The draft is inconsistent on how it defines the frequency break points in equations. For some multi-segment limit lines, there is a small discontinuity at the break point, so it should be clear which limit applies to the exact break frequency.

**Suggested Remedy**

- In equations 85-23 from "= -0.7 - 0.2\times10^{-9}(f\times10^6)" to "= -0.7 - 0.2\times10^{-3}f"
- Change equation 85-24 from "= -0.7 + 0.2\times10^{-9}(f\times10^6)" to "= -0.7 + 0.2\times10^{-3}f"
- Remove the first two "\times"s from equations 85-31 and 85-32
- Remove the "\times" between "20" and "\log" in equations 85-35, 85A-1 and 85A-2

**Response Status**: O

15. The draft is not consistent in its use of parameter names and figures illustrating limit lines. For example "Return loss" and "Reflection response, SDD22" are used for the same parameter.

**Suggested Remedy**

- Apply changes as described in dambrosia_01_0909.pdf

**Response Status**: O

16. The definition of Skew Variation is not correct.

- Consider a link with relative delays on 4 lanes of 0, 20, 20, 20 UI.
- The definition of Skew is: Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits.

**Suggested Remedy**

- The Skew Variation is defined as: Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation.

**Response Status**: O
Draft 2.2 Comments

IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

WG 2nd recirculation ballot

---

Cl 83 SC 83.5.4 P 213 L 13 # 17
Anslow, Peter
Nortel Networks

Comment Type E
Comment Status X

Double full stop ".."

Suggested Remedy
Change ".." to "."

Proposed Response Response Status O

---

Cl 83A SC 83A.3.3 P 385 L 19 # 18
Anslow, Peter
Nortel Networks

Comment Type E
Comment Status X

In Table 83A-1, the "Maximum De-emphasis" is given as 7.0 dB
In Table 83B-3, the "Maximum De-emphasis" is given as 6.0 dB
In accordance with the response to comment #501 against Draft 1.1, these should be 7 dB and 6 dB respectively.

Also on page 398 line 33 7.0 dB should be 7 dB

Suggested Remedy
In Table 83A-1, change "7.0" to "7"
In Table 83B-3, change "6.0" to "6"
On page 398 line 33, change "7.0" to "7"

Proposed Response Response Status O

---

Cl 85 SC 85.10.3 P 263 L 4 # 22
Anslow, Peter
Nortel Networks

Comment Type E
Comment Status X

The Cable assembly insertion loss deviation is required to be met from 50 MHz to 7.5 GHz. However, in Figure 85-7 the limits are illustrated from 50 MHz to 6 GHz only.
Also applies to Figures 85A-7, 85A-10, 85A-11

Suggested Remedy
Extend Figures 83A-6, 83A-7, 83A-10, 83A-11 to 10 MHz

Proposed Response Response Status O
Cl 85 SC 85.10.4 P 263 L 28 # 23
Anslow, Peter Nortel Networks

Comment Type E Comment Status X
Double full stop ".."

SuggestedRemedy
Change ".." to "."

Proposed Response Response Status O

Cl 85 SC 85.10.8 P 266 L 41 # 24
Anslow, Peter Nortel Networks

Comment Type E Comment Status X
This says:
"where IL IL denotes the value..."

SuggestedRemedy
change "IL) IL denotes the value..." to " IL is the value..."

Proposed Response Response Status O

Cl 85 SC 85.8.3.6 P 256 L 48 # 25
Anslow, Peter Nortel Networks

Comment Type E Comment Status X
Some of the equations in Clause 85 introduce an extra variable name that is not used elsewhere.
For example Equation 85-16 starts:
ILtf(f) <= ILtfmax(f) = (0.054)...
The ILtfmax(f) variable is not referred to anywhere in the draft and only serves to complicate the equation.

Where there are limit lines for both max and min for the same parameter (e.g., Equations 85-23 and 85-24) and the extra variables e.g. ILDmin(f) and ILDmax(f) are used elsewhere, they should be retained.
Also applies to Equations 85-35, 85A-3 and 85A-4

SuggestedRemedy
In 85-16 change "ILtf(f) <= ILtfmax(f) = (0.054)...

In 85-35 change "ILCATF(f) <= ILcatfmax(f) = (0.029)...

In 85A-3 change "ILCh(f) <= ILChmax(f) = IL..." to "ILCh(f) <= IL..."

In 85A-4 change "ILCh(f) <= ILChmax(f) = (0.05)..." to "ILCh(f) <= (0.05)...

Proposed Response Response Status O

Cl 85 SC 85.2 P 240 L 44 # 26
Anslow, Peter Nortel Networks

Comment Type E Comment Status X
Several references in Clause 85 that should be cross-references are not.

SuggestedRemedy
Make the following references to other places in the draft cross-references.

Page 240, line 44, "80.3"
Page 244, line 20, "85.10"
Page 246, line 39, "85.7.4"
Page 247, line 45, "45.2.1.7.4" (not blue)
Page 247, line 53, "45.2.1.7.5" (not blue)
Page 251, line 27, "85.7.12"
Page 252, line 3, "83.5.10" (not blue)
Page 252, line 34, "83.5.10"
Page 253, line 42, "85.7.3.2.3"
Page 267, line 28, "85.10"

Proposed Response Response Status O
<table>
<thead>
<tr>
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<th>CI</th>
<th>SC</th>
<th>P</th>
<th>L</th>
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<tr>
<td>27</td>
<td>85</td>
<td>85.9</td>
<td>259</td>
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<td>85A</td>
<td>85.12</td>
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<td>46</td>
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<td>85A</td>
<td>85A.5</td>
<td>423</td>
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<td>85A</td>
<td>85A.5</td>
<td>423</td>
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<td>85A</td>
<td>85A.4</td>
<td>422</td>
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<td>85A</td>
<td>85A-4</td>
<td>422</td>
<td>46</td>
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**Comment Type**

- **E** editorial
- **T** technical
- **G** general

**Comment Status**

- **A** accepted
- **R** rejected
- **D** dispatched
- **X** unresolved
- **O** open
- **W** written
- **C** closed
- **U** unsatisfied
- **Z** withdrawn

**Proposed Response**

- **Anslow, Peter**

**Suggested Remedy**

- **Page 277, line 46, "14.7" should be blue**
- **Page 278, line 11, "Clause 21" should be blue**
- **Page 278, line 44, "Clause 21" should be blue**

- **Equation 85A-2 starts:**
  "ILPCB(f) <= ILPCBmin(f) = (0.103)"... but ILPCB(f) should be greater than ILPCBmin(f) not less than.

- **Equation 85A-4 starts:**
  "ILCh(f) + ILH(f)" to "ILCh(f) + ILH(f)"

- **For equations 85A-3, 85A-4 and 85A-5 change the phrase "is the frequency in MHz" to normal font.**

- **For equations 85A-3, 85A-4 and 85A-5 change the phrase "is the frequency in MHz" to italic font.** This should be normal font.

- **Change "through.85A.7" to "through 85A.7"**

- **Change "(0.05 x ILCamax(f)) x (2 x ILHost(f))" to "0.05ILCamax(f) + 2ILHost(f)"**

- **Change "ILCh(f)" to "ILCh(f)"**

- **Change "(ILCh(f)" to "ILCh(f)"**

- **Change "(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)" is unclear and does not conform with the style manual.**

- **"(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)" is unclear and does not conform with the style manual.**

- **"(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)" to "(i.e., the maximum insertion loss between TP0 and TP1 and between TP4 and TP5)"**
Comment Type  T  Comment Status  X
Table 86-5 requires SIGNAL_DETECT to be OK when:
"Optical power at TP3 >= stressed receiver sensitivity (max) in OMA in Table 86.8" This is -5.4 dBm (OMA).
However, in Table 86-7 "Characteristics of signal within, and at the receiving end of, a compliant optical channel" we see that the OMA, each lane can be -7.9 dBm. Consequently, a fully compliant link can have SIGNAL_DETECT = FAIL

SuggestedRemedy
In Table 86-5 change:
"Optical power at TP3 >= stressed receiver sensitivity (max) in OMA in Table 86.8" to
"Optical power at TP3 >= Optical Modulation Amplitude (OMA), each lane in Table 86.7"

Proposed Response  Response Status  O

Comment Type  E  Comment Status  X
This says "an ideal 4th order Bessel Thompson response". However all other occurrences use "fourth" rather than "4th" and the style manual also states that "In general text, isolated numbers less than 10 should be spelled out."

SuggestedRemedy
Change "an ideal 4th order" to "an ideal fourth order"

Proposed Response  Response Status  O

Comment Type  E  Comment Status  X
In the equations of clause 86A, the phrase "f is the frequency in gigahertz" is used. In the rest of the draft (27 instances) this is "f is the frequency in GHz". In the base document the words "gigahertz", "megahertz" or "kilohertz" do not occur at all.

SuggestedRemedy
Change "gigahertz" to "GHz" throughout clause 86A (14 instances)

Proposed Response  Response Status  O
<table>
<thead>
<tr>
<th>Comment ID #</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Comment</th>
<th>Proposed Response</th>
<th>Response Status</th>
<th>Comment ID #</th>
<th>Comment Type</th>
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<th>Comment</th>
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<th>Response Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>38</td>
<td>E</td>
<td>X</td>
<td>The header is not consistent with respect to having a space between the number and unit. Starting on this page there is not space, but there should be a space.</td>
<td>Change: IEEE 802.3ba 40Gb/s and 100Gb/s Ethernet Task Force</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>TR</td>
<td>X</td>
<td>The CR4/10 Host IL (85-14) and the nPPI recommended electrical channel (86A-19) both defined with connector and test fixtures) should be IDENTICAL also for low frequencies (see page 4 of mazzini_01_0909).</td>
<td>Harmonize the curves as above.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>TR</td>
<td>X</td>
<td>The recommended maximum loss for the PCB only (without connector) (Draft 2.2, page 446, row 51), should be aligned with formula 85A-2 (Transmitter and receiver differential printed circuit board trace loss) that gives maximum PCB loss @5.156GHz = 3.5dB (see page 4 of mazzini_01_0909).</td>
<td>Harmonize the loss.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>TR</td>
<td>X</td>
<td>The connector loss (calculated as 85-37 values minus 85-35 and 85-16) of the test fixture improves when frequency increase (see slide 5). Above formulas should be corrected to avoid this.</td>
<td>As above.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>TR</td>
<td>X</td>
<td>The test fixture (85-16) and the HCB (86A-4) loss formulas must be IDENTICAL. In D2.2 losses just cross at same value @ 5.165GHz (see page 5 of mazzini_01_0909).</td>
<td>Harmonize the loss.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Comment Type: TR  Comment Status: X

Formula 86A.19 seems incorrect from in the range from 0.2 to 7GHz, should be
\[= -0.114-0.8914*?f-0.846*f\]

Suggested Remedy
Change the + to a -.

Proposed Response  Response Status: O

---

Comment Type: TR  Comment Status: X

There is no limit to the potential increment rate of the PRBS31 checker referenced in
49.2.12. The checker implementation is difficult to match at high increment rates or in the
presence of burst errors (the source synchronous descrambler implementation error
multiplication factor depends on burst pattern).

There will be less scope for a complex implementation in a PMA device versus a PCS.

For most practical purposes stringent matching of the 49.2.12 implementation is not
necessary. It would be sufficient to match the result of a 49.2.12 implementation only for
isolated single bit errors and at errors rates less than 1 in a thousand.

Suggested Remedy
Replace:
(see 49.2.12)

With:

The PRBS31 checker shall match the results of the checker implementation in 49.1.12 for
isolated single bit errors and at errors rates less than 1 in a thousand.

Proposed Response  Response Status: W

[Editor's Note: Commenter did not indicate comment type. Assigned comment Type TR]
### Comment ID: 48

**Cl 87 SC 8.11.1 P 326 L 41**

**Proposed Response**

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>TR</th>
<th>Comment Status</th>
<th>X</th>
</tr>
</thead>
</table>

**Comment:**

"The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz."

Providing such a wide range of frequency (in addition to amplitude) makes compliance testing difficult.

**Suggested Remedy**

Select a single sinusoidal amplitude interferer frequency of 1GHz.

There will be a contribution at the September interim to support this comment.

### Comment ID: 49

**Cl 87 SC 8.11.1 P 326 L 15**

**Proposed Response**

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>TR</th>
<th>Comment Status</th>
<th>X</th>
</tr>
</thead>
</table>

**Comment:**

"Stressed receiver sensitivity shall be within the limits given in Table 87-8 for 40GBASE-LR4 if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2."

Stressed receiver sensitivity compliance is a normative requirement, but the test setup has a number of variable parameters: BT filter parameters, sinusoidal jitter frequency, sinusoidal amplitude interferer frequency and amplitude, etc.

Given the wide range of alternative configurations that could meet the stressed eye VECP and SEJ values, is it the intention of the committee that all such test setups be tested against the Stressed receiver sensitivity requirement?

I.e. In order to be compliant is it sufficient to demonstrate compliance at just one such configuration, or does failure at any such configuration mean an implementation is non-compliant.

I see hazards in either position.

A single pass might allow an implementation to select a set of parameters particularly favorable in order to pass.

Conversely demonstrating that there is no single combination of parameters that does not cause a failure would cause testing to take an impracticable amount of time.

**Suggested Remedy**

Add some text indicating the committees intention.

There will be a contribution at the September interim to support this comment.

<p>| Proposed Response | Response Status | O |</p>
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Suggested Remedy</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>T</td>
<td>X</td>
<td>It is more appropriate to define RMSdev as the square-root of the sum of the square values sigma_1^2 and 2^2. Similarly for the RMSHdev.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>51</td>
<td>TR</td>
<td>X</td>
<td>The transmitter output waveform requirements do not address the case where the transmitter is requested to INITIALIZE per 72.6.10.4.2.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>52</td>
<td>TR</td>
<td>X</td>
<td>Correct the mapping from qi to the normalized coefficients c(n) by replace all instances of &quot;Dw&quot; with &quot;Dp&quot;.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>53</td>
<td>TR</td>
<td>X</td>
<td>Definitions of P2 and P3 are not correct.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>54</td>
<td>E</td>
<td>X</td>
<td>In relation to the presentation of equations in the draft, consult the IEEE style guide 17.3 for instructions on the use of italic and upright text in mathematical expressions.</td>
<td>Update equations to be consistent with the format prescribed by the style guide.</td>
<td>O</td>
</tr>
<tr>
<td>55</td>
<td>TR</td>
<td>X</td>
<td>Equations (85-29) and (85-30) are in error. The expression <em>(sinc</em>2 x (f/fn))^2 should be <em>(sinc</em>2 x (f/fn))^2 in both cases.</td>
<td>Remove the superfluous &quot;*&quot; in both equations.</td>
<td>O</td>
</tr>
</tbody>
</table>
Comment ID # 56

Healey, Adam  
LSI Corporation

Comment Type T  Comment Status X
The specified frequency range for channel insertion loss is inconsistent with the frequency range for cable assembly insertion loss in 85.10.2. It seems that they should be consistent. This should also apply to the transmitter and receiver differential printed circuit board trace loss in 85A.4 and the channel insertion loss deviation in 85A.7.

Suggested Remedy
Recommend using a consistent frequency range throughout.

Proposed Response  Response Status O

Comment ID # 57

Healey, Adam  
LSI Corporation

Comment Type T  Comment Status X
For the cable assembly, specifications for insertion loss to crosstalk ratio were replaced with integrated crosstalk noise requirements. It seems that the channel requirements should follow suit.

Suggested Remedy
Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.

Proposed Response  Response Status O

Comment ID # 58

Healey, Adam  
LSI Corporation

Comment Type T  Comment Status X
There are no requirements on PSXT(f) and it is not used as a parameter in any of the cable assembly specifications.

Suggested Remedy
Remove 85.10.7.

Proposed Response  Response Status O

Comment ID # 59

Healey, Adam  
LSI Corporation

Comment Type TR  Comment Status X
MDNEXTloss is defined to be computed over that range of 50 to 6000 MHz, but the calculation that uses this quantity, integrated crosstalk noise (85.10.8), requires values from 50 to 10000 MHz.

Suggested Remedy
Correct the frequency range to be consistent with 85.10.8. Also correct the frequency range in 85.10.6 (MDFEXTloss).

Proposed Response  Response Status O

Comment ID # 60

Dawe, Piers  
Independent

Comment Type E  Comment Status X
"is the frequency in MHz" should not be italicized.

Suggested Remedy
Correct two occurrences in this subclause, as well as an occurrences in 85A.7.

Proposed Response  Response Status O
Elsewhere in 802.3 where a Bessel-Thomson response for measurement (scope or reference receiver) is specified, it isn't called "3 dB upper electrical cutoff frequency" but "bandwidth" or "reference frequency fr" or simply "7.5 GHz Bessel-Thomson".

Please change "3 dB upper electrical cutoff frequency" to "reference frequency fr", or change "ideal fourth-order Bessel-Thomson response with a 3 dB upper electrical cutoff frequency of * GHz." to "ideal * GHz fourth-order Bessel-Thomson response with a bandwidth of * GHz."

Comment ID # 63

Dawe, Piers Independent

Proposal Response

 change "nPPI" to "PPI" throughout.

Comment ID # 64

Dawe, Piers Independent

Proposal Response

 change equations 85–16 and 85-35 so they are consistent with 86A-4 and 86A-5 respectively.

Comment ID # 67

Dawe, Piers Independent

Proposal Response

 85.8.3.4's "Insertion loss TP0 to TP2 or TP3 to TP5" is (above 200 MHz) consistent with the minimum SDD21 of host PCB, connector and HCB in 86A.6. The mated test fixtures insertion loss limits of 85.10.10.1 are consistent with the through response (SDD21) limits of mated HCB-MCB in 86A.5.1.1.2. Yet the test fixture insertion loss of 85.8.3.7 and the cable assembly test fixture insertion loss of 85.10.9 do not agree with the reference through responses (SDD21) of HCB and MCB in 86A.5.1.1.1. 85.8.3.7 and 85.10.9 use scaled backplane Amax while 86A.5.1.1.1 is based on experience with actual compliance boards. Because compliance boards are not backplanes (e.g. may use PTFE dielectric rather than FR4), the equations in 86A.5.1.1.1 are preferable.

My preferred solution is change "NEXT loss" to "NEXT" and "MDNEXT loss" to "MDNEXT", and flip the signs.
Proposed Response

Comment ID # 68

Cl 86A SC 86A.6 P 446 L 37 # 68
Dawe, Piers Independent

Comment Type T Comment Status X

Sign error in equation 86A-19. It should be a scaled version of D2.1 86A-20.

SuggestedRemedy

Change + 0.846f to – 0.846f.

Proposed Response

Response Status O

Comment ID # 69

Cl 82 SC 82.2.1 P 171 L 22 # 69
Dawe, Piers Independent

Comment Type T Comment Status X

Clarifying D2.1 comment 32:

There are two error counting mechanisms that can be used on 64B/66B signals: errored blocks and BIP errors. For isolated errors at error rates of interest, they will give near-identical results. But if burst errors are involved, the errored block counter will typically count 1 per burst while the BIP error counters will typically count the number of errors in the burst.

We should be unambiguous which is meant by BER for the purposes of compliance. As the errored block counter is not very good in service at good BERs, we expect in-service monitoring to use BIP (that's why it was introduced). It is HIGHLY desirable that the same definition of BER apply in compliance testing with the scrambled idle signal as in service. Also, as MTTFPA is so important and burst errors are a threat to it, BIP counting is preferable for another reason.

The response to D2.1 comment 32 points out that BIP counting saturates too low for the current hi_ber threshold. So continue with block counting (as is) for the BER monitor state diagram, but...

SuggestedRemedy

Say that BER for 64B/66B signals (including the scrambled idle signal) is defined by BIP error counting (rather than by the BER monitor state diagram). Although the count from the BER monitor state diagram may be useful for diagnostics at very bad BER.

Proposed Response

Response Status O
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<th>Line</th>
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<td>86A</td>
<td>86A.4.1</td>
<td>428</td>
<td>21</td>
<td>T</td>
<td>X</td>
<td>Add row, Termination mismatch at 1 MHz, max 5%</td>
<td>O</td>
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<tr>
<td>73</td>
<td>86A</td>
<td>86A.4.2</td>
<td>431</td>
<td>21</td>
<td>T</td>
<td>X</td>
<td>Confirm it or change it to a better number. Delete &quot;TBC&quot;</td>
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<td>86A</td>
<td>86A.5.1.1.2</td>
<td>434</td>
<td>44</td>
<td>T</td>
<td>X</td>
<td>Do we have measurements on QSFP and CXP mated HCB-MCB reflection response?</td>
<td>O</td>
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<tr>
<td>75</td>
<td>83</td>
<td>83.5.10</td>
<td>215</td>
<td>31</td>
<td>T</td>
<td>X</td>
<td>Increase 31 by the appropriate Skew Variation or say &quot;a delay of 31 UI plus the allowance for Skew Variation for the downstream sublayers as given in Table 80-5.&quot; But see another comment.</td>
<td>O</td>
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</table>

**Proposed Response**

| TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general |
| COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn |
| SORT ORDER: Comment ID |

**Page 16 of 47** 9/4/2009 6:10:21 PM
87.8.11.2 has a definition of VECP that contradicts the rest of 802.3. Detail follows:

In 52.9.9.2, VECP is defined as $10 \log(OMA/AO)$. Applies to 10G, scrambled, including 10GEPON. Also applies in 86.8.4.7. In 58.7.11.2, VECP is defined as $10 \log(10^{10}(AN/AO))$, where AN is to be measured with a square wave pattern consisting of four to eleven consecutive ones followed by an equal run of zeros. Applies to 100M and 1G, block coded.

In 53.9.14, VECP is defined as $10 \log(AO/AN)$ (sign error), where "AN is the normal amplitude without ISI, as measured in Figure 53–12." Applies to 10GBASE-LX4 (3.125 GBd, block coded).

10GBASE-LRM doesn't use VECP.

In D2.2 87.8.11.2, VECP is defined as $10 \log(OMA/AO)$, where AN is the normal amplitude without ISI, as shown in Figure 52–11 but 52.9.11 gives a precise definition.) D2.2 88.8.5.1 uses the 52.9.9.2 definition of VECP while 88.8.10 uses 87.8.11.

Suggested Remedy

Definitions and stressed eye generators will be shared across 40GBASE-LR4, 10GBASE-LR, 10GBASE-ER and 10GEPON, so 87.8.11.2 should conform.

Change the definition of VECP to $10 \log(OMA/AO)$. To avoid confusion, modify Figure 87–4 to remove "AN" (which is the "normal amplitude without ISI", 52.9.9.2 says "OMA is the normal amplitude without ISI", as shown in Figure 52–11 but 52.9.11 gives a precise definition.)

D2.2 88.8.5.1 uses the 52.9.9.2 definition of VECP while 88.8.10 uses 87.8.11.

Comment Type TR  Comment Status X

The test fixture insertion losses aren't maxima, they are reference losses. See text at 86A.5.1.1.

Suggested Remedy

Change "maximum" to "reference" here and in 85.10.9.

Comment Type TR  Comment Status X

As I pointed out in D2.1 comment 35, S-parameters define power gain, not loss. |SCC22| as a ratio must be <1, [SCC22] in dB must be negative. I'm sure our readers can cope with S-parameters and negative numbers.

Suggested Remedy

Change the signs on the right hand side, change the direction of the inequality back to <= as in D2.1.

Comment Type TR  Comment Status X

The larger delay could be generated by choosing appropriate seeds for each lane's PRBS generator and starting the generators together, but that's implementation.

Suggested Remedy

The first part of the remedy is similar to last time:

Change "on each of the lanes" to "on each of the PCS lanes" here and at line 30. Change "one lane and any other lane" to "one PCS lane and any other PCS lane" in the paragraphs beginning line 38 and line 50, change "lane" or "lanes" to "PCS lane" or "PCS lanes".

Delete "Note that bit multiplexing of per-lane PRBS31 may produce a signal which is not meaningful for downstream sublayers."

Provide 20 PRBS31 error counters in each direction, one per PCS lane.

Another solution which would take a few more words would be to generate by 10G lanes and check by 20G PCS lanes, for 100G. Do we have a name for a 10G lane? For 40G, because we have a binary series of lane speeds, generating per lane (whatever that is) and checking per (10G) PCS lane is ideal, but generating by 10G lanes with offset would still work.

Increase the 31 bits (UI) minimum delay between generator lanes to a number TBD, around 2000 UI.

Comment Type TR  Comment Status X

As a ratio must be <1, [SCC22] in dB must be negative. I'm sure our readers can cope with S-parameters and negative numbers.

Suggested Remedy

Change the signs on the right hand side, change the direction of the inequality back to <= as in D2.1.
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<tr>
<td>Cl 85 SC 85.3</td>
<td>TR</td>
<td>X</td>
<td>The response to D2.1 comment 37 (Exchange of DME frames is unnecessary) shows a misunderstanding by the BRC. Response says &quot;include backward compatability with CX4&quot;. CX4 doesn't use and can't understand DME frames, so compatability with CX4 is achieved by Parallel Detection. Response says &quot;Suggested remedy inconsistent with ... 802.3ap electricals&quot;: this isn't about electricals but about a protocol. DME frames are used in Backplane Ethemet where there is a choice of DME-aware PMD types. On a front-side port, there isn't. There is 10GBASE-CX4 and 40GBASE-CR4. You don't need DME frames to tell them apart. You have Parallel Detection to detect CX4. So you can use it to detect CR4 also. The unnecessary burden, apart from the obvious extra complexity of an unnecessary protocol, is that DME frames run at 312.5 Mb/s, 1/33 of the normal 10G rate, so a normal 10G CDR won't lock to this.</td>
<td>Add text in Clause 85 saying that 40GBASE-CR4 and 100GBASE-CR10 can use Parallel Detection. This is in line with the backward compatability with CX4 and baseline &quot;Parallel detection function to detect legacy 10GBASE-CX4 PHYs&quot;. If you wish, advertise FEC ability in the Training frame.</td>
<td>O</td>
</tr>
<tr>
<td>Cl 83A SC 83A.2</td>
<td>TR</td>
<td>X</td>
<td>Following up D2.1 comment 159, According to 83.3, a PMA has TX and RX directions, each of which has an input and an output. nAUI is intended to connect PMAs, e.g. one in the host and one in a module. Therefore nAUI must connect a (host) TX (transmitter) output to a (module) transmitter input, and a (module) RX (receiver) output to a (host) receiver input. 83B and 86A use the terms host output, module input, module output, host input, which is compatible with 83. But Figure 83A-2 shows two &quot;Transmitter&quot;s and two &quot;Receiver&quot;s, one for each direction. This isn't compatible terminology.</td>
<td>Change &quot;Transmitter&quot; to &quot;output&quot; or &quot;driver&quot; or &quot;driver output&quot; as appropriate, &quot;Transmit Compliance Point&quot; to &quot;output compliance point&quot;, &quot;Receiver&quot; to &quot;input&quot;, and &quot;Receive Compliance Points&quot; and &quot;Receive Compliance Point&quot; to &quot;output compliance point&quot;, throughout 83A.</td>
<td>O</td>
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Comment ID #82

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<tr>
<td>Cl 83A SC 83A.2.1</td>
<td>TR</td>
<td>X</td>
<td>SDD21 does not represent loss, it represents forward gain (&quot;through response&quot; or just &quot;response&quot;; 47.4.1 calls it &quot;transmission magnitude response&quot;). For modules, we should stay with S-parameters, as is common industry practice in SFP+, CXP, XAUI (Clause 47) and so on, but the names need cleaning up. SuggestedRemedy Change &quot;differential insertion loss&quot; to &quot;differential response&quot;. Change &quot;less than&quot; to &quot;more than or equal to&quot;. Reverse the signs and the inequality in equation 83A-1 and Figure 83A-3.</td>
<td>Add text in Clause 85 saying that 40GBASE-CR4 and 100GBASE-CR10 can use Parallel Detection. This is in line with the backward compatability with CX4 and baseline &quot;Parallel detection function to detect legacy 10GBASE-CX4 PHYs&quot;. If you wish, advertise FEC ability in the Training frame.</td>
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Comment ID #83

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<td>Cl 83A SC 83A.3.3.1</td>
<td>TR</td>
<td>X</td>
<td>We don't need to argue about de- versus pre-: just change &quot;De-emphasis&quot; to &quot;Emphasis&quot;, and &quot;Vtx-demph&quot; (or &quot;Vth-demph&quot;) to &quot;VMA&quot;, throughout.</td>
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**Comment Type:** TR/technical required  
**Comment Status:** X

**Proposed Response**  
This is a defensive comment. Whatever you do, don’t mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

**Suggested Remedy**  
Delete unused specs from Table 85-8

**Comment Type:** T/technical

**Comment Status:** X

**Proposed Response**  
[Editor’s Note: Commenter did not indicate comment type, assigned Comment Type: T, since the commenter is not part of the P802.3ba ballot group]

**Proposed Response**  
This is a defensive comment. Whatever you do, don’t mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

**Suggested Remedy**  
Delete unused specs from Table 85-8

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**  
Make indicated change

**Type:** TR/technical required  
**Comment Status:** X

**Proposed Response**

**Comment Type:** T/technical  
**Comment Status:** X

**Proposed Response**  
This is a defensive comment. Whatever you do, don’t mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

**Suggested Remedy**  
Delete unused specs from Table 85-8

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**  
This is a defensive comment. Whatever you do, don’t mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

**Suggested Remedy**  
Delete unused specs from Table 85-8

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**

**Comment Type:** E/editorial

**Comment Status:** X

**Proposed Response**
Comment Type  T  Comment Status  X
pulse amplitude out Tx at TP2 is defined but DC gain is not. This could allow slow, high amplitude Tx, which is hard to equalize, to pass.

Suggested Remedy
Specify Tx DC amplitude of Tx as "sum of linear fit pulse from step 3 divided by M from step 3" specify that DC amplitude is greater than 0.375 and less than 0.6 and that the peak of the linear fit pulse from step 3 shall be greater than 0.60*DC amplitude

Proposed Response
Response Status  O

Comment Type  T  Comment Status  X
Receiver interference tolerance test is incomplete.

Suggested Remedy
Proposed wording will be presented a meeting

Proposed Response
Response Status  O

Comment Type  ER  Comment Status  X
The sentence does not read well "The far-end transmitter output noise is noise in .."

Suggested Remedy
Suggested "The far-end transmitter output noise is the summ of this noise in .."

Proposed Response
Response Status  O

Comment Type  T  Comment Status  X
Column heading state maximum skew but the values have approximate symbol~

Suggested Remedy
Please replace~with max value of skew variation

Proposed Response
Response Status  W
[Editor's note: Please do not use special character "tilde" or approximate symbol in comments since this is used as delimiter by the comment tool]
Draft 2.2 Comments

IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

WG 2nd recirculation ballot

Proposed Response

Cl 86A SC 86A.4.2 P 430 L 14 # 96
Ghiasi, Ali
Broadcom
Comment Type TR Comment Status X
With current set of specifications the SerDes transmitter may have very large amount of de-emphasis 3-5 dB resulting in significant distortion at TP1a and also see comment 216/218 on D2.1
SuggestedRemedy
The options here are either limit max DDJ to about 0.125 or max 3 dB de-emphasis, see ghiasi_03_0909

Cl 85 SC 85A.4.2 P 249 L 40 # 97
Ghiasi, Ali
Broadcom
Comment Type TR Comment Status X

Cl 85 SC 85A.5 P 423 L 9 # 97
Ghiasi, Ali
Broadcom
Comment Type TR Comment Status X
ILmated could have as low as 2 dB loss and as high as 2.8 dB which could result cabling having higher loss
SuggestedRemedy
Add note the cable loss of 24.44 dB is when ILmated loss is 2.4 dB, if ILmated loss is less than 2.4 dB then ILch shall be reduced by the same amount

Cl 85 SC 85.8.3.1 P 249 L 31 # 98
Ghiasi, Ali
Broadcom
Comment Type TR Comment Status X
No test method is defined how to measure "Total Jitter Excluding Data Dependent Jitter"
SuggestedRemedy
A suggested method is given below:
Total Jitter is measured with PRBS31 (pattern 3) at BER of 10-12. Data Dependent jitter is measured with PRBS9 based on method given in 85.8.3 with following definition
Ddj=max(dt1, dt2,.....dt256) - min(dt1, dt2,.....dt256).
Section 85.8.3 would need to be updated or the other option is to create a standalone section.

Cl 85 SC 85.8.3.1 P 249 L 31 # 98
Ghiasi, Ali
Broadcom

Cl 85 SC 85.8.3.4 P 255 L 35 # 100
Ghiasi, Ali
Broadcom
Comment Type TR Comment Status X
It would more readable if Fig 85-4 is plotted with linear scale and similar to Fig 86A-12
SuggestedRemedy
Please follow or copy Fig 86A-12

Cl 85 SC 85.8.3.4 P 255 L 35 # 101
Ghiasi, Ali
Broadcom
Comment Type TR Comment Status X
Figure is missing min loss
SuggestedRemedy
Please add min loss and follow or copy Fig 86A-12

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**TYPE:** TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general

**COMMENT STATUS:** D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn

**SORT ORDER:** Comment ID

**Page 22 of 47**  9/4/2009  6:10:22 PM
The cable assembly test fixture is not consistent with Eq 86A-5. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

Suggested Remedy
Please use Eq 86A-5

Comment Type TR
Comment Status X

Proposed Response Response Status O

The channel loss budget has been changed during D2.1 but this equation was not adjusted accordingly

Suggested Remedy
Mated response loss 6.5 dB at 5.16 GHz, less 1.25 dB for HCB, less 0.5 dB for connector, leaves 4.75 dB loss per end.
The 4.75 dB host PCB loss is based on assumption the connector has loss of 0.5 dB, higher loss connector require reducing channel PCB loss.

Proposed Response Response Status O

The cable assembly test fixture is not consistent with Eq 86A-4. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

Suggested Remedy
Please use Eq 86A-4

Proposed Response Response Status O
Cl 86A SC 86A.5.1.1.2 P 436 L 32 # 114
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
Mated test fixture crosstalk loss in current draft are place holder and some of the limit specially PSFXT will impact the measurements accuracy
Suggested Remedy
For the new limits please see ghiasi_01_0909

Proposed Response Response Status O

Cl 85 SC 85.11.1.1 P 272 L 34 # 115
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
Connector IEC number is missing
Suggested Remedy
Please add connector IEC number, if not available then use the SFF number

Proposed Response Response Status O

Cl 85 SC 85.11.1.1 P 274 L 10 # 116
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
Contact 27 is not listed in table 85-11
Suggested Remedy
Please add all 38 contacts to table 85-11

Proposed Response Response Status O

Cl 85 SC 85.11.3 P 277 L 10 # 117
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
Some of the contacts shown in the MDI diagram are not listed in table 85-11
Suggested Remedy
Please include all contacts

Proposed Response Response Status O
Cl 88 SC 88.5.1 P 346 L 12 # 121
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
Fig 88-2 as drawn indicate and optical retimer!

Suggested Remedy
Please move L0-L3 before and after optical mux.

Proposed Response Response Status O

Cl 88 SC 88.5.1 P 346 L 12 # 122
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
The L0-L3 is not connected to any instantiation logical or Physical

Suggested Remedy
Please update figure to show gearbox and CAUI

Proposed Response Response Status O

Cl 83A SC 88.5.2 P 395 L 37 # 123
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
FR4 trace stress not clear what it is

Suggested Remedy
Suggest either use Frequency Dependnet Attenuator or PCB Trace

Proposed Response Response Status O

Cl 87 SC 88.5.3 P 316 L 12 # 124
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
The L0-L3 is not connected to any instantiation logical or Physical

Suggested Remedy
Please update figure to show XLAUI retimer

Proposed Response Response Status O

Cl 87 SC 88.5.3 P 317 L 12 # 125
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
Fig 87-2 as drawn indicate and optical retimer!

Suggested Remedy
Please move L0-L3 before and after optical mux.

Proposed Response Response Status O

Cl 88 SC 88.8.5.3 P 356 L 12 # 126
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
The CRU BW for the TDP measurement is defined to be 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Suggested Remedy
Propose to consider CRU BW 7.5 MHz instead of current 10 MHz, see ghiasi_02_0909

Proposed Response Response Status O

Cl 88 SC 88.8.5.3 P 356 L 12 # 127
Ghiasi, Ali Broadcom

Comment Type TR Comment Status X
The CRU BW for the TDP measurement is defined to be 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Suggested Remedy
Propose to consider CRU BW 7 MHz instead of current 10 MHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

Proposed Response Response Status O
Comment Type: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn
SORT ORDER: Comment ID

Cl 88  SC 88.8.5.3  P 356  L 12  # 128
Ghiasi, Ali  Broadcom

Comment Type: TR  Comment Status: X
Transmitter eye diagram is measured CRU BW of 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Suggested Remedy
Propose to consider CRU BW 7 MHz instead of current 10 MHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

Proposed Response  Response Status: O

Cl 88  SC 88.8.10  P 357  L 21  # 129
Ghiasi, Ali  Broadcom

Comment Type: TR  Comment Status: X
Stress receiver sensitivity has corner frequency of 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Suggested Remedy
Propose to consider corner frequency of 7 MHz instead of current 10 MHz and change 100 KHz to 70 KHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

Proposed Response  Response Status: O

Cl 85  SC 85.2  P 241  L 9  # 132
DiMinico, Christopher  MC Communications

Comment Type: E  Comment Status: X
Spelling interpret

Suggested Remedy
Change interpret to interpret

Proposed Response  Response Status: O

Cl 85  SC 85.11.1.2  P 274  L 36  # 133
DiMinico, Christopher  MC Communications

Comment Type: E  Comment Status: X
Spelling compatibility

Suggested Remedy
Change compatibility to compatibility.

Proposed Response  Response Status: O

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn
SORT ORDER: Comment ID

Comment ID # 133  Page 26 of 47  9/4/2009  6:10:22 PM
<table>
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<th>SC</th>
<th>P</th>
<th>L</th>
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<th>Comment Status</th>
<th>Suggested Remedy</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
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<tr>
<td>134</td>
<td>85</td>
<td>85.11.2</td>
<td>275</td>
<td>41</td>
<td>E</td>
<td>X</td>
<td>Change assignments to assignments</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>135</td>
<td>85A</td>
<td>85A.2</td>
<td>421</td>
<td>11</td>
<td>E</td>
<td>X</td>
<td>Change voltage to voltage</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>136</td>
<td>85A</td>
<td>85A.4</td>
<td>422</td>
<td>27</td>
<td>E</td>
<td>X</td>
<td>Change transmitter to transmitter</td>
<td></td>
<td>O</td>
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<td>85A</td>
<td>85A.4</td>
<td>422</td>
<td>43</td>
<td>E</td>
<td>X</td>
<td>Change insertion to insertion</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>138</td>
<td>85</td>
<td>85.8.3.5</td>
<td>256</td>
<td>1</td>
<td>E</td>
<td>X</td>
<td>Provide consistency with test fixture representation and labeling in Figure 85–5 with 85.10.10 Mated test fixtures Figure 85–11.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>139</td>
<td>85</td>
<td>85.8.4.2</td>
<td>258</td>
<td>21</td>
<td>T</td>
<td>X</td>
<td>Comment #138 against Draft 2.1 was incorrectly implemented; a4 for test 1 values should be a4 = 0.03. See response to comment #138 Draft 2.1 - (2) Limits given by polynomial coefficients (low loss a1=2.15,a2=.78,a4=.03) (high loss a1=6.04,a2=0.94,a4=0.08).</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>140</td>
<td>85</td>
<td>85.10.10.1</td>
<td>268</td>
<td>40</td>
<td>T</td>
<td>X</td>
<td>Rather than using minimum insertion loss [equation 85–36] and a maximum insertion loss [equation 85–37] to specify the mated test fixtures insertion loss in 85.10.10.1, I suggest we use a fit to the mated test fixtures and an ILD to address the IL deviations from the fit. This is consistent with 85.8.4.3.1 Test channel insertion loss and 85.10.2 Cable assembly insertion loss 85.10.1.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>141</td>
<td>85</td>
<td>85.10.10.1</td>
<td>268</td>
<td>43</td>
<td>E</td>
<td>X</td>
<td>Provide consistent labeling in Figure 85–5 with 85.10.10 Mated test fixtures Figure 85–11.</td>
<td></td>
<td>O</td>
</tr>
</tbody>
</table>

**Proposed Response**

DiMinico, Christopher
MC Communications
1. Comment on Clause 52:

   **Comment Type:** E  
   **Comment Status:** X  
   There is a wrap around error in the listing for Clause 52.

   **Suggested Remedy:** Fix wrap-around error for Clause 52 entry.

   **Proposed Response**

2. Comment on Clause 83.5.2:

   **Comment Type:** ER  
   **Comment Status:** X  
   There is some concern regarding the use of the term mapping and how it relates to what is illustrated in Fig 83-6. The use of the word “mapping” seems to address how input lanes are directed to output lanes, but in the commenter's opinion does not do an adequate job addressing the sequencing of bits on the output lanes, which may lead to interpretation issues.

   **Suggested Remedy:** Further clarifying text is needed. See presentation by D'Ambrosia.

   **Proposed Response**

3. Comment on Clause 74.5:

   **Comment Type:** ER  
   **Comment Status:** X  
   IEEE P802.3az is making changes Clause 74 IEEE Std 802.3-2008. These changes are specific to 10GBASE-R PHYs. IEEE P802.3ba has changed Clause 74 to address 10GBASE-R and 40/100GBASE-R PHYs. Therefore, coordination between the two projects is needed to manage the changes in that project to only the 10GBASE-R PHY section.

   **Suggested Remedy:** Coordinate modifications of Clause 74 with IEEE P802.3az editorial team.

   **Proposed Response**

4. Comment on Clause 85.10.6:

   **Comment Type:** E  
   **Comment Status:** X  
   Unnecessary left parenthesis at end of sub-clause heading.

   **Suggested Remedy:** Delete parenthesis at end of 85.10.6

   **Proposed Response**

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**Sorting Order:** Comment ID
Draft 2.2 Comments

IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

WG 2nd recirculation ballot

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**Cl 86 SC 86.8.4.6.1 P 300 L 24 # 145**

D'Ambrosia, John

Force10 Networks

- **Comment Type:** E
- **Comment Status:** X

**Comment:** looks like spacing error between text on lines 24/25 and Fig 86-4

**Suggested Remedy:**

fix.

**Proposed Response:**

Response Status O

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**Cl 81 SC 81.1 P 144 L 3 # 149**

D'Ambrosia, John

Force10 Networks

- **Comment Type:** E
- **Comment Status:** X

**Comment:** The use of the term "scalable" could be misconstrued. There are two distinct interfaces - one that supports 40Gb/s and another that supports 100 Gb/s

**Suggested Remedy:**

Change

a) It is scalable and capable of supporting speeds of 40 Gb/s and 100 Gb/s.
b) Data and delimiters are synchronous to a clock reference.
c) It provides independent 64-bit-wide transmit and receive data paths.
d) It provides for full duplex operation only.

to

a) The XLGMII interface supports speeds of 40 Gb/s.
b) The CGMII interface supports speeds of 100 Gb/s.
c) Data and delimiters are synchronous to a clock reference.
d) It provides independent 64-bit-wide transmit and receive data paths.
e) It provides for full duplex operation only.

**Proposed Response:**

Response Status O

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**Cl 85 SC 85.10.8 P 267 L 1 # 147**

D'Ambrosia, John

Force10 Networks

- **Comment Type:** E
- **Comment Status:** X

**Comment:**

Other figures in the draft have shown where the pass region is in relation to a stated curve

**Suggested Remedy:**

add text "Pass Region" to region below the curve.

**Proposed Response:**

Response Status O

---

**Cl 00 SC 0 P L # 150**

D'Ambrosia, John

Force10 Networks

- **Comment Type:** ER
- **Comment Status:** X

**Comment:** Several illustrations of MDI Connectors have provided greater detail than is necessary for illustration. Readers of the draft are provided with the reference document numbers for normative details regarding the connector.

**Suggested Remedy:**

Simplified illustrative drawings to be provided.

**Proposed Response:**

Response Status O

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**Cl 83A SC P L # 151**

D'Ambrosia, John

Force10 Networks

- **Comment Type:** TR
- **Comment Status:** X

**Comment:** A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.

**Suggested Remedy:**

Change 83A-1 to

\[ |SDD21| \leq -0.00086 + (0.2286 \times f^{1/2}) + (0.08386 \times f) \]

Change 83A-2 to

\[ |SDD21| \leq -0.00086 + (0.2286 \times f^{1/2}) + (0.08386 \times f) \]

**Proposed Response:**

Response Status O

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*TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general*

*COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn*

*SORT ORDER: Comment ID*
Cl 83A SC P L # 152
D’Ambrosia, John Force10 Networks

Comment Type TR Comment Status X
A number of equations related to return loss / Symm have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers. For Return Loss constraints the requirement should be "greater than or equal to" the equation

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.


Suggested Remedy
For noted equations change sign from "less than or equal to" to "greater than or equal to"

Proposed Response Response Status O

Cl 83B SC P L # 154
D’Ambrosia, John Force10 Networks

Comment Type TR Comment Status X
A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83B-1, 83B-2, 83B-3, and 83B-4.

Suggested Remedy
Change 83B-1 and 83B-2 to
\[ |SDD21| \leq 0.111 + (1.046 \times f^{(1/2)}) + (1.05 \times f) \quad 0.25 \leq f \leq 7 \]
\[ |SDD21| \leq -11.95 + (3.15 \times f) \quad 7 \leq f \leq 11.1 \]

Change 83B-3 to
\[ |SDD21| \leq 0.04 + (0.33 \times f^{(1/2)}) + (0.32 \times f) \quad 0.25 \leq f \leq 7 \]
\[ |SDD21| \leq -3.72 + f \quad 7 \leq f \leq 11.1 \]

Change 83B-4 to
\[ |SDD21| \leq -0.00086 + (0.2286 \times f^{(1/2)}) + (0.08386 \times f) \]

Proposed Response Response Status O
A number of equations related to return loss / $S_{xym}$ have been arranged where the absolute magnitude of the $s$-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers.

The equations all result in negative numbers.

For Return Loss constraints the requirement should be "greater than or equal to" the equation.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83B-5, 83B-6, 83B-8, and 83B-9.

**Suggested Remedy**

Change Eqs 83B-5, 83B-9 to:

$$|S_{DD11}| \geq 12 - (2 \cdot f) \text{ for } 0.01 \leq f \leq 2.19$$

$$5.56 - (8.76 \cdot \log_{10} (f/5.5)) \text{ for } 2.19 \leq f \leq 11.1$$

Change Eqs 83B-6, 83B-8 to:

$$|S_{DD22}| \geq 12 - (2 \cdot f) \text{ for } 0.01 \leq f \leq 2.19$$

$$5.56 - (8.76 \cdot \log_{10} (f/5.5)) \text{ for } 2.19 \leq f \leq 11.1$$

For noted equations change sign from "less than or equal to" to "greater than or equal to".

---

**Comment ID #153**

D'Ambrosia, John

Texas Instruments

**Comment Type** TR

**Comment Status** X

The English is strange. "...can have a minimum value .... due to ......requirements".

**Suggested Remedy**

Option 1 Replace "can" with "may"

Option 2 Replace "clock tolerance and lane alignment requirements" with "clock and lane alignment allowed variations"

Do the same in Annex 4A page 369 line 24

---

**Comment ID #154**

Dudek, Mike

QLogic

**Comment Type** T

**Comment Status** X

This paragraph (85.7.1) says that TP2 is at the output end of the mated connector and defines this as TP2. Table 85-4 says that the specifications are at TP2, but 85.8.3.5 says that the measurements are at the output of the test fixture.

**Suggested Remedy**

Change "The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2." to "The electrical transmit signal is defined at TP2 the output of the test fixture described in 85.8.3.5 mated to the connector in place of the cable. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2."

In Figure 85-5 Show the connector and PCB traces to the left of TP2 or TP3. To clarify things make the Test fixture impedance 85.8.3.6 and Test fixture insertion loss 85.8.3.7 sub-sections of 85.8.3.5.
Clip 85 SC 85.8.3.2 P 250 L 29 # 159
Dudek, Mike QLogic

**Comment Type**: TR **Comment Status**: X
The transmitter noise will add to the ICN in an RMS fashion, not a linear fashion.

**SuggestedRemedy**
Change Equation 85-2 and 85-3 to use RMS addition (sqrt(a^2 + b^2)) not linear (a + b)

**Proposed Response**
Response Status O

Clip 85 SC 85.8.3.3.4 P 253 L 42 # 160
Dudek, Mike QLogic

**Comment Type**: T **Comment Status**: X
Wrong reference (85.7.3.2.3 doesn't exist.)

**SuggestedRemedy**
Change 85.7.3.2.3 to 85.8.3.3.3

**Proposed Response**
Response Status O

Clip 85 SC 85.8.4.3.1 P 258 L 50 # 161
Dudek, Mike QLogic

**Comment Type**: TR **Comment Status**: X
The test cables attenuation for the interference tolerance test should have a specified value (not just a max value).

**SuggestedRemedy**
Delete the words "maximum allowable".

**Proposed Response**
Response Status O
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Document Section</th>
<th>Comment ID</th>
<th>Document Section</th>
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<tr>
<td>164</td>
<td>SC 85.10</td>
<td>165</td>
<td>SC 85.10.2</td>
</tr>
<tr>
<td>167</td>
<td>SC 85.10.9</td>
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</tbody>
</table>

### Comment 164

**Comment Type:** TR  
**Comment Status:** X

The parameters in Table 85-8 do not adequately specify the cable as there are no insertion loss or insertion loss deviation specifications at frequencies other than 5.15625GHz. Resonances can occur that meet the specification at this one frequency but cause problems at other frequencies. Also the return loss specification is too relaxed.

**Suggested Remedy:**

Change the parameter for the first row of table 85-8 to "Maximum fitted insertion loss at 5.15625 GHz". For insertion loss deviation delete "at 5.15625GHz" and change the value to "see 85.10.3". Delete at 5.15625 GHz from the return loss specification and change the specification to "see equation 85-1", or "see 85.10.4".

**Proposed Response:**

Response Status: O

### Comment 165

**Comment Type:** T  
**Comment Status:** X

Due to the restrictions on a1, a2 and a4, caused by the maximum insertion loss at 5.125625GHz the curve in Figure 85-6 is only one example and doesn't show the maximum insertion loss at any specific frequency. Also the reference to Figure 85-6 is duplicated on page 262 line 5.

**Suggested Remedy:**

Change the sentence from "The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and the maximum allowed values of a1, a2, and a4 is illustrated in Figure 85-6." to "The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and one example of the maximum allowed values of a1, a2, and a4 is illustrated in Figure 85-6."

Delete the duplicate sentence on page 262 line 5.

**Proposed Response:**

Response Status: O

### Comment 167

**Comment Type:** TR  
**Comment Status:** X

Results will vary depending on the fixture insertion loss. We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A. It would also be good to specify exactly what is included in the Test fixture loss. Also the test fixture loss is not matching what was used to derive the link budget (The link budget was derived in Healey_03a_0709 has the same PCB test fixture loss as clause 86A). We should make sure that the test fixture loss is the same as in clause 86A.

**Suggested Remedy:**

Change "The maximum test fixture insertion loss shall meet the values determined using Equation (85–35). The values for the coefficients b1 , b2, b3, b4 and e are given in Equation (85–16)” to "The reference test fixture insertion loss shall meet the values determined using Equation (85–35).

Make Equation 85-35 match the loss of the MCB in 86A. Also add a sentence at the end of the end of 85.10.9 "The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements." Also state whether the connector loss is included in the test fixture loss or not.

**Proposed Response:**

Response Status: O
Cl 85A SC 85A.4 P 422 L 46 # 168
Dudek, Mike QLogic
Comment Type T Comment Status X
maximum used where it should be minimum
SuggestedRemedy change maximum to minimum
Proposed Response Response Status O

Cl 85A SC 85A.4 P 422 L 16 # 169
Dudek, Mike QLogic
Comment Type T Comment Status X
It would help understanding if IL(Camax) were better defined.
SuggestedRemedy Change IL(Camax) definition to "The maximum cable assembly insertion loss as measured with the cable assembly test fixtures using Equation (85-19)"
Proposed Response Response Status O

Cl 85A SC 85A.5 P 423 L 19 # 170
Dudek, Mike QLogic
Comment Type T Comment Status X
Assuming my other comments are accepted to change to a reference loss for the test fixtures. The IL(mated) definition should be changed from maximum insertion loss to reference insertion loss
SuggestedRemedy Change the definition of IL(mated) to "The reference insertion loss of the mated test fixture using equation (85-37)"
Proposed Response Response Status O

Cl 85A SC 85A.5 P 423 L 21 # 171
Dudek, Mike QLogic
Comment Type T Comment Status X
ILChax(f) is a single named variable but it has been given two different curves. (equations 85A-3 and 85A-4) which is bad practice. In any case the maximum channel loss at 0.5m is not a very interesting characteristic.
SuggestedRemedy Delete the text between lines 21 and 35. As an alternative that would perhaps have more interest consider changing this section to minimum channel loss.
Proposed Response Response Status O

Cl 85A SC 85A.5 P 423 L 20 # 172
Dudek, Mike QLogic
Comment Type T Comment Status X
It would be very helpful to better define the test points and the losses and show where equation 85A-3 comes from
SuggestedRemedy Insert at line 20. “The losses are shown diagnostically in NEW FIG”
Use slide 14 from Healey_03a_0709 as the basis of NEW FIG. Title the figure as “Illustration of loss budget” Labelling TP1 to TP4 as “IL(camax) (17.04dB)” TP0 to TP2 and TP3 to TP5 as “IL(host)(3.25dB)” and label the mated test fixture loss as “ILMatedTF (2.8dB)”
Proposed Response Response Status O

Cl 85 SC 85.8.4.3.1 P 258 L 43 # 173
Dudek, Mike QLogic
Comment Type T Comment Status X
The units are wrong
SuggestedRemedy It should state “Where f is the frequency in GHz.”
Proposed Response Response Status O
Cl 85 SC 85.10.2 P 261 L 12 # 174
Dudek, Mike QLogic

Comment Type T Comment Status X
The units are wrong
Suggested Remedy
Change to "Where f is the frequency in GHz."
Proposed Response Response Status O

Cl 85 SC 85.8.3.6 P 256 L 38 # 175
Dudek, Mike QLogic

Comment Type ER Comment Status X
There are multiple equations and graphs in the clause that are functions of frequency. Most use GHz, some use MHz, Hz also occurs. It would be good to standardize them all. This specific instance obviously applies to line 42 as well. Other instances are this page lines 48 and 49 with page 257 lines 1 to 6 and related change on page 267 lines 33 and 38, and related changes in 85a page 422 line 40 and page 423 line 1 Page 262 lines 44 to 52 Figure 85-7
Suggested Remedy
Change all the equations and graphs covering the GHz range to use GHz as listed in the comment(no technical change.) Also do the same in Annex 85a (page 423 lines 30 and 53), (page 424 lines 43 and 46 and fig 85a-1)
Proposed Response Response Status O

Cl 86A SC 86A.5.1.1.1 P 431 L 39 # 176
Dudek, Mike QLogic

Comment Type T Comment Status X
The MCB SDD21 is expected to be approximately half the loss of the HCB, but the frequency independent term ratio is far larger.
Suggested Remedy
Change MCB frequency independent term from -0.0006 to -0.006
Proposed Response Response Status O

Cl 85 SC 85.8.3.7 P 256 L 46 # 177
Dudek, Mike QLogic

Comment Type TR Comment Status X
Results will vary depending on the fixture insertion loss and 85.8.3.7 gives a maximum test fixture insertion loss (and no minimum). We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86a for commonality. Note that the PCB loss of the test fixture of clause 86a is what was used to derive the budget in Healey_03a_0709 (which doesn't match what is here). We should also specify exactly what is included in the insertion loss.
Suggested Remedy
Change the Test Fixture insertion loss to a reference insertion loss (not just max) and use the same equations as 86a. Also add a sentence at the end of the Test Fixture insertion loss "The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements."
State in 85.8.3.6.7 that the connector loss is not included in the test fixture insertion loss.
Proposed Response Response Status O

Cl 85 SC 85.8.4.3.1 P 258 L 38 # 178
Dudek, Mike QLogic

Comment Type TR Comment Status X
We should state specifically where the test channel insertion loss is measured.
Suggested Remedy
Change "The fitted test channel 1 or test channel 2 insertion loss ILTC(f)...") to "The fitted test channel 1 or test channel 2 insertion loss between the pattern generator and the output of the test fixture described in 85.10.9 ILTC(f)...")
Proposed Response Response Status O

Type: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
Comment Status: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
Sort Order: Comment ID

**Comment ID**: 180  
**Comment Type**: TR  
**Comment Status**: X  
**Comment**: The definition of TP1 has been adjusted (per Healey_03a_0709) to be at the input to the cable test fixture so it does not include all the PCB, resulting in an ambiguity. The loss specified on line 33 matches the loss we have in the budget for TP0 to TP1 (not for the complete PCB) but does not match the loss in equation 85A-1 which is only 5.18dB at Nyquist. Also Clause 86A allows a max 2x4.4dB for the total PCB loss on the assumption a host might use a lower loss connector.

**Suggested Remedy**: Either  
1. Delete "(ie the maximum insertion loss between TP0-TP1 and TP4-TP5)." and change the multiplier in equation 85A-1 from 0.3 to 0.508.  
2. Change the paragraph to "The maximum insertion loss allocation for the transmitter plus receiver differential controlled impedance printed circuit boards for each differential lane between TP0-TP1 and TP4-TP5 is determined using Equation (85A-1) and the coefficients b1 through b4 are given in Equation (85-16)." The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards between these test points is 7 dB at 5.15625 GHz. Note that there is an additional 1.4dB allowance in the PCB loss for the equivalent PCB loss between TP1 and TP4 and the connectors."  
   Change the multiplier in equation 85A-1 from 0.3 to 0.405

**Response Status**: O

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**Comment ID**: 181  
**Comment Type**: TR  
**Comment Status**: X  
**Comment**: The minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The HCB PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.

**Suggested Remedy**: Add a row to the equation

1. \(0.01 < f < 1\) value 0
2. Change the existing first row to \(+0.5 - 0.5f\)

Consider also increasing the minimum loss at Nyquist by approx 0.5dB by changing this existing first row to \(0.6 - 0.6f\) and changing the second row to \(-3.7\)

**Response Status**: O
Comment Type  T  Comment Status  X

Table 83A-2 is actually a mixture of receiver characteristics (e.g., return losses) and specifications of the most degraded signal the receiver has to tolerate (e.g., total jitter). The receiver does not have a maximum total jitter tolerance. It’s characteristic is a minimum total jitter tolerance.

Suggested Remedy
Split table 83A-2 into two tables. Table A labelled "Receiver input tolerance requirements" with everything in the existing table except the return losses. Table B labelled "Receiver characteristics" with just the return loss lines.

The sentence on page 389 line 26 then becomes. "The receiver shall tolerate signals with the characteristics given in Table A. The receiver shall also have the characteristics given in Table B."

An alternative remedy keeping one table is changing the maximum values of the input signal into minimum input tolerances as done in table 86A-4.
In table 86-8, the attribute, "Receiver jitter tolerance signal level in OMA, each lane" is really a test condition and as such should be included with the other jitter tolerance test conditions.

**Suggested Remedy**

In table 86-8, move the attribute, "Receiver jitter tolerance signal level in OMA, each lane" so that it is included with the other jitter tolerance test conditions.

**Proposed Response**

Response Status: O

In table 86.8, unlike the case for Stressed receiver sensitivity which has an explicit entry for the attribute, there is no entry for a receiver tolerance attribute, only conditions for such. Further, there is no explicit link to the test definition in 86.8.4.8 which may compound the confusion of the missing test entry. Finally, since this is a test of the ability of a system to track low frequency jitter, it would be helpful to note (similar helpful information are included in footnotes a & c) that the test is not intended for subsystems where CDR and/or bit-error-detector functions is/are not included. See figure 86-14 which shows a System under test, SUT, comprising a PCS, PMA and PMD. Without the CDR and bit-error-detector of the PMA and/or PCS, equipment external to the SUT would be needed and the test would become, primarily, a test of this external equipment.

**Suggested Remedy**

In Table 86-8, insert an entry, "Receiver jitter tolerance in BER, each lane" above the "Conditions of receiver tolerance test". Append a footnote indicator at the end of the entry. In the Type column enter "Max". In the value column enter "10-12" and leave a blank in the units column. For the footnote, insert, "Measured with conformance test signal at TP3. See 86.8.4.8. This is test of the system receiver's ability to track low frequency jitter and is inappropriate for any subsystem that does not include CDR and/or bit-error-detector function(s)."

**Proposed Response**

Response Status: O

Clause 68.6.11 is referenced with exceptions. There is no exception declared for the requirement in 68.6.11, "The optical waveform is connected ... and mode-conditioning patch cord suitable for 62.5/125 um fiber". The "mode-conditioning patch cord suitable for 62.5/125 um fiber" does not seem necessary for SR and, if not, is an unnecessary burden. If such a mode-conditioning patch cord is required, then further definition of its characteristics and use are required.

**Suggested Remedy**

In 68.6.11 add another exception, fj, to the list that states, 'the mode-conditioning patch cord suitable for 62.5/125 um fiber is not used'.

**Proposed Response**

Response Status: O

In Table 86A-1 does not declare the units for the y-axis. While the units may be inferred from the associated equations, the y-axis title lists SDD11 and similar terms but the equations are '20 log (|...|) = ...', so there's not a one-to-one match. For consistency, if the '20 log (|...|) remains in the equation it should be in the axis title. Otherwise we appear to be saying that 20log10(|SDD11|) = SDD11. Further, while the units for the x-axis could also be inferred from the equations they are explicit in the x-axis title. Similar cases occur for figures 86A-2, 3, 4, 5 & 6.

**Suggested Remedy**

1. If the 20 log(|...|) terms remain in the reflection and response equations, then they should be included in the associated y-axis titles for figures 86A-1, 2, 3, 4, 5 & 6.
2. dB should be included as the y-axis units for figures 86A-1, 2, 3 & 4.

**Proposed Response**

Response Status: O
IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

WG 2nd recirculation ballot

Cl 86A SC 86A.1 P427 L 15 #192

Petrilla, John Avago Technologies

Comment Type E Comment Status X

In the overview it's said about PPI that, "It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside." As PPI can similarly support 40GBASE-LR4 modules, the overview should make that visible. Further PPI does not preclude use of CDRs within a module.

Suggested Remedy

Change from, "It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside." to "It allows the construction of compact optical transceiver modules for 40GBASE-SR4, 40GBASE-LR4 or 100GBASE-SR10 with no clock and data recovery circuits required inside."

Proposed Response Response Status O

Cl 86A SC 86A.4.2 P431 L 16 #193

Petrilla, John Avago Technologies

Comment Type ER Comment Status X

In Table 86A-4, unlike table 86-8, there is no explicit indication of a low frequency SJ jitter tolerance requirement, although there is much detail in the associated 86A.5.3.8, specifically the template in 86A.5.3.8.6. It doesn't seem good practice where a table of requirements is available not to indentify all significant attributes.

Suggested Remedy

In table 86A-4, add a row, 'Applied sinsuoidal jitter', for low frequency SJ to the receiver signal tolerance test conditions. Enter 'TP4' in the Test Point column, 'See 86A.5.3.8' in the Spec.values column, and leave the Units and Conditions columns blank.

Proposed Response Response Status O

Cl 86A SC 86A.4.2 P431 L 21 #195

Petrilla, John Avago Technologies

Comment Type TR Comment Status X

In Table 86A-4, the value for the Transition time value is shown as, "34 TBC". A predetermined transition time value may preclude generating a stressed signal that reaches all of the eye mask coordinates, J2, J9 and DDPWS simultaneously. Since there appears to be more value having an input signal that simultaneously stresses min and max signal levels, eye mask corners, J2, J9 and DDPWS, a transition time spec may be redundant.

Suggested Remedy

Delete the Transition time requirement from Table 86A-4 and in 86A.5.3.8.5 append to the end of the sentence, "The vertical eye opening and peak level specifications are verified." 'such that eye mask coordinates X1, X2, Y1, Y2, and jitter values DDPWS, J2, J9 are all simultaneously met.' In 86A.5.3.8.5 page 444, line 12, change the phrase, "... the amplitude and the transition time are as given in Table 86A-4.* to "... and the amplitude are as given in Table 86A-4.*

Proposed Response Response Status O
Proposed Response

Is the position of bit 1 in PRBS9 defined in 802.3? If so please cite a reference? If not delete, "These are bits 10 to 18 and 1 to 14, respectively." or create a definition for bit 1.

Suggested Remedy

Unless a definition that permits locating bit 1 exists, delete the sentence, "These are bits 10 to 18 and 1 to 14, respectively.". Otherwise cite the definition.

Proposed Response

The 'shall' in "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." seems more an instruction to the editors then to implementers.

Suggested Remedy

Change, "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." to "Host electrical receiver signal tolerance is defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." or if a shall statement is desired to "To be compliant a host electrical receiver signal tolerance shall satisfy the requirements defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6."

Proposed Response

The term LB in figure 86A-11 is not defined. Assuming it's the same LB as in 87 and 88, the definition in 88.8.10, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested." can be referenced or copied and pasted below figure 86A-11.

Suggested Remedy

Insert after figure 86A-11, the definition for LB, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

Proposed Response

The title for figure 86A-1 is, "Reflection specifications" but is more properly, 'Reflection specifications illustrations' as the specifications are in the associated table and equations. Even the text, see page 428, line 44 states, "the limit given in Equation 86A–2 and illustrated in Figure 86A–1." Similar issues exist with Figures 86A-2, 3, 4, 5 & 6.

Suggested Remedy

Change the title for figure 86A-1 from, "Reflection specifications", to 'Reflection specifications illustrations'. Do likewise for figures 86A-2, 3, 4, 5 & 6.

Proposed Response

If the XLAUI/CAUI Component & XLAUI/CAUI IC are the same use the same name. Likewise for Driver & Transmitter use Transmitter and for Input & Receiver use Receiver.

Proposed Response
Comment ID # 201

Pettrilla, John
Avago Technologies

**Comment Type** ER  **Comment Status** X

Requirements for TJ and DJ are found in a subclause titled, "Transmitter eye mask definition". This can make these definitions difficult to find and seems unnecessary as a subclause can easily be added for jitter definition.

**Suggested Remedy**

Create a subclause, ‘83A.3.3.6 Transmitter jitter definition’. Cut the sentence, "The measured jitter at the transmit compliance point shall be less than the maximum Total Jitter as defined in Table 83A-1, and are conducted with de-emphasis off.” and paste it into 83A.3.3.6 as the first sentence. From 83A.3.3.5 copy the sentence "Jitter and eye mask measurement requirements are described in 83A.5.1, and are conducted with de-emphasis off.” and paste it into 83A.3.3.6 deleting the words, ‘and eye mask’. Then in 83A.3.3.5, in the last sentence delete the words, ‘Jitter and’. Update the references in tables 83B-3 and 83B-5 to refer to 83A.3.3.6 for TJ and DJ.

**Proposed Response**  **Response Status** O

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Comment ID # 202

Pettrilla, John
Avago Technologies

**Comment Type** T  **Comment Status** X

In figure 83A-12 the template for SJ tolerance includes the region below 40 kHz while similar templates in clauses 87 and 86A do not. Clause 87 explicitly defines this region as not specified. These low freq jitter tolerance tests all have the same objective and there seems no reason for a difference in 83A.

**Suggested Remedy**

Redraw the template in 83A-12 to stop below 40 kHz. For reference, see figure 87-5 or 86A-11.

**Proposed Response**  **Response Status** O

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Comment ID # 203

Pettrilla, John
Avago Technologies

**Comment Type** ER  **Comment Status** X

In table 83B-2, compliance point terms TP1, TP1a and TP4 are used without definition or reference. If these are the same points as in clause 86 or 86A, then 86 should be cited. (Clause 85 also defines a TP1 and TP4 but no TP1a) If not, there should be a figure defining these points.

**Suggested Remedy**

If TP1, TP1a and TP4 are the same as in clause 86, add a note to table 83B-2 citing clause 86, figure 86-3, for the definition of these points.

**Proposed Response**  **Response Status** O

---

Comment ID # 204

Pettrilla, John
Avago Technologies

**Comment Type** E  **Comment Status** X

Table 83B-3 footnote a is redundant with the entry in the subclause column and can be deleted. This also occurs in Table 83B-5.

**Suggested Remedy**

In table 83B-3 and 83B-5, delete footnotes a.

**Proposed Response**  **Response Status** O

---

Comment ID # 205

Trowbridge, Stephen
Alcatel-Lucent

**Comment Type** E  **Comment Status** X

The optical interfaces listed in the table give their respective reaches while the electrical interfaces do not.

**Suggested Remedy**

For 40GBASE-KR4, add “with reach up to at least 1m”
For 40GBASE-CR4 and 100GBASE-KR4, add “with reach up to at least 7m”

**Proposed Response**  **Response Status** O
**Comment Type** E  **Comment Status** X
Run on sentence (too many "ands")

**Suggested Remedy**
Replace
"The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers and is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."

with
"The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers, is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."

**Comment Type** T  **Comment Status** X
The specification of which sequence ordered set values is reserved is not specified clearly. It appears that lane one or lane two can be anything (>=0x00) but that lane 3 must be >=0x03 for it to be a reserved value. But a value like 0x01 0x00, 0x00 in lanes 1-2-3 are probably also in the group that are considered to be reserved even though it doesn't meet the lane 3 inequality.

**Suggested Remedy**
Consider showing three rows for reserved:
lane 1 >=0x01, lane 2 >=0x00, lane 3>=0x00
lane 1>=0x00, lane 2 >=0x01, lane 3>=0x00
lane 1>=0x00, lane 2 >0x00, lane 3>=0x03 (the existing one)
Lane 3 can be 0x01 or 0x02 if lane 1 or lane 2 is >=0x01 and it is still reserved

**Comment Type** TR  **Comment Status** X
"If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive."

Suggest adding a reference to Figure 83-5 to make it clear in which direction the PRBS signal is being generated.

**Suggested Remedy**
Change sentence to read:
"If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)"
Proposed Response

I think the following sentence on line 51 is incorrect:

"The 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset."

This means the upper 14 bits in register 3.44 would immediately be cleared when software reads the lower 6 bits in register 3.33. This means that software would likely always read all zeros from register 3.44.

Suggested Remedy

I think the sentence should say:

"The lower 6 bits of the 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset and the upper 14 bits of the 20 counter shall be reset to all zeros when register 3.44 is read or upon PCS reset".

Also is the assumption that while the upper 14 bits of register 3.44 are in a latched state (due to a software read of the lower 6 bits in register 3.33) that errors continue to be accumulated in the background and are not simply ignored ? I guess what I am getting at here is if there is any time requirement or constraint between software reading 3.33 and subsequently reading 3.44 to ensure that no errors are missed ? For example if after reading 3.33 software has to read 3.44 before 3.33 overflows at a count of 2^6=64 errors, then this would place a constraint that software would have to read 3.44 no later than ~211us after reading 3.33 ... this seems fairly tight. Perhaps we need a note to clarify the behavior or expectations a little more clearly ?

Proposed Response

Response Status W

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

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Comment Type TR

Comment Status X

I think the following sentence on line 51 is incorrect:

"The 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset."

This means the upper 14 bits in register 3.44 would immediately be cleared when software reads the lower 6 bits in register 3.33. This means that software would likely always read all zeros from register 3.44.

Suggested Remedy

I think the sentence should say:

"The lower 6 bits of the 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset and the upper 14 bits of the 20 counter shall be reset to all zeros when register 3.44 is read or upon PCS reset".

Also is the assumption that while the upper 14 bits of register 3.44 are in a latched state (due to a software read of the lower 6 bits in register 3.33) that errors continue to be accumulated in the background and are not simply ignored ? I guess what I am getting at here is if there is any time requirement or constraint between software reading 3.33 and subsequently reading 3.44 to ensure that no errors are missed ? For example if after reading 3.33 software has to read 3.44 before 3.33 overflows at a count of 2^6=64 errors, then this would place a constraint that software would have to read 3.44 no later than ~211us after reading 3.33 ... this seems fairly tight. Perhaps we need a note to clarify the behavior or expectations a little more clearly ?

Proposed Response

Response Status W

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]
Comment Type: E  Comment Status: X

See the following note under Figure 83-5:

"inst PMD, PMA, or FEC, depending on which sublayer is below this PMA SIL Signal."

The parameter 'inst' appears to be there to address the fact that the sublayer below the PMA can be either a PMD, PMA or FEC.

No such convention appears to be adopted on the same figure for the interface above the PMA. In this case the service interface primitives are 'hard coded' with the name PMA, even though the sublayer above the PMA can be either a PMA, FEC or PCS.

Suggested Remedy

Suggest adopting a similar naming convention for the service interface primitives for the interface above the PMA (i.e. at the top of the figure), to reflect that the sublayer above the PMA can be either a PMA, FEC or PCS.

Response Status: O

Comment Type: E  Comment Status: X

Figure 82-2 does not show any indication of the PCS lane BIP error check (although it does show the BER monitor based on sync header errors)

Suggested Remedy

Update Figure 82-2 to show BIP error monitoring.

Response Status: O

Comment Type: E  Comment Status: X

I know what is meant, but I still find that the phrase "for each 8-bit BIP value in error" in the last sentence is not as clear as it could be.

Suggested Remedy

Suggest replacing the last sentence with:

"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented by one, each time the calculated BIP value does not exactly match the BIP value received in the BIP3 field (registers 3.90 through 3.99)."

Response Status: O

Comment Type: E  Comment Status: X

Text does not make it clear that as agreed to at the last meeting we changed from counting bit to block errors.

Suggested Remedy

Update text to reflect the fact that these counters are now counting block errors as described in section 82.2.14 and associated comment against the same section that I submitted this time against D2.2.

Response Status: O
### Table 45-65d.

The PRBS error counter is only sized at 12 bits. This means the counter will saturate at a count of $2^{12}$ or 4096 errors. Assuming the host is polling the counters at a rate of once per second, then the counter will saturate at an error rate of $1.6 \times 10^{-7}$ for a 25G lane rate. To facilitate optical waterfall curve testing it would be preferable for the counter not to saturate up to an error rate of $1 \times 10^{-4}$.

**Suggested Remedy**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

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**Comment ID # 218**

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<td>85.8.3</td>
<td>251</td>
<td>2531</td>
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**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

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**Comment ID # 219**

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**Proposed Response**

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**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

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**Comment ID # 220**

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</tbody>
</table>

**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

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**Comment ID # 221**

<table>
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</table>

**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.

**Proposed Response**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6 \times 10^{-6}$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1 \times 10^{-4}$.
Cl 85 SC 85.8.3 P 251 L 2531 # 221
Li, Mike Altera
Comment Type TR Comment Status X
"Total jitter excluding DDJ" is a confusing and self-inconsistent name. Total jitter is not "total" anymore if DDJ is removed.
Suggested Remedy
Change "Total jitter excluding DDJ" to uncorrelated total jitter (uTJ).
Proposed Response Response Status O

Cl 85 SC 85.8.3 P 251 L 2531 # 222
Li, Mike Altera
Comment Type TR Comment Status X
Amplitude pk-to-pk (line 19) and Far-end transmit output noise (line 22-23) are max values and are not specified
Suggested Remedy
Add (max) after those parameters.
Proposed Response Response Status O

Cl 83A SC 83A.3.3.2 P 386 L 42 # 223
Latchman, Ryan Gennum Corp
Comment Type T Comment Status X
"Rise/fall time is measured with de-emphasis off" should include a reference to 83A.5.1
Suggested Remedy
"Rise/fall time is measured with de-emphasis off as defined in 83A.5.1"
Proposed Response Response Status W
[Editor's Note: Late comment submitted after the close of the ballot; for consideration by the Task Force]
Palkert, Tom  Xilinx/Luxtera

Comment Type：TR  Comment Status：X

Cable assembly insertion loss is not consistent with 24.4dB total loss budget

Suggested Remedy

Change 17.04 to 11

Response Status：O