The recommended maximum loss for the PCB only (without connector) (Draft 2.2, page 446, row 51), should be aligned with formula 85A-2 (Transmitter and receiver differential printed circuit board trace loss) that gives maximum PCB loss @5.156GHz = 3.5dB (see page 4 of mazzini_01_0909).

SuggestedRemedy
Harmonize the loss.

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment 180

Also add a reference in clause 85 to the example in 86A and a reference in clause 86A to the example in 85, with editorial licence.

The CR4/10 Host IL (85-14) and the nPPI recommended electrical channel (86A-19) both defined with connector and test fixtures) should be IDENTICAL also for low frequencies (see page 4 of mazzini_01_0909).

SuggestedRemedy
Harmonize the curves as above.

Response
Response Status C
ACCEPT IN PRINCIPLE.

Change equation (85-14)
From:
0.114+0.8914 × sqrt(f)+0.846 × f 0.05 = f < 7
- 35.91 + 6.3291 × f 7 = f < 8
14.72 8 = f = 10

To:
0.682 0.05 <= f < 0.2
0.114+0.8914 × sqrt(f)+0.846 × f 0.2 <= f < 7
- 35.91 + 6.3291 × f 7 <= f < 8
14.72 8 <= f <= 10

The draft is not consistent in its use of parameter names and figures illustrating limit lines. For example "Return loss" and "Reflection response, SDD22" are used for the same parameter. See comment #327 against D 2.1

For a detailed discussion of this issue see dambrosia_01_0909.pdf

SuggestedRemedy
Apply changes as described in dambrosia_01_0909.pdf

Response
Response Status C
ACCEPT IN PRINCIPLE.

Apply changes as described in dambrosia_01_0909.pdf "Detailed changes" and "Proposal for consistency for graphs" slides with the exception of the "Indicate compliant region" bullet.

A vote of the task force on the above response was:
Yes 30
No 0

See also comment 85
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**Comment Type**: E  **Comment Status**: A

In the equations within the draft, the use of "x" to signify multiplication is inconsistent. According to the style manual, A multiplication sign "x" should only be used to indicate multiplication of two numbers (e.g., "1 x 10" or "3 cm x 4 cm"). Some equations do not use "x" e.g. "10 log" or "2f" and others use "10 x log" or "2 x f"

**Suggested Remedy**

- Note there is another comment against equation 85A-4

**Response**: ACCEPT.

Also see comment #54 regarding style

Some of the suggested equations may be modified by other comments.

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**Comment Type**: T  **Comment Status**: A

The draft is inconsistent on how it defines the frequency break points in equations. For some multi-segment limit lines, there is a small discontinuity at the break point, so it should be clear which limit applies to the exact break frequency.

**Suggested Remedy**

- In equations 85-39, 85-40, 85-41, 85-42 change "<10" to "<=10"
- In equation 86A-1, 86A-2, 86A-3, 86A-7, 86A-8, 86A-9, 86A-10, 86A-11, 86A-12, 86A-13, 86A-14, 86A-19, 86A-20 for all the frequency segments except the highest segment, change the second inequality from <= to < e.g. for equation 86A-8 change "0.01 <= f <= 2.5" to "0.01 <= f < 2.5" and change "2.5 <= f <= 5" to "2.5 <= f < 5"

**Response**: ACCEPT IN PRINCIPLE.

Change where appropriate to make the equations consistent across the draft as per suggested response.

---

**Comment Type**: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general

**COMMENT STATUS**: D/dispatched  A/accepted  R/rejected  **RESPONSE STATUS**: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn

**SORT ORDER**: Clause, Subclause, page, line

**Page 2 of 64**  9/24/2009  11:34:33 AM
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**Comment:**

The test fixture (85-16) and the HCB (86A-4) loss formulas must be IDENTICAL. In D2.2 losses just cross at same value @ 5.165GHz. (see page 5 of mazzini_01_0909).

**Suggested Remedy:**

Harmonize the loss.

**Response:**

ACCEPT IN PRINCIPLE.

Answer to comment #43

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**Comment:**

In relation to the presentation of equations in the draft, consult the IEEE style guide 17.3 for instructions on the use of italic and upright text in mathematical expressions.

**Suggested Remedy:**

Update equations to be consistent with the format prescribed by the style guide.

**Response:**

ACCEPT.

Editors will review this issue for their clauses in coordination with each other.

See related comment #13

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**Comment:**

The header is not consistent with respect to having a space between the number and unit. Starting on this page there is not space, but there should be a space.

**Suggested Remedy:**

Change: IEEE 802.3ba 40Gb/s and 100Gb/s Ethernet Task Force

To: IEEE 802.3ba 40Gb/s and 100Gb/s Ethernet Task Force

**Response:**

ACCEPT IN PRINCIPLE.

---

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**Comment:**

The English is strange. "...can have a minimum value ..... due to .....requirements".

**Suggested Remedy:**

Option 1 Replace "can" with "may"

Option 2 Replace "clock tolerance and lane alignment requirements" with "clock and lane alignment allowed variations"

Do the same in Annex 4A page 369 line 24

**Response:**

REJECT.

The existing sentence provides better clarity than the suggested remedy.

The use of "can have" is consistent with rest of the notes in 4.4.2 of base document.

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**Comment:**

Change 'that packaged' to 'that is packaged'

**Suggested Remedy:**

As above

**Response:**

ACCEPT.
The PRBS error counter is only sized at 12 bits. This means the counter will saturate at a count of $2^{12}$ or 4096 errors. Assuming the host is polling the counters at a rate of once per second, then the counter will saturate at an error rate of $1.6e-7$ for a 25G lane rate. To facilitate optical waterfall curve testing it would be preferable for the counter not to saturate up to an error rate of $1e-4$.

**Suggested Remedy**

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6e-6$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1e-4$.

**Response**

ACCEPT IN PRINCIPLE.

Change all PRBS error counters to 16 bits.

---

This section defines a 20 bit BER counter. It was my understanding that we agreed to increase the size of the BER counter to at least 24 bits as defined in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf.

Reading through the proposed implementation in this section I can understand the reluctance to increase the counter to the full 24 bits, as this would require assigning another full 16 bit register. However given this an aggregate BER counter (i.e. one single count for the interface) then adding one extra register would not appear to be a huge overhead.

**Suggested Remedy**

Consider increasing the size of the BER counter to be 24 bits as recommended in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf, or as a minimum use all 16 bits in the higher order register for the BER count, resulting in a 22 bit aggregate counter (lower 6 bits in reg 3.33 and the upper 16 bits in reg 3.44).

**Response**

ACCEPT IN PRINCIPLE.

Increase the total counter size to 22 bits.
### Comment 215

**Comment Type:** E  
**Comment Status:** R

Text does not make it clear that as agreed to at the last meeting we changed from counting bit to block errors.

**Suggested Remedy:**
Update text to reflect the fact that these counters are now counting block errors as described in section 82.2.14 and associated comment against the same section that I submitted this time against D2.2.

**Response Status:** C

**Response:** REJECT.

82.2.14 was changed by comment #270 against draft 2.1. It is now clear that block errors are counted, not bit errors. Nothing in 45.2.3.37 contradicts this.

### Comment 210

**Comment Type:** TR  
**Comment Status:** A

Table 45-114a defines an 8 bit BIT counter for each PCS lane.

Slide 6 in http://www.ieee802.org/3/ba/public/jan09/nicholl_01_0109.pdf, recommended that:

"A suitably sized counter shall be allocated in the MDIO memory space for each PCS lane, to ensure that the counter will not saturate (overflow) even if polled at a rate of once per second."

This proposal was accepted by the group as documented in the response to comment #374 in http://www.ieee802.org/3/ba/public/jan09/P8023ba-D11_Final_Resolution_byClause.pdf.

An 8 bit counter is not a 'suitably sized' counter.

A suitably sized counter would be 14 bits.

**Suggested Remedy:**
Update all PCS lane BIP counters to be at least 14 bits. The simplest approach would be to assign a full 16 bit register to each PCS lane BIP counter.

**Response Status:** C

**Response:** ACCEPT IN PRINCIPLE.

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

Change all PCS BIP counters to 16 bit.

### Comment 10

**Comment Type:** T  
**Comment Status:** A

Implement 802.3 maintenance request 1209:

http://grouper.ieee.org/groups/802/3/maint/requests/maint_1209.pdf

**Suggested Remedy:**
Change DME_receive_idle to an_receive_idle
also do the same for mr_parallel_detection_fault variable

**Response Status:** C

**Response:** ACCEPT.

---

**Type:** TR/technical required  
**ER/editorial required:** G/general required  
**T/technical:** E/editorial  
**G/general:**

**Comment Status:** D/dispatched  
**A/accepted:** R/rejected  
**Response Status:** O/open  
**W/written:** C/closed  
**U/unsatisfied:** Z/withdrawn

**Sort Order:** Clause, Subclause, page, line
IEEE P802.3az is making changes Clause 74 IEEE Std 802.3-2008. These changes are specific to 10GBASE-R PHYs. IEEE P802.3ba has changed Clause 74 to address 10GBASE-R and 40/100GBASE-R PHYs. Therefore, coordination between the two projects is needed to manage the changes in that project to only the 10GBASE-R PHY section.

**Suggested Remedy**

Coordinate modifications of Clause 74 with IEEE P802.3az editorial team.

**Response**

REJECT.

This is a reject because no changes will be made to the 802.3ba draft as a result of this comment.

The P802.3ba editorial team recognizes that the P802.3az project is also proposing changes to Clauses 74, 45 and 69. The relevant 802.3ba editors will co-ordinate with 802.3az editors regarding this issue.

The current expectation is that 802.3ba will be published before 802.3az so it will be 802.3az that will need to take into account the changes made by 802.3ba rather than the other way round.

---

FEC_corrected_blocks_counter and FEC_corrected_blocks_counter_i count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.87 (1.172, 1.173) and 45.2.1.89 (1.176 to 1.215).

FEC_uncorrected_blocks_counter and FEC_uncorrected_blocks_counter_i count once for each uncorrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.88 (1.174, 1.175) and 45.2.1.90 (1.216 to 1.255).

**Suggested Remedy**

Change to:

FEC_corrected_blocks_counter counts once for each corrected FEC blocks processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK.

FEC_uncorrected_blocks_counter counts once for each uncorrected FEC blocks processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK.

**Response**

ACCEPT IN PRINCIPLE.

Change:

FEC_corrected_blocks_counter counts once for each corrected FEC blocks processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK.

to:

FEC_corrected_blocks_counter (for single lane PHYs) or FEC_corrected_blocks_counter_i (for multi-lane PHYs) count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. These are 32-bit counters. These variables are accessed through a management interface that may be mapped to the registers defined in 45.2.1.87 (1.172, 1.173) and 45.2.1.89 (1.176 to 1.215).

Change:

FEC_uncorrected_blocks_counter counts once for each uncorrected FEC blocks processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK.

to:

FEC_uncorrected_blocks_counter (for single lane PHYs) or FEC_uncorrected_blocks_counter_i (for multi-lane PHYs) count once for each uncorrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. These are 32-bit counters. These variables are accessed through a management interface that may be mapped to the registers defined in 45.2.1.88 (1.174, 1.175) and 45.2.1.90 (1.216 to 1.255).
The optical interfaces listed in the table give their respective reaches while the electrical interfaces do not.

**Suggested Remedy**
- For 40GBASE-KR4, add "with reach up to at least 1m"
- For 40GBASE-CR4 and 100GBASE-KR4, add "with reach up to at least 7m"

**Response**
- ACCEPT IN PRINCIPLE.

In Table 80-1 and clause 1.4
- For 40GBASE-KR4, add "with reach up to at least 1m"
- For 40GBASE-CR4 and 100GBASE-CR10, add "with reach up to at least 7m"

---

**Comment Type**: E  **Comment Status**: A

**Comment**: Runon sentence (too many "ands")

**Suggested Remedy**
- Replace "The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers and is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."
- with "The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers, is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."

**Response**
- ACCEPT.
Comment Type: T  

Comment Status: A  

The definition of Skew Variation is not correct. Consider a link with relative delays on 4 lanes of 0, 20, 20, 20 UI.

The definition of Skew is:

Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits.

So the skew of the above example is 20 UI.

Now change the delay in the second lane so that the relative delays become: 0, 0, 20, 20 UI. The Skew is still 20 UI.

Skew Variation is defined as:

Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation.

So the Skew Variation after the change is 0 UI. However, the delay on the second lane has changed by 20 UI so you need 20 bits in the gearbox buffer.

Suggested Remedy:

Change:

"Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation."

to:

"Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation."

Response: ACCEPT.

Comment Type: TR  

Comment Status: A  

No test method is defined for measuring dynamic skew.

Suggested Remedy:

Transmitter lane under test transmits suitably long PRBS pattern with length at least twice as long as the maximum skew variation and based on the scope capability while other lanes transmit PRBS31. Transmitter lane under test output is split in two. One set of output goes to the golden PLL as defined by the specific PMDS to provide triggering to oscilloscope. The second output goes to the oscilloscope inputs which can lock to the PRBS pattern. Skew variation on the first lane is recorded, the measurement is then repeated for the remaining lanes to determine maximum skew variation.

Response: ACCEPT IN PRINCIPLE.

At the end of 85.5 add:

The measurements of Skew and Skew Variation are defined in 85.5.1 >>>Title 85.5.1 Measurements of Skew and Skew Variation

Skew and Skew Variation are defined in 80.5 and are required to remain within the limits given in 85.5 over the time that the link is in operation. The measurement of Skew and Skew variation is made by acquiring the data on each lane using a clock and data recovery unit with a high frequency corner bandwidth and slope as specified in 86.8.3.2. The arrival times of the one to zero transition of the alignment marker sync bits on each lane are then compared. This arrangement ensures that any high frequency jitter that is present on the signals is not included in the skew measurement.
**Comment Type**: T

**Comment Status**: A

Column heading state maximum skew variation but the values have approximate symbol=

**Suggested Remedy**

- Please replace~ with max value of skew variations

**Response**

ACCEPT IN PRINCIPLE. [Editor's note: Please do not use special character "tilde" or approximate symbol in comments since this is used as delimiter by the comment tool]

See response to comment #94

---

**Comment Type**: TR

**Comment Status**: A

No test method is defined for measuring skew

**Suggested Remedy**

Transmitter lane under test transmits suitably long PRBS pattern with length at least twice as long as the maximum skew and based on the scope capability while other lanes transmit PRBS31. Transmitter lane under test output is split into two. One set of output goes to the golden PLL as defined by the specific PMDS to provide triggering to oscilloscope. The second output goes to the to the oscilloscope inputs which can lock to the PRBS pattern. A visible edge is identified for the first lane, the measurement is then repeated for the remaining lanes to determine maximum skew.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #105

---

**Comment Type**: E

**Comment Status**: A

The use of the term "scalable" could be misconstrued. There are two distinct interfaces - one that supports 40Gb/s and another that supports 100 Gb/s

**Suggested Remedy**

- Change
  a) It is scalable and capable of supporting speeds of 40 Gb/s and 100 Gb/s.
  b) Data and delimiters are synchronous to a clock reference.
  c) It provides independent 64-bit-wide transmit and receive data paths.
  d) It provides for full duplex operation only.

to

a) The XLGMII interface supports speeds of 40 Gb/s.
b) The CGMII interface supports speeds of 100 Gb/s.
c) Data and delimiters are synchronous to a clock reference.
d) It provides independent 64-bit-wide transmit and receive data paths. 
e) It provides for full duplex operation only.

**Response**

ACCEPT IN PRINCIPLE.

a) The XLGMII interface supports a speed of 40 Gb/s.
b) The CGMII interface supports a speed of 100 Gb/s.
c) Data and delimiters are synchronous to a clock reference.
d) It provides independent 64-bit-wide transmit and receive data paths. 
e) It provides for full duplex operation only.
The specification of which sequence ordered set values is reserved is not specified clearly. It appears that lane one or lane two can be anything (>=0x00) but that lane 3 must be >=0x03 for it to be a reserved value. But a value like 0x01 0x00, 0x00 in lanes 1-2-3 are probably also in the group that are considered to be reserved even though it doesn’t meet the lane 3 inequality.

Suggested Remedy
Consider showing three rows for reserved:

<table>
<thead>
<tr>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
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<tbody>
<tr>
<td>&gt;=0x01</td>
<td>&gt;=0x00</td>
<td>&gt;=0x00</td>
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<td>&gt;=0x00</td>
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<tr>
<td>&gt;=0x00</td>
<td>&gt;0x00</td>
<td>&gt;=0x03</td>
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</table>

Lane 3 can be 0x01 or 0x02 if lane 1 or lane 2 is >=0x01 and it is still reserved.

Accept in principle.
Delete this row and add a note: “All other values in lanes 1-3 not shown in this table are reserved.”

Clarifying D2.1 comment 32:
There are two error counting mechanisms that can be used on 64B/66B signals: errored blocks and BIP errors. For isolated errors at error rates of interest, they will give near-identical results. But if burst errors are involved, the errored block counter will typically count 1 per burst while the BIP error counters will typically count the number of errors in the burst.

We should be unambiguous which is meant by BER for the purposes of compliance. As the errored block counter is not very good in service at good BERs, we expect in-service monitoring to use BIP (that’s why it was introduced). It is HIGHLY desirable that the same definition of BER apply in compliance testing with the scrambled idle signal as in service. Also, as MTTFP is so important and burst errors are a threat to it, BIP counting is preferable for another reason.

The response to D2.1 comment 32 points out that BIP counting saturates too low for the current hi_ber threshold. So continue with block counting (as is) for the BER monitor state diagram, but...

Suggested Remedy
Say that BER for 64B/66B signals (including the scrambled idle signal) is defined by BIP error counting (rather than by the BER monitor state diagram). Although the count from the BER monitor state diagram may be useful for diagnostics at very bad BER.

Accept.

The proposal is not a complete solution and is proposing a significant change to the PCS test pattern operation.
Comment Type E  Comment Status A
I know what is meant, but I still find that the phrase "for each 8-bit BIP value in error" in the last sentence is not as clear as it could be.

Suggested Remedy
Suggest replacing the last sentence with:
"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented by one, each time the calculated BIP value does not exactly match the BIP value received in the BIP3 field (registers 3.90 through 3.99)."

Response Response Status C
ACCEPT IN PRINCIPLE.
Change:
"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented for each 8-bit BIP value in error (registers 3.90 through 3.99)."
To:
"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 3.90 through 3.99) is incremented by one each time the calculated BIP value does not equal the value received in the BIP3 field."

Comment Type TR  Comment Status A
There is no limit to the potential increment rate of the PRBS31 checker referenced in 49.2.12.
The checker implementation is difficult to match at high increment rates or in the presence of burst errors (the source synchronous descrambler implementation error multiplication factor depends on burst pattern).
There will be less scope for a complex implementation in a PMA device versus a PCS.
For most practical purposes stringent matching of the 49.2.12 implementation is not necessary. It would be sufficient to match the result of a 49.2.12 implementation only for isolated single bit errors and at errors rates less than 1 in a thousand.

Suggested Remedy
Replace:
(see 49.2.12)
With:
The PRBS31 checker shall match the results of the checker implementation in 49.1.12 for isolated single bit errors and at errors rates less than 1 in a thousand.
There will be a contribution at the September interim to support this comment

Response Response Status C
ACCEPT IN PRINCIPLE. [Editor's Note: Commenter did not indicate comment type. Assigned comment Type TR]
Replace:
(see 49.2.12)
With:
The checker shall increment the test pattern error counter by one for each incoming bit error in the PRBS31 pattern (see 49.2.8) for isolated single bit errors. Implementations should be capable of counting at least one error whenever one or more errors occur in a sliding 1000 bit window.
Comment Type: E  Comment Status: A
Gbaud

Suggested Remedy: GBd (twice)

Response: ACCCEPT.

Comment Type: E  Comment Status: D
Nicholl, Gary  Cisco

Suggested Remedy:
Suggest adopting a similar naming convention for the service interface primitives for the interface above the PMA (i.e. at the top of the figure), to reflect that the sublayer above the PMA can be either a PMA, FEC or PCS.

Proposed Response: REJECT.

This comment was WITHDRAWN by the commenter.

The service interface is named according to the sublayer that provides the service. The problem with the sublayer below is that you know that the sublayer provides the generic service interface, but you don't know which sublayer it is (PMD, PMA, or FEC) that is providing it. To describe the PMA service interface, the sublayer providing the service is always the PMA, so you can name the primitives, e.g., PMA:IS_UNITDATA_i.request(tx_bit) without having to know whether it is the PCS, FEC, or another PMA invoking that primitive.
Comment Type: TR/technical required

Comment Status: R/rejected

Following up on D2.1 comment 33. anslow_05_0709 showed that for two scenarios with an almost-minimum 32 UI delay between lanes, the peak baseline wander was about 50% more than for a single PRBS31. I believe that if the delay is substantially increased, that 50% will substantially reduce. Maybe I'll get the simulation done by the meeting. The larger delay could be generated by choosing appropriate seeds for each lane’s PRBS generator and starting the generators together, but that’s implementation.

Suggested Remedy

The first part of the remedy is similar to last time: Change “on each of the lanes” to “on each of the PCS lanes” here and at line 30. Change “one lane and any other lane” to “one PCS lane and any other PCS lane”. In the paragraphs beginning line 38 and line 50, change “lane” or “lanes” to “PCS lane” or “PCS lanes”.

Delete “Note that bit multiplexing of per-lane PRBS31 may produce a signal which is not meaningful for downstream sublayers.”

Provide 20 PRBS31 error counters in each direction, one per PCS lane.

Another solution which would take a few more words would be to generate by 10G lanes and check by 20G PCS lanes, for 100G. Do we have a name for a 10G lane? For 40G, because we have a binary series of lane speeds, generating per lane (whatever that is) and checking per (10G) PCS lane is ideal, but generating by 10G lanes with offset would still work.

Increase the 31 bits (UI) minimum delay between generator lanes to a number TBD, around 2000 UI.

Response: REJECT.

D2.1 comment 33 was rejected based on the analysis in anslow_05_0709. The decision should not be reconsidered unless:
1) simulation results can be provided to show that larger offsets do not significantly increase the baseline wander over PRBS31;
2) it can be shown that it is not unduly onerous to be required to generate 20 PRBS31 sequences that are offset by 2000 UI; and
3) a specific offset value can be provided which meets the necessary requirements.

Note that there is no other aspect of the PMA which is aware of PCS lanes and other mechanisms (e.g., scrambled idle test pattern, BIP) are available for multi-sublayer testing.

Draft says “There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane.”. This was to stop the lanes being highly correlated and hence the lane-to-lane crosstalk being unrealistic. However, Skew Variation, not necessarily in the generating PMA, could reduce these relative delays.

Suggested Remedy

Increase 31 by the appropriate Skew Variation or say “a delay of 31 UI plus the allowance for Skew Variation for the downstream sublayers as given in Table 80-5.” But see another comment.

Response: ACCEPT IN PRINCIPLE.

Replace:

“There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane.”

with:

“To avoid correlated crosstalk, it is highly recommended that the PRBS31 patterns generated on each lane be generated from independent, random seeds or at a minimum offset of 20 000 UI between the PRBS31 sequence on any lane and any other lane.”

Response: ACCEPT IN PRINCIPLE.

Overtaken by events. See comment #75.
Comment Type: T
Comment Status: A

Piling on to D2.1 comment 253. What is in the draft seems so impractical and unnecessarily power-hungry that it won't be obeyed fully. Draft refers to 49.2.12 which says "The test-pattern error counter shall increment once for each bit time that the PRBS31 pattern error signal is high," which could approach the lane line rate. Unlike the assertion in the response to comment 34, choosing an implementation dependent limitation would seem not to be allowed. For comparison, even a lab BERT saturates or drops sync at some point e.g. $10^{-5}$ or $10^{-3}$.

Suggested Remedy
If you want to stay with the checker of 49.2.12 then write down that a .3ba version need not count error ratios above $10^{-3}$ accurately. This will ease both the high-speed analog silicon and also the management counters. Also, it might be desirable to define a maximum reported error rate so that the management software doesn't have to be designed to cope with ridiculous BERs. (Per response to D2.1 comment 32, the high BER state machine kicks in at a 10^-4 BER, so anything much above that is hopelessly bad and we don't need an exact measurement of it.) Also, it may ease the implementation to write down that a .3ba version need not count burst errors precisely as 49.2.12 (which isn't accurate for all bursts, anyway).

Response
ACCEPT IN PRINCIPLE.
See response to comment 45.

Comment Type: ER
Comment Status: A

There is some concern regarding the use of the term mapping and how it relates to what is illustrated in Fig 83-6. The use of the word "mapping" seems to address how input lanes are directed to output lanes, but in the commenter's opinion does not do an adequate job addressing the sequencing of bits on the output lanes, which may lead to interpretation issues.

Suggested Remedy
Further clarifying text is needed. See presentation by dambrosia.

Response
ACCEPT IN PRINCIPLE.
In clause 83.1.4, replace "remaps" with "maps". Replace text in 83.5.2 and Figure 83-6 with trowbridge_01_0909.pdf. Update PICS LANE_MAPPING to read "Maintain sequence of PCSLs on all output lanes".

Response
ACCEPT.

Comment Type: E
Comment Status: A

Note on Fig 83-6 is incorrect. Note reads:
"NOTE: i.k indicates bit i on PCSL k. Skew may exist between PCSLs"

The i and k are reversed from what is shown in the figure.

Suggested Remedy
Change note to read:
"NOTE: i.k indicates bit k on PCSL i. Skew may exist between PCSLs"

Response
ACCEPT.
Cl 83 SC 83.5.4 P 213 L 13 # 17
Anslow, Peter Nortel Networks
Comment Type E  Comment Status A
Double full stop ".."
SuggestedRemedy Change ".." to ""
Response Response Status C
ACCEPT.

Cl 83A SC 83A.2.1 P L # 151
D'Ambrosia, John Force10 Networks
Comment Type TR  Comment Status A
A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83A-1 and 83A-2.

SuggestedRemedy Change 83A-1 to
[SDD21] <= -0.00086 + (0.2286 x f^(1/2)) + (0.08386 X f)
Change 83A-2 to
[SDD21] <= -0.00086 + (0.2286 x f^(1/2)) + (0.08386 X f)
Response Response Status C
ACCEPT IN PRINCIPLE.

See resolution to comment #15
see also dambrosia_01_0909 for parameter naming convention
Comment Type | TR | Comment Status | A
---|---|---|---

A number of equations related to return loss / Sxymn have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers. For Return Loss constraints the requirement should be "greater than or equal to" the equation.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.


Suggested Remedy

For noted equations change sign from "less than or equal to" to "greater than or equal to"

Response | Response Status | C
---|---|---

ACCEPT IN PRINCIPLE.

See previous Remedy. Change Equations 83A-5, 83A-7, 83A-8, and 8A-10 to "greater than or equal to" sign.

see also dambrosia_01_0909 for parameter naming convention & equation format

Ensure consistency & suggested remedy

---

Comment Type | TR | Comment Status | R
---|---|---|---

Following up D2.1 comment 159, According to 83.3, a PMA has TX and RX directions, each of which has an input and output. nAUI is intended to connect PMAs, e.g. one in the host and one in a module. Therefore nAUI must connect a (host) TX (transmitter) output to a (module) transmitter input, and a (module) RX (receiver) output to a (host) receiver input. 83B and 86A use the terms host output, module input, module output, host input, which is compatible with 83. But Figure 83A-2 shows two "Transmitter"s and two "Receiver"s, one for each direction. This isn't compatible terminology.

Suggested Remedy

Change "Transmitter" to "output" or "driver" or "driver output" as appropriate, "Transmit Compliance Point" to "output compliance point", "Receiver" to "input", and "Receiver Compliance Points" and "Receive Compliance Point" to "output compliance point", throughout 83A.

Response | Response Status | W
---|---|---

REJECT.

See comment 200 for consistency between 83A & 83B

---

Comment Type | T | Comment Status | A
---|---|---|---

I seem to remember that there is a style guide rule that all figures must be referred to by some text. Even if it is not in the style guide rules it is good practice. There are a number of figures in this annex that do not have references. Figure 83A-3 is the first one.

This also applies to figure 83A-4, 83A-6, 83A-7, 83A-10, 83A-11, 83A-13, 83A-14

Suggested Remedy

If I am correct then add "and illustrated in figure 83A-3" to the end of line 23, and a similar remedy for the other figures.

Response | Response Status | C
---|---|---

ACCEPT IN PRINCIPLE.

See comment 153
Cl 83A  SC 83A.2.1  P 383  L 25  #  83
Dawe, Piers  Independent
Comment Type  TR  Comment Status  A
SDD21 does not represent loss, it represents forward gain ("through response" or just "response"; 47.4.1 calls it "transmission magnitude response"). For modules, we should stay with S-parameters, as is common industry practice in SFP+, CXP, XAUI (Clause 47) and so on, but the names need cleaning up.

SuggestedRemedy
Change "differential insertion loss" to "differential response". Change "less than" to "more than or equal to". Reverse the signs and the inequality in equation 83A-1 and Figure 83A-3.

Response  Response Status  W
ACCEPT IN PRINCIPLE.

See comment 151.

Cl 83A  SC 83A.3.3  P 385  L 19  #  18
Anslow, Peter  Nortel Networks
Comment Type  E  Comment Status  A

In Table 83A-1, the "Maximum De-emphasis" is given as 7.0 dB
In Table 83B-3, the "Maximum De-emphasis" is given as 6.0 dB
In accordance with the response to comment #501 against Draft 1.1, these should be 7 dB and 6 dB respectively.
Also on page 398 line 33 7.0 dB should be 7 dB

SuggestedRemedy
In Table 83A-1, change "7.0" to "7"
In Table 83B-3, change "6.0" to "6"
On page 398 line 33, change "7.0" to "7"

Response  Response Status  C
ACCEPT.

Cl 83A  SC 83A.3.3.1  P 386  L 8  #  64
Dawe, Piers  Independent
Comment Type  TR  Comment Status  R
De-emphasis means a relative attenuation of the higher frequencies, as in "Dolby noise reduction is a form of dynamic preemphasis employed during recording, plus a form of dynamic deemphasis used during playback". So de-emphasis is the opposite of what you want.

SuggestedRemedy
We don’t need to argue about de- versus pre-: just change "De-emphasis" to "Emphasis", and "Vth-demph" (or "Vth-demph") to "VMA", throughout.

Response  Response Status  W
REJECT.

De-emphasis is an industry standard term.

Cl 83A  SC 83A.3.3.2  P 386  L 42  #  223
Latchman, Ryan  Gennum Corp
Comment Type  T  Comment Status  A

"Rise/fall time is measured with de-emphasis off" should include a reference to 83A.5.1

SuggestedRemedy
"Rise/fall time is measured with de-emphasis off as defined in 83A.5.1"

Response  Response Status  C
ACCEPT.

See suggested remedy
<table>
<thead>
<tr>
<th>CI</th>
<th>SC</th>
<th>Subclause</th>
<th>Page</th>
<th>Line</th>
<th>Type</th>
<th>Comment</th>
<th>Status</th>
<th>Response</th>
<th>Status</th>
<th>Commenter</th>
<th>Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>83A</td>
<td>83A.3.3.3</td>
<td>P 387</td>
<td>L 12</td>
<td>#19</td>
<td>E</td>
<td>The differential output return loss is required to be met from 10 MHz, but Figure 83A-6 stops at 50 MHz. Also applies to Figures 83A-7, 83A-10, 83A-11</td>
<td>A</td>
<td>Anslow, Peter Nortel Networks</td>
<td>C</td>
<td>Extend Figures 83A-6, 83A-7, 83A-10, 83A-11 to 10 MHz</td>
<td>ACCEPT.</td>
</tr>
<tr>
<td>83A</td>
<td>83A.3.3.4</td>
<td>P 387</td>
<td>L 49</td>
<td>#80</td>
<td>TR</td>
<td>As I pointed out in D2.1 comment 35, S-parameters define power gain, not loss.</td>
<td>R</td>
<td>Dawe, Piers Independent</td>
<td>W</td>
<td>Change the signs on the right hand side, change the direction of the inequality back to &lt;= as in D2.1.</td>
<td>REJECT.</td>
</tr>
<tr>
<td>83A</td>
<td>83A.3.3.5</td>
<td>P 388</td>
<td>L 32</td>
<td>#20</td>
<td>ER</td>
<td>Requirements for TJ and DJ are found in a subclause titled, &quot;Transmitter eye mask definition&quot;. This can make these definitions difficult to find and seems unnecessary as a subclause can easily be added for jitter definition.</td>
<td>A</td>
<td>Petrilla, John Avago Technologies</td>
<td>C</td>
<td>Create a subclause, '83A.3.3.6 Transmitter jitter definition'. Cut the sentence, &quot;The measured jitter at the transmit compliance point shall be less than the maximum Total Jitter as defined in Table 83A-1 and a maximum Deterministic Jitter as defined in 83A-1.&quot; from 83A.3.3.5 and paste it into 83A.3.3.6 as the first sentence. From 83A.3.3.5 copy the sentence &quot;Jitter and eye mask measurement requirements are described in 83A.5.1, and are conducted with de-emphasis off.&quot; and paste it into 83A.3.3.6 deleting the words, 'and eye mask'. Then in 83A.3.3.5, in the last sentence delete the words, 'Jitter and'. Update the references in tables 83B-3 and 83B-5 to refer to 83A.3.3.6 for TJ and DJ.</td>
<td>ACCEPT IN PRINCIPLE.</td>
</tr>
</tbody>
</table>
Cl 83A SC 83A.3.4 P 389 L 35 # 184
Dudek, Mike QLogic

Comment Type T Comment Status A

Table 83A-2 is actually a mixture of receiver characteristics (e.g., return losses) and specifications of the most degraded signal the receiver has to tolerate (e.g., total jitter). The receiver does not have a maximum total jitter. It's characteristic is a minimum total jitter tolerance.

Suggested Remedy
Split table 83A-2 into two tables. Table A labelled "Receiver input tolerance requirements" with everything in the existing table except the return losses. Table B labelled "Receiver characteristics" with just the return loss lines.

The sentence on page 389 line 26 then becomes. "The receiver shall tolerate signals with the characteristics given in Table A. The receiver shall also have the characteristics given in Table B."

An alternative remedy keeping one table is changing the maximum values of the input signal into minimum input tolerances as done in table 86A-4

Response ACCEPT IN PRINCIPLE.

Rename the following:
Maximum Total Jitter to "Minimum Total Input Jitter Tolerance"
Maximum Deterministic Jitter to: "Minimum Deterministic Input Jitter Tolerance"

Add row above Minimum total input jitter tolerance and have the following text:
"Stressed Receiver Tolerance"

Modify section 83A.3.4.6 accordingly (maximum becomes minimum)

Cl 83A SC 83A.3.4.6 P 393 L 4 # 202
Petrilla, John Avago Technologies

Response ACCEPT.

See suggested remedy

Cl 83A SC 83A.5.1 P 395 L 16 # 233
Misek, Brian Avago Technologies

Comment Type T Comment Status R

In the process of implementing my previous comment about this "off" state I think this is too ambiguous. The off state was agreed to be the state where the Tx equilization could be set to compensate for the compliance point not being at the pins of the package. I don't think the text conveys that clearly.

Suggested Remedy
Change line 15: from
"Transmit de-emphasis off state is the optimal setting for transmitter jitter and eye mask evaluation."

"Transmit de-emphasis off state is the optimal setting for the channel present in the transmitter jitter and eye mask evaluation."

Response REJECT.

Current definition is adequate

[Editor's note: Late comment for consideration by the Task Force]
Comment Type: TR

Comment Status: A

FR4 trace stress not clear what it is

Suggested Remedy:

- Suggest either use Frequency Dependent Attenuator or PCB Trace

Response: C

ACCEPT IN PRINCIPLE.

Change:
FR4 trace stress is then added until 0.42 UI peak-to-peak deterministic jitter is achieved

to:
Stress is then added using PCB trace or Frequency Dependent Attenuation which emulates PCB loss. PCB trace stress is added until 0.42 UI peak-to-peak deterministic jitter is achieved.

Modify diagram (change FR4 to PCB)

Make same changes in 83B.2.3

---

Comment Type: TR

Comment Status: A

A number of equations related to return loss / Sxymn have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers.

The equations all result in negative numbers

For Return Loss constraints the requirement should be "greater than or equal to" the equation

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83B-5, 83B-6, 83B-8, and 83B-9.

Suggested Remedy:

Change Eqs 83B-5, 83B-9 to
\[ |SDD11| \geq 12 - (2 \times f) \]
\[ 5.56 - (8.76 \times \log_{10} (f/5.5)) \]
\[ 0.01 \leq f \leq 2.19 \]
\[ 2.19 \leq f \leq 11.1 \]

Change Eqs 83B-6, 83B-8 to
\[ |SDD22| \geq 12 - (2 \times f) \]
\[ 5.56 - (8.76 \times \log_{10} (f/5.5)) \]
\[ 0.01 \leq f \leq 2.19 \]
\[ 2.19 \leq f \leq 11.1 \]

For noted equations change sign from "less than or equal to" to "greater than or equal to"

Response: C

ACCEPT IN PRINCIPLE.

See suggested Remedy for correction of the signs.

See resolution to comment #15

see also dambrosia_01_0909 for parameter naming convention
**Comment Type**: E  
**Comment Status**: A  
**Comment**: All of the figures in this clause follow equations, but there are no statements regarding an equation being illustrated in a figure.  
**Suggested Remedy**: Add statement following equation that the equation is illustrated in Fig 83B-x.  
**Response**: ACCEPT.  
**Response Status**: C  
Add the following to 83B.1:  
Equation 83B-1 is illustrated in Figure 83B-1 and Equation 83B-2 is illustrated in Figure 83B-2.  
Modify the following sentence in 83B.2:  
The differential insertion loss, expressed in decibels, for the HCB shall be less than the insertion loss defined by Equation (83B-3) and illustrated in Figure 83B-3.  
Modify the following sentence in 83B.2:  
The differential insertion loss, expressed in decibels, for the MCB shall be less than the insertion loss defined by Equation (83B-4) and illustrated in Figure 83B-6.  
83B.2.1  
Modify the following:  
where \( f \) is the frequency in GHz. Maximum module input reflection is illustrated in figure 83B-8.  
Modify the following:  
where \( f \) is the frequency in GHz. Maximum module output reflection is illustrated in figure 83B-8.  
Make similar changes to 83B.2.2  

---  

**Comment Type**: TR  
**Comment Status**: A  
**Comment**: A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.  
**Suggested Remedy**: Change 83B-1 and 83B-2 to:  
\[
|SDD21| \leq 0.111 + (1.046 \times f^{(1/2)}) + (1.05 \times f) \quad 0.25 \leq f \leq 7  
|SDD21| \leq -11.95 + (3.15 \times f) \quad 7 \leq f \leq 11.1
\]  
Change 83B-3 to:  
\[
|SDD21| \leq 0.04 + (0.33 \times f^{(1/2)}) + (0.32 \times f) \quad 0.25 \leq f \leq 7  
|SDD21| \leq -3.72 + f \quad 7 \leq f \leq 11.1
\]  
Change 83B-4 to:  
\[
|SDD21| \leq 0.00086 + (0.2286 \times f^{(1/2)}) + (0.088386 \times f)  
\]  
**Response**: ACCEPT IN PRINCIPLE.  
See suggested Remedy for correction of the signs.  
See resolution to comment #15.  
see also dambrosia_01_0909 for parameter naming convention.
**Comment Type:** T  
**Comment Status:** A  
**Suggested Remedy:**  
Equation for module loss not correctly scaled  

**Response Status:** C  
**Response:**  
ACCEPT IN PRINCIPLE.

**SDD22 = 3.2 - 0.84f  7<f<11**

---

**Comment Type:** ER  
**Comment Status:** A  
**Suggested Remedy:**  
Repeating comment 159 of D2.1, Figure 83A-1 is similar to Figure 83B-3 but the names on what may be identical items are different, e.g. XLAUI/CAUI Component vs XLAUI/CAUI IC, Driver vs Transmitter, Input vs Receiver. It's not good practice where block diagrams showing the same level of detail use different names for the same item. If these block diagram elements are actually the same, please use the same terminology, otherwise this is inconsistent and can be confusing. See also Figs 83B-5 & 7.

**Response Status:** C  
**Response:**  
ACCEPT IN PRINCIPLE.

**Suggestion:**  
If the XLAUI/CAUI Component & XLAUI/CAUI IC are the same use the same name. Likewise for Driver & Transmitter use Transmitter and for Input & Receiver use Receiver.

**Response Status:** C  
**Response:**  
ACCEPT IN PRINCIPLE.

For Driver use Transmitter and for Input use Receiver and use Component instead of IC in figure 83B-3, 83B-5, 83B-7.

---

**Comment Type:** TR  
**Comment Status:** A  
**Suggested Remedy:**  
The loss of the host compliance board is allowed to vary from zero to 2.1dB at Nyquist. This will significantly change the results of measurements.

**Response Status:** C  
**Response:**  
ACCEPT IN PRINCIPLE.

**Suggestion:**  
1. Change the sentence on line 19 to "The differential insertion loss, CPIL, expressed in decibels, for the reference HCB shall be CPIL, as defined by Equation (83B-3). Differences between this reference loss and the loss of an actual HCB shall be accounted for in the measurements. Change the inequality in equation 83B-3 into =. Change figure 83B-5 to HCB PCB 2.1dB

or

2. add a minimum loss for the HCB with this minimum loss scaled to 1.1dB at the Nyquist rate. Change figure 83B-5 to HCB PCB between 1.1 and 2.1dB

**Response Status:** C  
**Response:**  
ACCEPT IN PRINCIPLE.

Delete text: "The differential insertion loss, CPIL, expressed in decibels, for the HCB shall be less than CPILmax, as defined by Equation (83B-3)"

Replace with:"  
The reference HCB test fixture PCB insertion loss is given in Equation (83B-3-[note change <= to =]). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.
Comment Type: T  Comment Status: A

The equation (83B-3) has an inequality sign for the [SDD21] Host Compliance Board insertion loss.

Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

Suggested Remedy
Replace the inequality sign with an equal sign "=".

Response  Response Status: C
ACCEPT IN PRINCIPLE.

See comment#186

Comment Type: T  Comment Status: A

The equation (83B-4) has an inequality sign for the [SDD21] Module Compliance Board insertion loss.

Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

Suggested Remedy
Replace the inequality sign with an equal sign "=".

Response  Response Status: C
ACCEPT IN PRINCIPLE.

In Table 83B-2, compliance point terms TP1, TP1a and TP4 are used without definition or reference. If these are the same points as in clause 86 or 86A, then 86 should be cited. (Clause 85 also defines a TP1 and TP4 but no TP1a) If not, there should be a figure defining these points.

Suggested Remedy
If TP1, TP1a and TP4 are the same as in clause 86, add a note to table 83B-2 citing clause 86, figure 86-3, for the definition of these points.

Proposed Response  Response Status: Z
REJECT.

This comment was WITHDRAWN by the commenter.
Type: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
Comment Status: D/dispatched  A/accepted  R/rejected  Response Status: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn
Sort Order: Clause, Subclause, page, line

---

**Comment:** Petrella, John  Avago Technologies  
*Comment Type:* E  *Comment Status:* A  
Table 83B-3 footnote a is redundant with the entry in the subclause column and can be deleted. This also occurs in Table 83B-5.

**Suggested Remedy:** In Table 83B-3 and 83B-5, delete footnotes a.

**Response:**  *Response Status:* C  
ACCEPT.

---

**Comment:** Dudek, Mike  QLogic  
*Comment Type:* T  *Comment Status:* A  
Vth-demph is used in equation 83B-7 however Vtx-demph is used in Table 83B-3.

**Suggested Remedy:** Change Vth-demph to Vtx-demph in equation 83B-7.

**Response:**  *Response Status:* C  
ACCEPT.

---

**Comment:** Ghiasi, Ali  Broadcom  
*Comment Type:* TR  *Comment Status:* A  
FR4 trace stress not clear what it is.

**Suggested Remedy:** Suggest either use Frequency Dependent Attenuator or PCB Trace.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE. See comment 123.

---

**Comment:** Misek, Brian  Avago Technologies  
*Comment Type:* T  *Comment Status:* A  
The rest of the document uses linear frequency for plots of Insertion loss, Return Loss etc., this section does not. It has the tendency to give too much visual weight to the low frequencies.

**Suggested Remedy:** All plots of this nature changed to linear frequency.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force] see resolution comment #88.

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**Comment:** Dudek, Mike  QLogic  
*Comment Type:* TR  *Comment Status:* A  
The parameters in Table 85-8 do not adequately specify the cable as there are no insertion loss or insertion loss deviation specifications at frequencies other than 5.15625GHz. Resonances can occur that meet the specification at this one frequency but cause problems at other frequencies. Also the return loss specification is too relaxed.

**Suggested Remedy:** Change the parameter for the first row of Table 85-8 to "Maximum fitted insertion loss at 5.15625GHz". For insertion loss deviation delete "at 5.15625GHz and change the value to "see 85.10.3". Delete at 5.15625 GHz from the return loss specification and change the specification to "see equation 85.1" or "see 85.10.4".

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE.

---

**Comment:** Ghiasi, Ali  Broadcom  
*Comment Type:* TR  *Comment Status:* A  
FR4 trace stress not clear what it is.

**Suggested Remedy:** Suggest either use Frequency Dependent Attenuator or PCB Trace.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE.
See comment 123.

---

**Comment:** Misek, Brian  Avago Technologies  
*Comment Type:* T  *Comment Status:* A  
The rest of the document uses linear frequency for plots of Insertion loss, Return Loss etc., this section does not. It has the tendency to give too much visual weight to the low frequencies.

**Suggested Remedy:** All plots of this nature changed to linear frequency.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force] see resolution comment #88.

---

**Comment:** Dudek, Mike  QLogic  
*Comment Type:* TR  *Comment Status:* A  
The parameters in Table 85-8 do not adequately specify the cable as there are no insertion loss or insertion loss deviation specifications at frequencies other than 5.15625GHz. Resonances can occur that meet the specification at this one frequency but cause problems at other frequencies. Also the return loss specification is too relaxed.

**Suggested Remedy:** Change the parameter for the first row of Table 85-8 to "Maximum fitted insertion loss at 5.15625GHz". For insertion loss deviation delete "at 5.15625GHz and change the value to "see 85.10.3". Delete at 5.15625 GHz from the return loss specification and change the specification to "see equation 85.1" or "see 85.10.4".

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE.

---

**Comment:** Ghiasi, Ali  Broadcom  
*Comment Type:* TR  *Comment Status:* A  
FR4 trace stress not clear what it is.

**Suggested Remedy:** Suggest either use Frequency Dependent Attenuator or PCB Trace.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE.
See comment 123.

---

**Comment:** Misek, Brian  Avago Technologies  
*Comment Type:* T  *Comment Status:* A  
The rest of the document uses linear frequency for plots of Insertion loss, Return Loss etc., this section does not. It has the tendency to give too much visual weight to the low frequencies.

**Suggested Remedy:** All plots of this nature changed to linear frequency.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force] see resolution comment #88.

---

**Comment:** Dudek, Mike  QLogic  
*Comment Type:* TR  *Comment Status:* A  
The parameters in Table 85-8 do not adequately specify the cable as there are no insertion loss or insertion loss deviation specifications at frequencies other than 5.15625GHz. Resonances can occur that meet the specification at this one frequency but cause problems at other frequencies. Also the return loss specification is too relaxed.

**Suggested Remedy:** Change the parameter for the first row of Table 85-8 to "Maximum fitted insertion loss at 5.15625GHz". For insertion loss deviation delete "at 5.15625GHz and change the value to "see 85.10.3". Delete at 5.15625 GHz from the return loss specification and change the specification to "see equation 85.1" or "see 85.10.4".

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE.

---

**Comment:** Ghiasi, Ali  Broadcom  
*Comment Type:* TR  *Comment Status:* A  
FR4 trace stress not clear what it is.

**Suggested Remedy:** Suggest either use Frequency Dependent Attenuator or PCB Trace.

**Response:**  *Response Status:* C  
ACCEPT IN PRINCIPLE.
See comment 123.
<table>
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**Moore, Charles**  
Avago Technologies

**Comment Type**  
T  
**Comment Status**  
A

In table 85-8 Minima for MDNEXT loss, MDFEXT loss and power sum crosstalk loss are listed but the references do not specify either values or equations for minima. This is because these specs have been replaced by Minimum integrated crosstalk noise. These minima are no longer needed.

**Suggested Remedy**  
Delete unused specs from table 85-8

**Response**  
**Response Status**  
C  
ACCEPT IN PRINCIPLE. [Editor's Note: Commenter did not indicate comment type, assigned Comment Type: T, since the commenter is not part of the P802.3ba ballot group]

85.10.8 Cable assembly integrated crosstalk noise (ICN) uses MDNEXT and MDFEXT. Delete minimum Table 85-8 from "minimum MDNEXT" and "minimum FEXT".

<table>
<thead>
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<th>CI</th>
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</tbody>
</table>

**Mark, Gustlin**  
Cisco

**Comment Type**  
TR  
**Comment Status**  
A

The connector loss (calculated as 85-37 values minus 85-35 and 85-16) of the test fixture improves when frequency increase (see slide 5). Above formulas should be corrected to avoid this.

**Suggested Remedy**  
As above.

**Response**  
**Response Status**  
C  
ACCEPT IN PRINCIPLE.  
Replace: Test fixture insertion loss equation (85-16).  
With: equation (86A-4) using frequency range of 0.05 GHz to 10 GHz.

Also Replace: Cable assembly test fixture equation (85-35).  
With: equation (86A-5) using frequency range of 0.05 GHz to 10 GHz.

<table>
<thead>
<tr>
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</table>

**Ghiasi, Ali**  
Broadcom

**Comment Type**  
TR  
**Comment Status**  
A

The mated test fixture loss are included but the target loss for host and module test board are not included in CL85. Mated fixture loss can be met by shifting the loss from host to module or from module to host PCB by different users, in effect meeting Figure 85-12 but not interoperable

**Suggested Remedy**  
Please copy section 86A.5.1.1 in to CL85

**Response**  
**Response Status**  
C  
ACCEPT IN PRINCIPLE.  
The 85.10.10 Mated test fixtures insertion loss as well as the test fixtures (85.8.3.7-[TP-TF]) and (85.10.9-[CA-TF]) insertion losses are specified.  
See response to comment #43.
Comment Type: TR  Comment Status: A

SuggestedRemedy:
- Please use linear freq scale similar to fig 86A-3

Response: Response Status C
- ACCEPT IN PRINCIPLE. For Figure 85-12 use linear scale for consistency with linear freq scale of Figure 86A-3.

Comment Status: A

Response Status: C

Response: Ghiasi, Ali Broadcom

Proposed Response: Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Comment Type: TR  Comment Status: A

SuggestedRemedy:
- Add nominal test fixture loss at Nyquist is 2.4 dB. Test fixtures with loss lower than nominal shall account for test fixture loss difference from nominal in the equation 85-19.

Proposed Response: Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Comment Type: ER  Comment Status: A

SuggestedRemedy:
- Apparently, variable names in equations are not allowed to contain spaces. I suppose this is because to a mathematician "NEXT loss" means "NEXT" multiplied by "loss".

Response: Response Status W

ACCEPT IN PRINCIPLE.

Follow style guide; if space is to be removed then>

Change: NEXT loss

To: NEXT with subscripted loss
<table>
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<th>Cl</th>
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<tr>
<td>Dawe, Piers</td>
<td>Independent</td>
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<td></td>
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</table>

**Comment Type**: TR  
**Comment Status**: R

"NEXT loss" sounds wrong. We never expected all the power incident on the pair of test fixtures to appear as crosstalk, so how is it "lost"? It seems to be "lost" several times over, to NEXT, to FEXT, to regular transmission loss, and to reflection. This doesn't make sense. A better term to loss, which is used frequently in 802.3, is attenuation, because it focuses on the signal that's there rather than the signal that's "lost". Of course, it would be much better to specify NEXT (−dB) rather than "NEXT loss" or "NEXT attenuation" (you need to the right-way-up NEXT to calulate MDNEXT anyway).

**Suggested Remedy**: Whatever you do, don't mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

**Response**  
**Response Status**: W

REJECT.

**Multiple disturber power sum near-end crosstalk calculation and associated description in (85-26) is used in base document e.g., 802.3an..10GBASE-T..**

<table>
<thead>
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<td>Dawe, Piers</td>
<td>Independent</td>
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</table>

**Comment Type**: ER  
**Comment Status**: R

Cable assembly insertion loss is not consistent with 24.4 dB total loss budget

**Suggested Remedy**  
**Response**  
**Response Status**: Z

REJECT.

This comment was WITHDRAWN by the commenter.

The maximum channel insertion loss is determined using Equation (85A-3). The maximum channel insertion loss is 24.4 dB at 5.15625 GHz (db) (85A-3) for 50 MHz = f = 6000 MHz.

\[
\text{ILCh}(f) = \text{ILChmax}(f) = \text{ILCamax}(f) + (2 \times \text{ILHost}(f)) - (2 \times \text{ILMatedTF}(f)) \quad (85-A3)
\]

where:

- \( f \) is the frequency in MHz.
- \( \text{ILCamax}(f) \) (17.04 dB)>> The maximum cable assembly insertion loss using Equation (85-19) and Table 85-9 coefficients.
- \( \text{ILHost}(f) \) (6.5 dB)>> The maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (85-14).
- \( \text{ILMatedTF}(f) \) (2.8 dB)>> The maximum insertion loss of the mated test fixture using Equation (85-37).

\[
\text{ILCh}(f) = \text{ILChmax}(f) = 17.04 + (2 \times 6.5) - (2 \times 2.8) = 24.44 \text{ dB}
\]

**Type**: TR/technical required  
**Comment Status**: D

**Comment Type**: T  
**Comment Status**: A

The units are wrong

**Suggested Remedy**  
**Response**  
**Response Status**: C

ACCEPT.

See suggested remedy.
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<tr>
<td>Due to the restrictions on (a_1, a_2) and (a_4), caused by the maximum insertion loss at 5.125625GHz the curve in Figure 85-6 is only one example and doesn't show the maximum insertion loss at any specific frequency. Also the reference to Figure 85-6 is duplicated on page 262 line 5</td>
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<td>Change the sentence from &quot;The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and the maximum allowed values of (a_1, a_2,) and (a_4) is illustrated in Figure 85-6.&quot; to &quot;The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and one example of the maximum allowed values of (a_1, a_2,) and (a_4) is illustrated in Figure 85-6.&quot;</td>
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<td>Change the title of figure 85-6 to &quot;Example maximum cable assembly insertion loss&quot;. Delete the duplicate sentence on page 262 line 5.</td>
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<td>See suggested remedy.</td>
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<tr>
<td>The Cable assembly insertion loss deviation is required to be met from 50 MHz to 7.5 GHz. However, in Figure 85-7 the limits are illustrated from 50 MHz to 6 GHz only. Also applies to Figure 85-14 where the lines cannot be seen from 8 to 10 GHz. Also Figure 85A-1 is plotted to 6 GHz but only applies to 5.15625 GHz</td>
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<tr>
<td>Extend the lines in Figure 85-7 to 7.5 GHz</td>
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<td>Make the lines visible in Figure 85-14 up to 10 GHz</td>
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<td>Stop the line in Figure 85A-1 at 5.15625 GHz</td>
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<td>Change &quot;..&quot; to &quot;.&quot;</td>
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<tr>
<td>MDNEXTloss is defined to be computed over that range of 50 to 6000 MHz, but the calculation that uses this quantity, integrated crosstalk noise (85.10.8), requires values from 50 to 10000 MHz.</td>
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<tr>
<td>Correct the frequency range to be consistent with 85.10.8. Also correct the frequency range in 85.10.6 (MDFEXTloss).</td>
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<tr>
<td>See suggested remedy.</td>
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</tr>
</tbody>
</table>
Cl 85 SC 85.10.6 P 264 L 48 # 146
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

Unnecessary left parenthesis at end of sub-clause heading

Suggested Remedy
delete parenthesis at end of 85.10.6

Response Response Status C
ACCEPT
Suggested remedy

Cl 85 SC 85.10.7 P 263 L 14 # 60
Healey, Adam LSI Corporation

Comment Type T Comment Status A

There are no requirements on PSXT(f) and it is not used as a parameter in any of the cable assembly specifications.

Suggested Remedy
Remove 85.10.7.

Response Response Status C
ACCEPT

Cl 85 SC 85.10.8 P 265 L 40 # 55
Healey, Adam LSI Corporation

Comment Type TR Comment Status A

Equations (85-29) and (85-30) are in error. The expression "sinc² x (f/fn)" should be "(sinc(f/fn))^2" in both cases.

Suggested Remedy
Remove the superfluous "x" in both equations.

Response Response Status C
ACCEPT
See suggested remedy.

Cl 85 SC 85.10.8 P 266 L 41 # 24
Anslow, Peter Nortel Networks

Comment Type E Comment Status A

This says: "where
IL) IL denotes the value..."

Suggested Remedy
change "IL) IL denotes the value..." to "IL is the value..."

Response Response Status C
ACCEPT See suggested remedy

Cl 85 SC 85.10.8 P 267 L 1 # 147
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status R

Other figures in the draft have shown where the pass region is in relation to a stated curve

Suggested Remedy
add text "Pass Region" to region below the curve.

Response Response Status C
REJECT.

Clause 85 does not identify pass regions in other graphs and the guidance is clear..

"The total integrated crosstalk RMS noise voltage shall be less than the value specified by Equation (85-34) illustrated in Figure 85-9."

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

Page 29 of 64 9/24/2009 11:34:34 AM
Results will vary depending on the fixture insertion loss. We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A. It would also be good to specify exactly what is included in the Test fixture loss. Also the test fixture loss is not matching what was used to derive the link budget (The link budget was derived in Healey_03a_0709 has the same PCB test fixture loss as clause 86A).

**Suggested Remedy**

Change "The maximum test fixture insertion loss shall meet the values determined using Equation (85-35). The values for the coefficients b1, b2, b3 b4 and e are given in Equation (85-16)" to **"**

The reference test fixture insertion loss shall meet the values determined using Equation (85-35).

Make Equation 85-35 match the loss of the MCB in 86A

Also add a sentence at the end of the end of 85.10.9

"The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements."

Also state whether the connector loss is included in the test fixture loss or not.

**Response**

ACCEPT IN PRINCIPLE.

Make Equation 85-35 match the loss of the MCB in 86A-5.

The cable assembly test fixture is not consistent with Eq 86A-5. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

**Suggested Remedy**

Please use Eq 86A-5

ACCEPT IN PRINCIPLE.

See response comment #43.
Comment Type | TR  | Comment Status | A
---|---|---|---

Hardware contact definitions in Table 85-12 violate the QSFP connector specification of SFF-8436: the table requires that contact 27 be open in the case of a copper module, while the QSFP spec defines this contact as module presence pin and requires it to be grounded in the module. As a result of this discrepancy, passive QSFP copper cables created for all other standards using SFF-8436 will not be interoperable with 40GE. Conversely, if the connector is pinned out per table 85.11, the cable will not as a general rule be able to be used in Infiniband and other equipment already deployed in the field. While not strictly a problem from IEEE point of view, I believe this incompatibility will have negative impact on the broad market potential and future adoption of this standard. In addition, electronic keying is also required for CR10 and is currently missing, and defining it along the lines of table 85-12 causes even more severe discrepancy with the CXP specification (see my next comment).

Suggested Remedy

The entire section 85.11.1.1.1 as currently written needs to be deleted. There does not appear to be a way to define electronic keying without violating the QSFP spec. The reasonable solution is to use the SFF-8436 management interface, which has provisions for identifying the module as a copper or an optical module. Also, it is obvious that everyone will end up using the management interface anyway, because it is de facto industry standard and it does the job. If management interface definition is beyond the scope of the project, then we could either make an informative statement referencing the SFF-8436 management interface; or we could make a statement along the lines of "Electronic keying shall be used in order to enable detection of Style-1 plug connector versus fiber module or no module present. The details of implementation of such keying are beyond the scope of this standard". This would prompt people to use the management interface without calling it out, or it would enable proprietary/custom designs along the lines of table 85-12.

Response | Response Status | C
---|---|---

ACCEPT IN PRINCIPLE.

The basis for Table 85-12 requires a distinction between a module and a direct attach plug. If this distinction is clear in SFF-8436, as I had assumed when creating the table, Table 85-12 is not in conflict with SFF-8436. Given the number of similar comments the distinction is not clear or not made.

Delete: sub-clause 85.11.1.1.1
Add: 85.11.4 Electronic keying

Electronic keying can be used to enable the detection of Style-1 40GBASE-CR4 MDI connectors or 100GBASE-CR10 MDI cable assembly plugs versus fiber modules or no modules present. Specifications of electronic keying are beyond the scope of this standard.
<table>
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<tr>
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<th>Page</th>
<th>L</th>
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<td>TR</td>
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<td>Ghiasi, Ali Broadcom</td>
<td>Connector IEC number is missing Please add connector IEC number, if not available then use the SFF number</td>
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<td>R</td>
<td>Ghiasi, Ali Broadcom</td>
<td>Contact 27 is not listed in table 85-11 Please add all 38 contacts to table 85-11</td>
<td>REJECT. See response comment#2.</td>
<td>C</td>
<td>TR</td>
<td>R</td>
<td>Ghiasi, Ali Broadcom</td>
<td>Contact 27 is not listed in table 85-11 Please add all 38 contacts to table 85-11</td>
<td>REJECT. See response comment#2.</td>
<td>C</td>
<td>TR</td>
<td>R</td>
<td>Ghiasi, Ali Broadcom</td>
<td>Contact 27 is not listed in table 85-11 Please add all 38 contacts to table 85-11</td>
<td>REJECT. See response comment#2.</td>
<td>C</td>
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<tr>
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<td>274</td>
<td>3</td>
<td>#36</td>
<td>T</td>
<td>A</td>
<td>Moeller, Merrick Cinch Connectors Inc.</td>
<td>Referring Table 85-12. Style-1 contact 27 is designated to state 1 for copper module presence. This contact is defined in SFF-8436 as ModPrsL, and fixed to state 0 for passive copper assemblies. Contact 28 is defined as IntL, which is a don't care state for passive interconnects, but may be used in other instances. Remove Table and text. Use management protocol based on SFF-8436.</td>
<td>ACCEPT IN PRINCIPLE. [Editor's Note: Commenter submitted a TR comment. Changed to comment type: T since the commenter is not in P802.3ba ballot group]See response comment#2.</td>
<td>C</td>
<td>T</td>
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<td>DiMinico, Christopher MC Communications</td>
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<td>Change compatibility.</td>
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<td>TR</td>
<td>Some of the contacts shown in the MDI diagram are not listed in table 85-11</td>
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</table>

**Comment:**

Spelling assignments

**Suggested Remedy:**

Change assignments to assignments

**Response:**

ACCEPT. See suggested remedy

---

**Comment:**

Some of the contacts shown in the MDI diagram are not listed in table 85-11

**Suggested Remedy:**

Please include all contacts

**Response:**

REJECT. The 100GBASE-CR10 MDI supports 84 connections only the transmitter and receiver contact assignments are specified. The other pins are not used in the scope of this specification.

**Comment:**

References to clauses not in the draft should be blue

**Suggested Remedy:**

Page 277, line 46, "14.7" should be blue
Page 278, line 11, "Clause 21" should be blue
Page 278, line 44, "Clause 21" should be blue

**Response:**

ACCEPT. See suggested remedy

---

**Comment:**

Spelling interpret

**Suggested Remedy:**

Change interpret to interpret

**Response:**

ACCEPT. See suggested remedy

---

**Comment:**

Unnecessary hyphen

**Suggested Remedy:**

Change 'The-' to 'The'

**Response:**

ACCEPT. See suggested remedy

---

**Comment:**

Several references in Clause 85 that should be cross-references are not.

**Suggested Remedy:**

Make the following references to other places in the draft cross-references.

Page 240, line 44, "80.3"
Page 244, line 20, "85.10"
Page 246, line 39, "85.7.4"
Page 247, line 45, "45.2.1.7.4" (not blue)
Page 247, line 53, "45.2.1.7.5" (not blue)
Page 251, line 27, "85.7.12"
Page 252, line 3, "83.5.10" (not blue)
Page 252, line 34, "83.5.10"
Page 253, line 42, "85.7.3.2.3"
Page 257, line 28, "85.10"

**Response:**

ACCEPT. See suggested remedy

---

**Comment:**

Spelling interpret

**Suggested Remedy:**

Change interpret to interpret

**Response:**

ACCEPT. See suggested remedy
Comment Type: TR  Comment Status: R

The response to D2.1 comment 37 (Exchange of DME frames is unnecessary) shows a misunderstanding by the BRC. Response says "include backward compatibility with CX4". CX4 doesn't use and can't understand DME frames, so compatibility with CX4 is achieved by Parallel Detection. Response says "Suggested remedy inconsistent with ... 802.3ap electricals": this isn't about electricals but about a protocol. DME frames are used in Backplane Ethernet where there is a choice of DME-aware PMD types. On a front-side port, there isn't. There is 10GBASE-CX4 and 40GBASE-CR4. You don't need DME frames to tell them apart. You have Parallel Detection to detect CX4. So you can use it to detect CR4 also.

The unnecessary burden, apart from the obvious extra complexity of an unnecessary protocol, is that DME frames run at 312.5 MBd, 1/33 of the normal 10G rate, so a normal 10G CDR won't lock to this.

SuggestedRemedy

Add text in Clause 85 saying that 40GBASE-CR4 and 100GBASE-CR10 can use Parallel Detection. This is in line with the backward compatibility with CX4 and baseline "Parallel detection function to detect legacy 10GBASE-CX4 PHYs".

If you wish, advertise FEC ability in the Training frame.

Response  Response Status: W

REJECT.

AN uses DME signaling to exchange link partner abilities and to negotiate FEC capability.

The commenter has not provided a sufficiently complete proposal for replacement of DME with parallel detection.

Comment Type: TR  Comment Status: A

This paragraph (85.7.1) says that TP2 is at the output end of the mated connector and defines this as TP2. Table 85-4 says that the specifications are at TP2, but 85.8.3.5 says that the measurements are at the output of the test fixture.

SuggestedRemedy

Change "The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2."

In Figure 85-5 Show the connector and PCB traces to the left of TP2 or TP3. To clarify things make the Test fixture impedance 85.8.3.6 and Test fixture insertion loss 85.8.3.7 sub-sections of 85.8.3.5.

Response  Response Status: C

ACCEPT IN PRINCIPLE.

(1)In Figure 85-5 illustrate Figure 85-11 TP2 or TP3 test fixture attached to TP2 or TP3 test points.

(2)Change: The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2.

To: The electrical transmit signal is defined at TP2.

Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2 utilizing the test fixture specified in 85.8.3.5.
IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

Comment Type E Comment Status A
"Amplitude peak-to-peak" should be "Amplitude peak-to-peak (max)"

Suggested Remedy
make indicated change

Response Response Status C
ACCEPT IN PRINCIPLE.

See response comment #222.

Comment Type T Comment Status A
Collect up the transmit parameters derived from the wave form analysis into the table. They are sprinkled in the text.

Suggested Remedy
Table 85-4
Under Transmitted wave form add lines

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>min amplitude (linear fit), &quot;p&quot;</td>
<td>5.8.3.3 0.24 V</td>
</tr>
<tr>
<td>normalized error (linear fit), &quot;e&quot;</td>
<td>5.8.3.3 0.037</td>
</tr>
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<td>abs coefficient step size</td>
<td>5.8.3.3.1 min 0.0083 max 0.06</td>
</tr>
<tr>
<td>minimum precursor fullscale range</td>
<td>85.8.3.3.2 1.54</td>
</tr>
<tr>
<td>minimum post cursor fullscale range</td>
<td>85.8.3.3.2 4</td>
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</tbody>
</table>

Response Response Status C
ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force]
Editor given license to implement suggested remedy with changes to values as approved in other comments.

Comment Type TR Comment Status A
No test method is defined how to measure "Total Jitter Excluding Data Dependent Jitter"

Suggested Remedy
A suggested method is given below:
Total jitter is measured with PRBS31 (pattern 3) at BER of 10^-12. Data Dependent jitter is measured with PRBS9 based on method given in 85.8.3 with following definition
DDJ=max(dt1, dt2, ... , dt256) - min(dt1, dt2, ... , dt256).
Section 85.8.3 would need to be updated or the other option is to create a standalone section.

Total Jitter excluding DDJ = TJ - DDJ

Response Response Status C
ACCEPT IN PRINCIPLE. [Editor's note removed mistyped special character from subclause field. Changed to 85.8.3]
Response: Measure Total jitter at BER 1E-12 per 83A.5.1.=TJ
Measure DDJ with PN9=DDJ
Total Jitter excluding Data Dependent Jitter = TJ - DDJ

Editor given license to implement response incorporating comment #218 in response.

Comment Type TR Comment Status A
Amplitude pk-to-pk (line 19) and Far-end transmit output noise (line 22-23) are max values and are not specified

Suggested Remedy
Add (max) after those parameters.

Response Response Status C
ACCEPT.
See suggested remedy and remedy to comment #87
<table>
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<td>SuggestedRemedy</td>
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<tr>
<td>Give the data dependent jitter (DDJ) definition: DDJ is the zero-crossing time deviation referenced to the ideal bit clock timing derived from an averaged differential waveform where uncorrelated signal components have been removed.</td>
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<tr>
<td>ACCEPT IN PRINCIPLE.</td>
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<tr>
<td>Expand footnote c in Table 85-4 to add definition for DDJ.</td>
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<tr>
<td>DDJ is a jitter component where jitter that is not correlated to the data pattern has been removed.</td>
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<tr>
<td>Resolve with comment#98.</td>
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<td>Tx jitter testing method and procedure is not defined.</td>
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<td>See response to comment#98</td>
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<tbody>
<tr>
<td>SuggestedRemedy</td>
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<tr>
<td>Needs to give the Tx jitter testing method, including Tx equalization setting and receiver CDR condition.</td>
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<td>Response</td>
<td>Response Status</td>
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<td>ACCEPT.</td>
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<tbody>
<tr>
<td>&quot;Total jitter excluding DDJ&quot; is a confusing and self-inconsistent name. Total jitter is not &quot;total&quot; anymore if DDJ is removed.</td>
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<tr>
<td>SuggestedRemedy</td>
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<tr>
<td>Change &quot;Total jitter excluding DDJ&quot; to uncorrelated total jitter (uTJ).</td>
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<tr>
<td>Proposed Response</td>
<td>Response Status</td>
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</tr>
<tr>
<td>REJECT.</td>
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<tr>
<td>This comment was WITHDRAWN by the commenter.</td>
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<tr>
<td>Total jitter excluding DDJ sufficiently characterizes the parameter.</td>
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<tbody>
<tr>
<td>SuggestedRemedy</td>
<td></td>
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<tr>
<td>DDJ should be specified. With the TJ being uncorrelated TJ (namely TJ with DDJ removed) in D2.2. DDJ is now not bounded and this needs to be fixed.</td>
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<td>Response</td>
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<tr>
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</table>
Transmitter common mode output return loss is missing

Suggested Remedy:
The reference impedance for common mode return loss measurement shall be 25 ohms

- Return loss \( \geq -7 + 1.6 \times f \) from \(-0.05\) to \(2.5\) GHz
- \(-3\) from \(2.5\) to \(10\) GHz

Proposed Response:

REJECT.

This comment was WITHDRAWN by the commenter.

Common-mode return loss specified; see Table 85-4 - Common-mode output return loss (min.).

-----

Special character

Suggested Remedy:
Please remove the special character at end of line

Proposed Response:

ACCEPT.

-----

suggest rewording that attention is drawn to the far-end transmitter output noise

Suggested Remedy:
change

- The measured RMS deviation for the low loss cable assembly shall meet

Proposed Response:

ACCEPT.

Change: The measured RMS deviation for the low loss cable assembly shall meet the values determined using Equation (85-2).

To: For the low loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85-2).

Change: The measured RMS deviation for the high loss cable assembly shall meet the values determined using Equation (85-3).

To: For the high loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85-3).
### IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

#### Draft 2.2 Comments

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<td>85.8.3.2</td>
<td>250</td>
<td>29</td>
<td>159</td>
</tr>
</tbody>
</table>

**Dudek, Mike**  QLogic

**Comment Type**  TR  **Comment Status**  A

The transmitter noise will add to the ICN in an RMS fashion, not a linear fashion.

**SuggestedRemedy**

- Change Equation 85-2 and 85-3 to use RMS addition  ($\sqrt{a^2 + b^2}$) not linear ($a + b$)

**Response**  

Accept IN PRINCIPLE.

See response comment #50.

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</table>

**Healey, Adam**  LSI Corporation

**Comment Type**  T  **Comment Status**  A

It is more appropriate to define RMSldev as the square-root of the sum of the square values $\sigma_l^2$ and $2^2$. Similarly for the RMShdev.

**SuggestedRemedy**

- Update Equations (85-2) and (85-3) accordingly. The far-end transmit output noise requirements may need to be updated accordingly.

**Response**  

Accept IN PRINCIPLE.

Update Equations (85-2) and (85-3) accordingly. The far-end transmit output noise requirements may need to be updated accordingly.

**SuggestedRemedy**

- Define RMSldev as the square-root of the sum of the square values $\sigma_l^2$ and $2^2$ in equation (85-2).
- Define RMSldev as the square-root of the sum of the square values $\sigma_h^2$ and $1^2$ in equation (85-3).

<table>
<thead>
<tr>
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<th>SC</th>
<th>P</th>
<th>L</th>
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<td>85</td>
<td>85.8.3.2</td>
<td>250</td>
<td>3</td>
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</tbody>
</table>

**Ghiasi, Ali**  Broadcom

**Comment Type**  ER  **Comment Status**  A

The sentence does not read well "The far-end transmitter output noise is noise in .."

**SuggestedRemedy**

- Suggested: "The far-end transmitter output noise is the summ of this noise in .."

**Response**  

Accept IN PRINCIPLE.

Accept IN PRINCIPLE.

**SuggestedRemedy**

- Replace: "The far-end transmitter output noise is noise in addition to the cable assembly integrated crosstalk noise (ICN)."

With: The far-end transmitter output noise is an additional source of noise to the cable assembly's integrated crosstalk noise (ICN).

<table>
<thead>
<tr>
<th>Cl</th>
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</thead>
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<tr>
<td>85</td>
<td>85.8.3.3</td>
<td>251</td>
<td>47</td>
<td>52</td>
</tr>
</tbody>
</table>

**Healey, Adam**  LSI Corporation

**Comment Type**  TR  **Comment Status**  A

The transmitter output waveform requirements do not address the case where the transmitter is requested to INITIALIZE per 72.6.10.4.2.

**SuggestedRemedy**

- Insert a new subclause under 85.8.3.3 with the heading "85.8.3.3.X Coefficient initialization" and containing the following text:

> "When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72-5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be ... 2.57 +/- 10%. These requirements apply upon the assertion a coefficient status report of "updated" for all coefficients."

**Response**  

Accept IN PRINCIPLE.

See suggested remedy.

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
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<td>85.8.3.3</td>
<td>251</td>
<td>47</td>
<td>52</td>
</tr>
</tbody>
</table>

**D'Ambrosia, John**  Force10 Networks

**Comment Type**  E  **Comment Status**  A

There is a reference to the cable assembly ICN prior to its introduction.

**SuggestedRemedy**

- Add reference to 85.10.8 in first sentence of 85.8.3.2.

**Response**  

Accept IN PRINCIPLE.

See suggested remedy.

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
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<td>85.8.3.3</td>
<td>251</td>
<td>36</td>
<td>51</td>
</tr>
</tbody>
</table>

**Healey, Adam**  LSI Corporation

**Comment Type**  TR  **Comment Status**  A

The far-end transmitter output noise is noise in addition to the cable assembly's integrated crosstalk noise (ICN).

**SuggestedRemedy**

- Correct the mapping from qi to the normalized coefficients c(n) by replace all instances of "Dw" with "Dp".

**Response**  

Accept IN PRINCIPLE.

See suggested remedy.
Comment Type: T  Comment Status: A

pulse amplitude out Tx at TP2 is defined but DC gain is not. This could allow slow, high amplitude Tx, which is hard to equalize, to pass.

Suggested Remedy
Specify Tx DC amplitude of Tx as "sum of linear fit pulse from step 3 divided by M from step 3" specify that DC amplitude is greater than 0.375 and less than 0.6 and that the peak of the linear fit pulse from step 3 shall be greater than 0.60*DC amplitude.

Response  Response Status: C
ACCEPT IN PRINCIPLE.

Specify Tx DC amplitude of Tx as "sum of linear fit pulse from step 3 divided by M from step 3" specify that DC amplitude is greater than [0.34 v] and less than 0.6 v and that the peak of the linear fit pulse from step 3 shall be greater than [0.63]*DC amplitude.

Editor given license to implement in procedure.

Comment Type: TR  Comment Status: A

Wrong reference (85.7.3.2.3 doesn't exist.)

Suggested Remedy
Change 85.7.3.2.3 to 85.8.3.3.3.

Response  Response Status: C
ACCEPT. See suggested remedy.
Cl 85 SC 85.8.3.4 P 255 L 9 # 89
Moore, Charles Avago Technologies

Comment Type T Comment Status D
Normative insertion loss spec between TP0 and TP2 and TP3 and TP5 is no longer needed

Suggested Remedy
Delete 85.8.3.4 including Equation 85-14 and Figure 85-A.4.

In 85-A.5, replace "Equation(85-14)" on line 18 and line 33 to "Equation (85-A-1)"

In equation 85-A-3 and equation 85-A-4, delete term *(2 x ILMatedTF(f))

or

Move 85.8.3.4 including Equation 85-14 and Figure 85-A-5 to Annex 85-A, most likely 85-A.4

If Figure 85-A-4, use a linear frequency scale.

Proposed Response Response Status Z
REJECT.

This comment was WITHDRAWN by the commenter.

The 85.8.3.4 Insertion loss basis is tied to supported trace lengths identified in D2.1 comment#96 resolution using gustlin_04_0709.

Cl 85 SC 85.8.3.5 P 254 L 10 # 226
Palkert, Tom Xilinx/Luxtera

Comment Type TR Comment Status A
PPI and CR will share a common interface when using the Type 1 connector. Therefore the test fixtures should have the same parameters.

Suggested Remedy
The test fixture parameters in Annex 86-A 5.1.1 should either be duplicated here or referenced.

Response Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #43

Cl 85 SC 85.8.3.5 P 256 L 1 # 138
DiMinico, Christopher MC Communications

Comment Type E Comment Status A
Provide consistency with test fixture representation and labeling in Figure 85-5 with 85.10.10 Mated test fixtures Figure 85-11.

Suggested Remedy
See comment

Response Response Status C
ACCEPT IN PRINCIPLE.
See suggested remedy comment#158

Cl 85 SC 85.8.3.5 P 256 L 18 # 111
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A
Figure 85-5 is not helpfull and conflicts with definition in 85.8.3.7 and implies the loss include 100 nF and scope front end

Suggested Remedy
Change Figure 85-5 title to "Example TP2 or TP3 Measurement Setup"

Response Response Status C
ACCEPT IN PRINCIPLE.
See response comment#168.

Remove TP3 form figure 85-5
2. Refer to mated test fixture illustration for TP-TF in 85-11 for Rx.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

Cl 85 SC 85.8.3.5 Page 40 of 64
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A
Figure 85-5 is not helpfull and conflicts with definition in 85.8.3.7 and implies the loss include 100 nF and scope front end

Suggested Remedy
Change Figure 85-5 title to "Example TP2 or TP3 Measurement Setup"

Replace TP2 or TP3 with MDI

Add a box between MDI and bias connection with RF ports, name this box Transmit/Receive Test Fixtrue

Added lable to the RF ports "TP2/TP3"

Response Response Status C
ACCEPT IN PRINCIPLE.
See response comment#158

Cl 85 SC 85.8.3.5
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A
Figure 85-5 is not helpfull and conflicts with definition in 85.8.3.7 and implies the loss include 100 nF and scope front end

Suggested Remedy
Change Figure 85-5 title to "Example TP2 or TP3 Measurement Setup"

Response Response Status C
ACCEPT IN PRINCIPLE.
See response comment#168.

Remove TP3 form figure 85-5
2. Refer to mated test fixture illustration for TP-TF in 85-11 for Rx.
There are multiple equations and graphs in the clause that are functions of frequency. Most use GHz, some use MHz, Hz also occurs. It would be good to standardize them all. This specific instance obviously applies to line 42 as well. Other instances are this page lines 48 and 49 with page 257 lines 1 to 6 and related change on page 267 lines 33 and 38, and related changes in 85A page 422 line 40 and page 423 line 1 Page 262 lines 44 to 52 Figure 85-7

Suggested Remedy
Change all the equations and graphs covering the GHz range to use GHz as listed in the comment (no technical change. Also do the same in Annex 85A (page 423 lines 30 and 53), (page 424 lines 43 and 46 and fig 85A-1)

Proposed Response
REJECT.

This comment was WITHDRAWN by the commenter.

Some of the equations in Clause 85 introduce an extra variable name that is not used elsewhere. For example Equation 85-16 starts:

\[ \text{ILtf}(f) \leq \text{ILtfmax}(f) = (0.054) \ldots \]

The ILtfmax(f) variable is not referred to anywhere in the draft and only serves to complicate the equation. Where there are limit lines for both max and min for the same parameter (e.g., Equations 85-23 and 85-24) and the extra variables e.g. ILDmin(f) and ILDmax(f) are used elsewhere, they should be retained. Also applies to Equations 85-35, 85A-3 and 85A-4

Suggested Remedy
In 85-16 change "ILtf(f) \leq \text{ILtfmax}(f) = (0.054)\ldots" to "ILtf(f) \leq (0.054)\ldots"
In 85-35 change "ILCATF(f) \leq \text{ILCATFmax}(f) = (0.029)\ldots" to "ILCATF(f) \leq (0.029)\ldots"
In 85A-3 change "ILCh(f) \leq \text{ILDmax}(f) = \text{ILDmax}(f)" to "ILCh(f) \leq \text{ILDmax}(f)"
In 85A-4 change "ILCh(f) \leq \text{ILChmax}(f) = (0.05)\ldots" to "ILCh(f) \leq (0.05)\ldots"

Response
ACCEPT.
See suggested remedy

The cable assembly test fixture is not consistent with Eq 86A-4. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

Suggested Remedy
Please use Eq 86A-4

Response
ACCEPT IN PRINCIPLE.
85.8.3.7 is Test fixture insertion loss. See comment #43.

The test fixture insertion losses aren't maxima, they are reference losses. See text at 86A.5.1.1.

Suggested Remedy
Change "maximum" to "reference" here and in 85.10.9.

Response
ACCEPT IN PRINCIPLE.
See response to comment #167, comment #177.
### Comment

**Comment Type**: TR  **Comment Status**: A

Results will vary depending on the fixture insertion loss and 85.8.3.7 gives a maximum test fixture insertion loss (and no minimum). We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A for commonality. Note that the PCB loss of the test fixture of clause 86A is what was used to derive the budget in Healey_03a_0709 (which doesn't match what is here). We should also specify exactly what is included in the insertion loss.

**Suggested Remedy**

Change the Test Fixture insertion loss to a reference insertion loss (not just max) and use the same equations as 86A. Also add a sentence at the end of the Test Fixture insertion loss "The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements."

State in 85.8.3.6.7 that the connector loss is not included in the test fixture insertion loss.

**Response**

**Response Status**: C  **Proposal Response Status**: Z

ACCEPT IN PRINCIPLE.

Delete: The maximum test fixture insertion loss shall meet the values determined using Equation (85-16).

Add: The reference test fixture PCB insertion loss is given in Equation (85-16). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.

Make Equation 85-16 match the loss of the HCB in 86A-4 from 0.05 GHz to 10 GHz.

---

### Comment

**Comment Type**: TR  **Comment Status**: D

It is very difficult to read the graph with log scale

**Suggested Remedy**

Please use linear freq scale

**Proposed Response**

**Response Status**: Z

REJECT.

This comment was WITHDRAWN by the commenter.

---

### Comment

**Comment Type**: T  **Comment Status**: A

85.3.4.7’s "Insertion loss TP0 to TP2 or TP3 to TP5" is (above 200 MHz) consistent with the minimum SDD21 of host PCB, connector and HCB in 86A-6. The mated test fixtures insertion loss limits of 85.10.10.1 are consistent with the through response (SDD21) limits of mated HCB-MCB in 86A.5.1.1.2. Yet the test fixture insertion loss of 85.8.3.7 and the cable assembly test fixture insertion loss of 85.10.9 do not agree with the reference through responses (SDD21) of HCB and MCB in 86A.5.1.1.1. 85.8.3.7 and 85.10.9 use scaled backplane Amax while 86A.5.1.1.1 is based on experience with actual compliance boards. Because compliance boards are not backplanes (e.g. may use PTFE dielectric rather than FR4), the equations in 86A.5.1.1.1 are preferable.

**Suggested Remedy**

Change equations 85-16 and 85-35 so they are consistent with 86A-4 and 86A-5 respectively.

**Response**

**Response Status**: C  **Proposal Response Status**: Z

ACCEPT IN PRINCIPLE.

See response to comment #43.
Comment Type T  Comment Status A
Receiver interference tolerance test is incomplete.

SuggestedRemedy
Proposed wording will be presented at a meeting.

Response  Response Status C
ACCEPT IN PRINCIPLE.
Replace "85.8.4.2 Receiver interference tolerance test at TP3" with moore_01a_0909.pdf revision to moore_01_0909.pdf.

Comment Type T  Comment Status A
Comment #138 against Draft 2.1 was incorrectly implemented; a4 for test 1 values should be a4 = 0.03. See response to comment#138 Draft 2.1 - (2) Limits given by polynomial coefficients (low loss a1=2.15,a2=-.78,a4=0.03) (high loss a1=6.04,a2=0.94,a4=0.08).

SuggestedRemedy
Change polynomial coefficients a4 from 0.3 to 0.03).

Response  Response Status C
ACCEPT. See suggested remedy.

Comment Type TR  Comment Status A
The test cables attenuation for the interference tolerance test should have a specified value (not just a max value).

SuggestedRemedy
Delete the words "maximum allowable".

Response  Response Status C
ACCEPT IN PRINCIPLE. See response comment#91.
We should be more explicit and normative about the location of the AC coupling capacitors. 

**Suggested Remedy**
- Replace "AC-coupling is considered to be part of the receive function for Style-2 40GBASE-CR4 connectors." with "AC-coupling shall be included in the receive function for Style-2 40GBASE-CR4 connectors."

Add an extra sub-clause in 85.10 (suggest at 85.10.9) Heading "Cable Assembly AC coupling."

"Cable assemblies for 40GBASE-CR4 using style 1 connectors and 100GBASE-CR10 shall include AC coupling capacitors see 85.11.1.1.2 and 85.11.3. Cable assemblies for 40GBASE-CR4 using style 2 connectors do not require AC coupling."

**Response**
- Accept in principle.

Replace: "The 40GBASE-CR4 and 100GBASE-CR10 receiver shall be AC-coupled to the cable assembly to allow for maximum interoperability. AC-coupling is considered to be part of the receive function for Style-2 40GBASE-CR4 connectors. For Style-1 40GBASE-CR4 and 100GBASE-CR10 plug connectors the receive lanes are AC-coupled; the coupling capacitors are contained within the plug connectors."

With: "The 40GBASE-CR4 and 100GBASE-CR10 receivers are AC-coupled. AC-coupling shall be part of the receive function for Style-2 40GBASE-CR4 connectors. For Style-1 40GBASE-CR4 and 100GBASE-CR10 plug connectors the receive lanes are AC-coupled; the coupling capacitors shall be within the plug connectors."

In 85.11.3 100GBASE-CR10 MDI AC-Coupling and 85.11.1.1.2 Style-1 AC-coupling After: For ... plug connectors the receive lanes are AC-coupled; the coupling capacitors are contained within the plug connectors...add reference to 85.8.4.6. delete paragraphs below and notes.

**Update:** PICS
The definition of TP1 has been adjusted (per Healey_03a_0709) to be at the input to the
cable test fixture so it does not include all the PCB, resulting in an ambiguity. The loss
specified on line 33 matches the loss we have in the budget for TP0 to TP1 (not for the
complete PCB) but does not match the loss in equation 85A-1 which is only 5.186 dB at
Nyquist. Also Clause 86A allows a max 2x4.4 dB for the total PCB loss on the assumption a
host might use a lower loss connector.

SuggestedRemedy
Either
1. Delete "(ie the maximum insertion loss between TP0-TP1 and TP4-TP5)." and change
the multiplier in equation 85A-1 from 0.3 to 0.508.
2. Change the paragraph to "The maximum insertion loss allocation for the transmitter plus
receiver differential controlled impedance printed circuit boards for each differential lane
between TP0-TP1 and TP4-TP5 is determined using Equation (85A-1) and the coefficients b1
through b4 are given in Equation (85-16). The maximum insertion loss allocation for the
transmitter and receiver differential controlled impedance printed circuit boards between
these test points is 7 dB at 5.15625 GHz. Note that there is an additional 1.4 dB allowance
in the PCB loss for the equivalent PCB loss between TP1 and TP4 and the connectors."
Change the multiplier in equation 85A-1 from 0.3 to 0.405

Response
ACCEPT IN PRINCIPLE.

Change: The maximum insertion loss allocation for the transmitter and receiver differential
controlled impedance
printed circuit boards for each differential lane (i.e., the maximum insertion loss between
TP0-TP1 and TP4-TP5) are determined using Equation (85A-1) and the coefficients b1 through b4 are given in
Equation (85-16). The maximum insertion loss allocation for the transmitter and receiver differential
controlled impedance
printed circuit boards is 7 dB at 5.15625 GHz

TO: Based on 85.8.3.4 insertion loss TP0 to TP2 or TP3 to TP5 and an assumed connector
loss of 1.74 dB,
the maximum insertion loss allocation for the transmitter and receiver differential controlled
impedance
printed circuit boards for each differential lane (i.e., the maximum value of the sum of the
insertion losses from TP0 to the MDI host receptacle and from TP5 to the MDI host
receptacle are determined using Equation (85A-1) and the coefficients b1 through b4 are
given in Equation (85-16). The maximum insertion loss allocation for the transmitter and receiver differential
controlled impedance
printed circuit boards is 7 dB at 5.15625 GHz
Cl 85A SC 85A.4 P 422 L 36 # 109

Ghiasi, Ali Broadcom

Comment Type TR Comment Status D

The channel loss budget has been changed during D2.1 but this equation was not adjusted accordingly.

Suggested Remedy

Mated response loss 6.5 dB at 5.16 GHz, less 1.25 dB for HCB, less 0.5 dB for connector, leaves 4.75 dB loss per end.
The 4.75 dB host PCB loss is based on assumption the connector has loss of 0.5 dB, higher loss connector require reducing channel PCB loss.

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

The maximum channel insertion loss of 24.44 dB is consistent with D2.1 comment#96 resolution.

where

ILCh(f) = ILChmax(f) = 17.04 + (2 × 6.5) - (2 × 2.8) = 24.44 dB

Cl 85A SC 85A.4 P 422 L 43 # 137

Diminico, Christopher MC Communications

Comment Type E Comment Status A

Spelling insertion

Suggested Remedy

Change insertion to insertion

Response Response Status C

ACCEPT.

See suggested remedy.
Cl 85A  SC 85A.4  P 422  L 51  # 103
Ghiasi, Ali  Broadcom

Comment Type: TR  Comment Status: A
Min loss Eq 85A-2 is not consistent with mated channel loss

Suggested Remedy
The mated min channel loss = 2.08
less min HCB loss = 1.04 dB
Min connector loss = 0.3 dB
Result in 0.74 dB loss per end

Response  Response Status: C
ACCEPT IN PRINCIPLE.
Change (0.103) to scale equation (85A-2) to 2*(0.67) dB @ 5.515626 GHz.

Cl 85A  SC 85A.5  P 421  L 14  # 58
Healey, Adam  LSI Corporation

Comment Type: E  Comment Status: A
"is the frequency in MHz" should not be italicized.

Suggested Remedy
Correct two occurrences in this subclause, as well as an occurrence in 85A.7.

Response  Response Status: C
ACCEPT.
See suggested remedy

Cl 85A  SC 85A.5  P 423  L 15  # 59
Anslow, Peter  Nortel Networks

Comment Type: E  Comment Status: A
For equations 85A-3, 85A-4 and 85A-5 the phrase "is the frequency in MHz" is shown in italic font. This should be normal font.

Suggested Remedy
For equations 85A-3, 85A-4 and 85A-5 change the phrase "is the frequency in MHz" to normal font.

Response  Response Status: C
ACCEPT.
See comment#58
<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Dudek, Mike QLogic</th>
<th>Response Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>A</td>
<td>It would help understanding if IL(Camax) were better defined.</td>
<td>C</td>
<td>This comment was WITHDRAWN by the commenter.</td>
</tr>
</tbody>
</table>

**Suggested Remedy**

- Change IL(Camax) definition to "The maximum cable assembly insertion loss as measured with the cable assembly test fixtures using Equation (85-19)"

**Response**

- ACCEPT IN PRINCIPLE.
- Change IL(Camax) definition to "The maximum cable assembly insertion loss using Equation (85-19) defined between TP1 and TP4."

<table>
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<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Dudek, Mike QLogic</th>
<th>Response Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>D</td>
<td>Assuming my other comments are accepted to change to a reference loss for the test fixtures. The IL(mated) definition should be changed from maximum insertion loss to reference insertion loss.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**

- Change the definition of IL(mated) to "The reference insertion loss of the mated test fixture using equation (85-37)"

**Response**

- ACCEPT IN PRINCIPLE.
- Change IL(mated) definition to "The reference insertion loss of the mated test fixture using equation (85-37)"

---

Despite having references for the independent test fixture insertion losses it's good to limit the insertion loss of the actual mated test fixture.
<table>
<thead>
<tr>
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<tr>
<td>T</td>
<td>A</td>
<td>Delete the text between lines 21 and 35. As an alternative that would perhaps have more interest consider changing this section to minimum channel loss.</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>Change Equation (85A-4) to Equation (85A-4): ILCh(f) = ILChmax(f) = (0.05 x ILCamax(f)) x (2 x ILHost(f)) - (2 x ILMatedTF(f))</td>
<td></td>
<td></td>
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<td>T</td>
<td>A</td>
<td>Change (85A-4) to (85A-4): ILCh(f) = ILChmax(f) = (0.05 x ILCamax(f)) x (2 x ILHost(f)) - (2 x ILMatedTF(f))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>Add note the cable loss of 24.44 dB is when ILmated loss is 2.4 dB, if ILmated loss is less than 2.4 dB then ILCh shall be reduced by the same amount</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>The channel, TP0 to TP5 can not have the same ILD as the cable assembly. If we are going to keep with the RL budgets from D2.2 then this number will need to be increased to allow for interactions between the hosts and the cable.</td>
<td>REJECT. [Editor's note: Late comment for consideration by the Task Force]</td>
<td>C</td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.</td>
<td>ACCEPT.</td>
<td>C</td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>For the cable assembly, specifications for insertion loss to crosstalk ratio were replaced with integrated crosstalk noise requirements. It seems that the channel requirements should follow suit.</td>
<td></td>
<td></td>
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<tr>
<td>T</td>
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<td>Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.</td>
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<td>C</td>
</tr>
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</table>

**Comment Status**: D/dispatched /A/accepted R/rejected

**Response Status**: O/open W/written C/closed U/unsatisfied Z/withdrawn

**Sort Order**: Clause, Subclause, page, line

**Type**: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

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**IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments**

**WG 2nd recirculation ballot**

**Draft 2.2 Comments**

**Comment Type**

<table>
<thead>
<tr>
<th>Comment Type</th>
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<td></td>
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<tr>
<td>T</td>
<td>A</td>
<td>Change (85A-4) to (85A-4): ILCh(f) = ILChmax(f) = (0.05 x ILCamax(f)) x (2 x ILHost(f)) - (2 x ILMatedTF(f))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>Add note the cable loss of 24.44 dB is when ILmated loss is 2.4 dB, if ILmated loss is less than 2.4 dB then ILCh shall be reduced by the same amount</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>The channel, TP0 to TP5 can not have the same ILD as the cable assembly. If we are going to keep with the RL budgets from D2.2 then this number will need to be increased to allow for interactions between the hosts and the cable.</td>
<td>REJECT. [Editor's note: Late comment for consideration by the Task Force]</td>
<td>C</td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.</td>
<td>ACCEPT.</td>
<td>C</td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>For the cable assembly, specifications for insertion loss to crosstalk ratio were replaced with integrated crosstalk noise requirements. It seems that the channel requirements should follow suit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.</td>
<td>ACCEPT.</td>
<td>C</td>
</tr>
</tbody>
</table>

**Comment Status**: D/dispatched /A/accepted R/rejected

**Response Status**: O/open W/written C/closed U/unsatisfied Z/withdrawn

**Sort Order**: Clause, Subclause, page, line

**Type**: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
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<th>Comment Type</th>
<th>Comment Status</th>
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</tr>
</thead>
<tbody>
<tr>
<td>85A</td>
<td>SC 85A.8</td>
<td>424</td>
<td>9</td>
<td>T</td>
<td>A</td>
<td>Misek, Brian Avago Technologies</td>
<td>This whole section seems to be not in sync with methods agreed to in the last meeting and should be expressed in ICN vs channel loss to be consistent with the way the cable is being described and tested.</td>
<td>ACCEPT IN PRINCIPLE. See response comment#57</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>85A-4</td>
<td>422</td>
<td>46</td>
<td>E</td>
<td>A</td>
<td>Anslow, Peter Nortel Networks</td>
<td>&quot;(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)&quot; is unclear and does not conform with the style manual.</td>
<td>ACCEPT IN PRINCIPLE. See response comment#168.</td>
<td>C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>86.1</td>
<td>SC</td>
<td>285</td>
<td>34</td>
<td>TR</td>
<td>D</td>
<td>Ghiasi, Ali Broadcom</td>
<td>The PMD electrical definition XLPPI and CPPI has no MDI definition</td>
<td>REJECT. This comment was WITHDRAWN by the commenter.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The medium dependent interface (MDI) for Clause 86 PMDs is the optical interface between the transmission medium (fiber) and the PMD (see 1.4.220 for definition of MDI). XLPPI and CPPI are physical instantiation of PMD service interface for 40GBASE-SR4 and 100GBASE-SR10.
In table 86.8, unlike the case for Stressed receiver sensitivity which has an explicit entry for the attribute, there is no entry for a receiver tolerance attribute, only conditions for such. Further, there is no explicit link to the test definition in 86.8.4.8 which may compound the confusion of the missing test entry. Finally, since this is a test of the ability of a system to track low frequency jitter, it would be helpful to note (similar helpful information are included in footnotes a & c) that the test is not intended for subsystems where CDR and/or bit-error-detector functions are not included. See figure 86-14 which shows a System under test, SUT, comprising a PCS, PMA and PMD. Without the CDR and bit-error-detector of the PMA and/or PCS, equipment external to the SUT would be needed and the test would become, primarily, a test of this external equipment.

**Suggested Remedy**

In Table 86-8, insert an entry, "Receiver jitter tolerance in BER, each lane" above the "Conditions of receiver tolerance test". Append a footnote indicator at the end of the entry. In the Type column enter "Max". In the value column enter "10^-12" and leave a blank in the units column. For the footnote, insert, "Measured with conformance test signal at TP3. See 86.8.4.7. This is test of the system receiver's ability to track low frequency jitter and is inappropriate for any subsystem that does not include CDR and/or bit-error-detector function(s)."

**Response**

ACCEPT IN PRINCIPLE.

In Table 86-8 add a note to "Receiver jitter tolerance signal level in OMA, each lane" to say: "This is test of the optical receiver's ability to track low frequency jitter and is inappropriate for any subsystem that does not include a CRU."

See also response to comment #188

---

Footnote b in Table 86-8 states, "Measured with conformance test signal at TP3 (see 86.8.4.7) for BER = 10^-12.", yet the setup conditions are J2 and J9 and, at least where the nPPI interface is exposed, see item e of 86.8.4.8, the output criteria is an eye mask with a 5E-5 hit ratio. No where is BER = 1E-12 mentioned. This apparent conflict can be confusing. Since 86.8.4.7 references 52.9.9 which calls for operation, "with BER less than 10^-12", there is no need to mention BER in note b and the apparent conflict is removed.

**Suggested Remedy**

Change Footnote b from "Measured with conformance test signal at TP3 (see 86.8.4.7) for BER = 10^-12." to "Measured with conformance test signal at TP3 (see 86.8.4.7)."

**Response**

ACCEPT.

The stressed receiver test refers to 52.9.9 for the test method which explicitly calls for a BER of 10^-12.

---

"an ideal 4th order Bessel Thompson response". However all other occurrences use "fourth" rather than "4th" and the style manual also states that "In general text, isolated numbers less than 10 should be spelled out."

**Suggested Remedy**

Change "an ideal 4th order" to "an ideal fourth order"

**Response**

ACCEPT IN PRINCIPLE.

Also in 88.8.8 change "Thompson" to "Thomson"
Cl 86 SC 86.8.4.8 P 301 L 33 # 190

Comment Type TR   Comment Status A

Petrilla, John Avago Technologies

Clause 68.6.11 is referenced with exceptions. There is no exception declared for the requirement in 68.6.11, "The optical waveform is connected ... and mode-conditioning patch cord suitable for 62.5/125 um fiber". The "mode-conditioning patch cord suitable for 62.5/125 um fiber" does not seem necessary for SR and, if not, is an unnecessary burden. If such a mode-conditioning patch cord is required, then further definition of its characteristics and use are required.

Suggested Remedy
In 68.6.11 add another exception, f), to the list that states, 'the mode-conditioning patch cord suitable for 62.5/125 um fiber is not used'.

Response
ACCEPT IN PRINCIPLE.
In 86.8.4.8 add another exception to the list: 'f) The mode-conditioning patch cord suitable for 62.5/125 um fiber is not used.'

Cl 86A SC 86A.1 P 427 L 15 # 192

Petrilla, John Avago Technologies

Comment Type E   Comment Status R

In the overview it's said about PPI that, "It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside." As PPI can similarly support 40GBASE-LR4 modules, the overview should make that visible. Further PPI does not preclude use of CDRs within a module.

Suggested Remedy
Change from, "It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside." to "It allows the construction of compact optical transceiver modules for 40GBASE-SR4, 40GBASE-LR4 or 100GBASE-SR10 with no clock and data recovery circuits required inside."

Response
REJECT.
Draft 2.2 says "allows" so the "required" isn't needed.
The suitability of PPI for 40GBASE-LR4 has not been shown; the expected link induced eye closure penalty for LR4 is significantly worse than for SR4.
Cl 86A  SC 86A.4  P 431  L 27  # 231
Misek, Brian  Avago Technologies

**Comment Type:** T  **Comment Status:** A

The inclusion of DDPWS for host Rx testing makes no sense at all to me. I have tried to find the reason behind this inclusion and can not find the rational. In fact I can find no comment or comment reponse that calls for this in the comments on 2.0 which led to this being inserted as a TBD. The only comment resolution I can find for the value has no technical backing for the number.

This type of jitter, is no more difficult to deal with for an electrical host Rx in a limiting application then jitter induced by ISI behind the limiter function. The inclusion in the spec only serves to make the test harder to create. The test system must have a second Sine generator and wideband noise source, to modulate the amplitude of a signal only to have it clipped with a limiter. I think that burdening the host vendors with this test for no proven benefit is not in the best interest of this group. If there is some proven benefit to this test parameter I would like to see it, which should of been in the record for why it was included.

Simultaneous meeting of J2 and J9 can be done in a more straight forward manner with edge modulation by random interference for J9 control(if needed) and the existing ISI for J2 control.

**Suggested Remedy:**
- Remove DDPWS from Table 86A-4
- Remove line 48 components dealing with this "sinusoidal interference (SI), and random interference (RI), all"
- Remove line 51 on page 442 "The test signal at TP4 has DDPWS as defined by Table 86A-4."
- Remove Voltage stress block from Figure 86A-9
- Remove paragraph at line 11 page 443 "A voltage stress is to be applied before the limiter function. This stress is composed of a single tone sinusoidal interferer (SI) in the frequency range 100 MHz to 2 GHz and a broadband noise source (RI) with a minimum power spectrum -3 dB point of 6 GHz and minimum crest factor of 7. It is the intent that this combination of voltage stress and limiting function introduce pulse-shrinkage jitter behavior. However no more than 20% of the J2 Jitter is created by the sinusoidal interferer."
- Change line 5 page 444 from 80% to 100% and remove the following 2 lines. "The sinusoidal interferer amplitude is then turned on and adjusted until the required level of J2 Jitter is achieved. The frequency of any sinusoidal interferer is asynchronous to the characteristic frequencies of the signal."
- Remove lines 9 to 11 page 444 "A compliant test signal exhibits Data Dependent Pulse Width Shrinkage (defined in 86A.5.3.4) as specific in Table 86A-4. This is measured with noise and clock-jitter sources turned off.
- Remove remove line 15-21 page 444 "Then the RI (random interference) voltage stress is added until the specified value of J9 Jitter is achieved. If necessary the sine interferer is readjusted to obtain the required level of J2 Jitter and if the sinusoidal interferer is changed then the random interferer is readjusted to obtain the required level of J9 Jitter. Iterative adjustments of the sinusoidal interferer and random interferer are made until the required values of both J2 Jitter and J9 Jitter are achieved."

**Response:**  **Response Status:** C

ACCEPT IN PRINCIPLE.
The DDPWS spec constrains the variety of test stressor eyes that would be allowed if just J2 and J9 specs were in place.

The test configuration shown in figure 86A-9 is an example of a test configuration that could be used to generate a test signal conforming to table 86A-4. In order to make this clearer, change title of figure 86A-9 to "Example jitter tolerance test configuration". Also make the "BT4 7.5 GHz" fit within the box.

[Editor's note: Late comment for consideration by the Task Force]

Cl 86A  SC 86A.4.1  P 428  L 21  # 14
Dawe, Piers  Independent

**Comment Type:** T  **Comment Status:** A

If Table 86A-3, nPPI module electrical output specifications at TP4, has a termination mismatch spec, why doesn't Table 86A-1, nPPI host electrical output specifications at TP1a? I don't believe that a 1 MHz measurement will be affected by the few inches of PCB trace in the host, as was alleged.

**Suggested Remedy:**
- Add row, Termination mismatch at 1 MHz, max 5%.

**Response:**  **Response Status:** C

ACCEPT.
Ghiasi, Ali

Comment Type: TR
Comment Status: R

With current set of specifications the SerDes transmitter may have very large amount of de-emphasis 3-5 dB resulting in significant distortion at TP1a and also see comment 216/218 on D2.1

Suggested Remedy:
The options here are either limit max DDJ to about 0.125 UI or max 3 dB de-emphasis, see ghiasi_03_0909

Response: Response Status: U

REJECT.
J2 spec constrains DDJ and eye mask constrains excessive emphasis.
Although ghiasi_03_0909 shows an example module/host combination with a near failing Tx eye mask at TP2, there is insufficient information to determine the corrective action required in the spec to avoid a potential eye-mask issue. Further work is invited.

Anslow, Peter

Comment Type: E
Comment Status: A

In the equations of clause 86A, the phrase "f is the frequency in gigahertz" is used. In the rest of the draft (27 instances) this is "f is the frequency in GHz". In the base document the words "gigahertz", "megahertz" or "kilocycle" do not occur at all.

Suggested Remedy:
Change "gigahertz" to "GHz" throughout clause 86A (14 instances)

Response: Response Status: C

ACCEPT.

Petrilla, John

Comment Type: E
Comment Status: A

The title for figure 86A-1 is, "Reflection specifications" but is more properly, 'Reflection specifications illustrations' as the specifications are in the associated table and equations. Even the text, see page 428, line 44 states, "the limit given in Equation 86A-2 and illustrated in Figure 86A-1."

Suggested Remedy:
Change the title for figure 86A-1 from, "Reflection specifications", to 'Reflection specifications illustrations'. Do likewise for figures 86A-2, 3, 4, 5 & 6.

Response: Response Status: C

REJECT.
The title follows the precedent set in the rest of the document and in clause 52.
IEEE P802.3ba D2.2 40Gb/s and 100Gb/s Ethernet comments

Draft 2.2 Comments

CI 86A SC 86A.4.2 P430 L 14 # 96
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

With current set of specifications the SerDes transmitter may have very large amount of de-emphasis 3-5 dB resulting in significant distortion at TP1a and also see comment 216/218 on D2.1

SuggestedRemedy

The options here are either limit max DDJ to about 0.125 or max 3 dB de-emphasis, see ghiasi_03_0909

Response Response Status U

REJECT.

see also response to comment 131

CI 86A SC 86A.4.2 P431 L 16 # 194
Petrilla, John Avago Technologies

Comment Type ER Comment Status A

In Table 86A-4, as in table 86-8, there is no explicit entry for a signal or jitter tolerance attribute, only the conditions are listed.

SuggestedRemedy

In Table 86A-4, insert a row, "Applied sinusoidal jitter", for low frequency SJ to the receiver signal tolerance test conditions. Enter 'TP4' in the Test Point column, 'See 86A.5.3.8' in the Spec.values column, and leave the Units and Conditions columns blank.

Response Response Status C

ACCEPT IN PRINCIPLE.

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Comment Type T Comment Status A

Transition time is given as 34 ps TBC.

SuggestedRemedy

Confirm it or change it to a better number. Delete "TBC".

Response Response Status C

ACCEPT IN PRINCIPLE.

Delete "TBC"
In Table 86A-4, the value for the Transition time value is shown as, "34 TBC". A predetermined transition time value may preclude generating a stressed signal that reaches all of the eye mask coordinates, J2, J9 and DDWPS simultaneously. Since there appears to be more value having an input signal that simultaneously stresses min and max signal levels, eye mask corners, J2, J9 and DDWPS, a transition time spec may be redundant.

Suggested Remedy
Delete the Transition time requirement from Table 86A-4 and in 86A.5.3.8.5 append to the end of the sentence, "The vertical eye opening and peak level specifications are verified." such that eye mask...jitter values DDPWS, J2, J9 are all simultaneously met. In 86A.5.3.8.5 page 444, line 12, change the phrase, "... the amplitude and the transition time are as given in Table 86A-4." to "... and the amplitude are as given in Table 86A-4."

Response
REJECT.
Commenter invited to submit material which justifies removing the Transition time spec.

The task force believes that it is more important to stress the minimum signal levels than the maximum, so there is no need to remove the rise time requirement.

Comment Type TR
Comment Status R

In equation 86A-7 change +0.861 to -0.861.

Suggested Remedy
Change MCB frequency independent term from -0.0006 to -0.006

Suggested Remedy
Replace crosstalk limits of equations 86A-11 through 86A-14 and associated text and Figure 86A-6 with a requirement that the ICN limits of 85.10.10.3 must be met.

Response
ACCEPT IN PRINCIPLE.

Replace crosstalk limits of equations 86A-11 through 86A-14 and associated text and Figure 86A-6 with a requirement that the ICN limits of 85.10.10.3 must be met.
Comment Type: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

**Comment**: Mated test fixture crosstalk loss in current draft are place holder and some of the limit specially PSFXT will impact the measurements accuracy.

**Suggested Remedy**
For the new limits please see ghiasi_01_0909

**Response**
ACCEPT IN PRINCIPLE.
see response to comment 113

---

**Comment**: Is the position of bit 1 in PRBS9 defined in 802.3? If so please cite a reference? If not delete, "These are bits 10 to 18 and 1 to 14, respectively." or create a definition for bit 1.

**Suggested Remedy**
Unless a definition that permits locating bit 1 exists, delete the sentence, "These are bits 10 to 18 and 1 to 14, respectively.". Otherwise cite the definition.

**Response**
ACCEPT IN PRINCIPLE.

---

**Comment**: The 'shall' in "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." seems more an instruction to the editors then to implementers.

**Suggested Remedy**
Change, "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." to "Host electrical receiver signal tolerance is defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6. or if a shall statement is desired to "To be compliant a host electrical receiver signal tolerance shall satisfy the requirements defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6."

**Response**
ACCEPT IN PRINCIPLE.

---

**Comment**: The term LB in figure 86A-11 is not defined. Assuming it's the same LB as in 87 and 88, the definition in 88.8.10, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested." can be referenced or copied and pasted below figure 86A-11.

**Suggested Remedy**
Insert after figure 86A-11, the definition for LB, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

**Response**
ACCEPT IN PRINCIPLE:
Add table with appropriate expressions to describe figure 86A-11, following the style of table 87-13, with editorial licence to make it look smashing !
add footnote to table:
"LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

See king_01_0909 for example table and text
Cl 86A SC 86A.6 P 444 L 37 # 44
Mark, Gustlin Cisco

Comment Type TR Comment Status A
Formula 86A-19 seems incorrect from in the range from 0.2 to 7GHz, should be
\[ = -0.114-0.8914*?f-0.846*f \]
SuggestedRemedy
Change the + to a -.
Response Response Status C
ACCEPT.
Note: Comment 15 has changed the sign of this equation. see also comments 68, and 232

Cl 86A SC 86A.6 P 446 L 37 # 232
Misek, Brian Avago Technologies

Comment Type T Comment Status A
Sign error in equation 86A-19
"+ 0.846f" should be "- 0.846f"
SuggestedRemedy
change
"+ 0.846f" should be "- 0.846f"
Response Response Status C
ACCEPT IN PRINCIPLE.
see comments 44 and 68

Cl 86A SC 86A.6 P 446 L 37 # 68
Dawe, Piers Independent

Comment Type T Comment Status A
Sign error in equation 86A-19. It should be a scaled version of D2.1 86A-20.
SuggestedRemedy
Change + 0.846f to - 0.846f.
Response Response Status C
ACCEPT IN PRINCIPLE.
see comment 44 and 232

Cl 86A SC 86A.6 P 446 L 44 # 181
Dudek, Mike QLogic

Comment Type T Comment Status A
The minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The HCB PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.
SuggestedRemedy

Response Response Status C
ACCEPT IN PRINCIPLE.
Duplicate Comment see comment 179.

Cl 86A SC 86A.6 P 446 L 45 # 179
Dudek, Mike QLogic

Comment Type TR Comment Status A
Equation 86A-20 is wrong. (requires gain at high frequency and has a discontinuity) and doesn't match Figure 86-12
Also with the correction the minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The HCB PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.
SuggestedRemedy
Add a row to the equation
0.01<f<1 value 0
Change the existing first row to +0.5 - 0.5*f
Consider also increasing the minimum loss at Nyquist by approx 0.5dB by changing this existing first row to 0.6 - 0.6*f and changing the second row to -3.7
Response Response Status C
ACCEPT IN PRINCIPLE.
Change sign to make the first row
+0.5 - 0.5*f
Note: Comment 15 has changed the overall sign of this equation.
Also, add a row to the equation
0.01<f<1 value 0
The minimum loss issue has been overtaken by events. The Host PCB min loss in Clause 85 has been reduced to 0.67 dB, which does not require the TP0 to TP2 min loss to change.
<table>
<thead>
<tr>
<th>Comment Type</th>
<th>T</th>
<th>Comment Type</th>
<th>TR</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IEEE is not the same as ISO/IEC</strong></td>
<td></td>
<td><strong>The L0-L3 is not connected to any instantiation logical or Physical</strong></td>
<td></td>
</tr>
<tr>
<td>SuggestedRemedy</td>
<td>Delete '(IEEE)'</td>
<td>SuggestedRemedy</td>
<td>Please move L0-L3 before and after optical mux.</td>
</tr>
<tr>
<td><strong>Accept in principle.</strong></td>
<td></td>
<td><strong>REJECT.</strong></td>
<td></td>
</tr>
<tr>
<td>Some clauses in the base standard (e.g. 46, 53, 57) use &quot;to the ISO/IEC (IEEE) OSI&quot; while others (e.g. 22, 54, 65) use just &quot;to the ISO/IEC OSI&quot;.</td>
<td></td>
<td>This comment was WITHDRAWN by the commenter.</td>
<td></td>
</tr>
<tr>
<td>Delete &quot;(IEEE)&quot; here, in subclause 88.1 and also in subclause 81.1</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>See also comment #12</td>
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<tr>
<td><strong>The L0 through L3 are the four lanes. This designation is not specifically optical or electrical.</strong></td>
<td></td>
<td><strong>XLAUI is an optional interface and therefore may not be present.</strong></td>
<td></td>
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<tr>
<td>The same arrangement is shown in Figure 53-2 and also in Figure 86-2.</td>
<td></td>
<td>See also comment #121</td>
<td></td>
</tr>
</tbody>
</table>
"Stressed receiver sensitivity shall be within the limits given in Table 87-8 for 40GBASE-LR4 if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2."

Stressed receiver sensitivity compliance is a normative requirement, but the test setup has a number of variable parameters: BT filter parameters, sinusoidal jitter frequency, sinusoidal amplitude interferer frequency and amplitude, etc.

Given the wide range of alternative configurations that could meet the stressed eye VECP and SEJ values, is it the intention of the committee that all such test setups be tested against the Stressed receiver sensitivity requirement?

i.e. In order to be compliant is it sufficient to demonstrate compliance at just one such configuration, or does failure at any such configuration mean an implementation is non-compliant.

I see hazards in either position. A single pass might allow an implementation to select a set of parameters particularly favorable in order to pass. Conversely demonstrating that there is no single combination of parameters that does not cause a failure would cause testing to take an impracticable amount of time.

Suggested Remedy
Add some text indicating the committees intention.

Response
There will be a contribution at the September interim to support this comment

REJECT.

The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz. Providing such a wide range of frequency (in addition to amplitude) makes compliance testing difficult.

Suggested Remedy
Select a single sinusoidal amplitude interferer frequency of 1GHz.

There will be a contribution at the September interim to support this comment

Response
REJECT.

The added sinusoidal jitter frequency is constrained to be at least a factor of ten higher than the loop bandwidth of the receiver CDR used, making it a specific frequency is an unnecessary constraint on test equipment manufacturers. This variation is the same as was used in subclause 52.9.9.1.
Cl 87 SC 87.8.11.2 P 328 L 8 # 77
Dawe, Piers Independent

Comment Type TR Comment Status A

87.8.11.2 has a definition of VECP that contradicts the rest of 802.3. Detail follows:
In 52.9.9.2, VECP is defined as 10 log(OMA/AO). Applies to 10G, scrambled, including 10GEPON. Also applies in 86.8.4.7.
In 58.7.11.2, VECP is defined as 10 log(10(AN)/AO), where AN is to be measured with a square wave pattern consisting of four to eleven consecutive ones followed by an equal run of zeros. Applies to 100M and 1G, block coded.
In 53.9.14, VECP is defined as 10 log(OMA/AN) (sign error), where "AN is the normal amplitude without ISI, as measured in Figure 53-12." Applies to 10GBASE-LX4 (3.125 GBd, block coded).
10GBASE-LRM doesn't use VECP.
In D2.2 87.8.11.2, VECP is defined as 10 log(AN/AO), where "AN is the normal amplitude without ISI, as shown in Figure 87-4." but unlike Figure 53-12, Figure 87-4 shows AN as difference of means of histograms at crossing time, which is not exactly OMA nor the "normal amplitude without ISI". (52.9.9.2 says "OMA is the normal amplitude without ISI, as shown in Figure 52-11" but 52.9.5 gives a precise definition.) D2.2 88.8.5.1 uses the 52.9.9.2 definition of VECP while 88.8.10 uses 87.8.11.

Suggested Remedy
Definitions and stressed eye generators will be shared across 40GBASE-LR4, 10GBASE-LR, 10GBASE-ER and 10GEPON, so 87.8.11.2 should conform.
Change the definition of VECP to 10 log(OMA/AO).

To avoid confusion, modify Figure 87-4 to remove "AN" (which is the "Approximate OMA" of Fig 52-11 and "Approximate AN" of Fig 58-9, and it's not relevant) and remove the histograms at the crossing time.
If wished, add pointers to illustrate where OMA would be, at the settled one and zero levels (this would be better done with the waveform of Figure 53-12 or 58-9).

Response Response Status W
ACCEPT IN PRINCIPLE.
In equation 87-1 change "10log(AN/AO)" to "10log(OMA/AO)" and "AN is the normal amplitude without ISI, as shown in Figure 87-4." to "OMA is the optical modulation amplitude as defined in 87.8.5".
In Figure 87-4 remove AN and related histograms etc.
In 88.8.5.1 change "as defined in 52.9.9.2 is less than" to "as defined in 87.8.8.11.2 is less than".

Cl 87 SC 87.8.11.2 P 329 L 16 # 47
Szczepanek, Andre HSZ Consulting Ltd

Comment Type TR Comment Status R

"With the sinusoidal interference and sinusoidal jitter turned off, greater than two thirds of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the fourth-order Bessel-Thomson filter."

Suggested Remedy
Change to:
"With the sinusoidal interference and sinusoidal jitter turned off, between 0.6 and 0.7 of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the fourth-order Bessel-Thomson filter."

There will be a contribution at the September interim to support this comment

Response Response Status C
REJECT.
[Editor's note: Subclause changed from 8.11.1 to 87.8.11.2. Commenter did not indicate comment type. Assigned comment Type TR]
This text is drawn from clause 52 and includes a range of 0.667 to 1.0 of the VECP. The proposed changes restrict the range and is an unnecessary constraint on test equipment manufacturers.

Comment Type ER Comment Status A

"The sinusoidal jitter added should result in at least 0.05 UI peak to peak DCD."

This is the only indication of a minimum DCD requirement in the draft and is not normative anyway. This sentence is redundant and should be removed.

Suggested Remedy
Remove the sentence.

Response Response Status C
ACCEPT IN PRINCIPLE.
[Editor's note Subclause changed from 8.11.1 to 87.8.11.2]
Many requirements are contained at only one place in the draft.

Change "The sinusoidal jitter added should result in at least 0.05 UI peak to peak DCD." to "The sinusoidal jitter added should result in at least 0.05 UI of pulse width shrinkage."
All but two 10G Ethernet Bessel-Thomson responses for measurement (even the one in 87.8.9) have a bandwidth / reference frequency fr / 3 dB upper electrical cutoff frequency of 7.5 GHz. 86.8.4.4 has 6.2 GHz for a reason. Here we have 7.73 GHz. Implementers are going to use the same 10G instruments for 40GBASE-LR4 as for 10GBASE-L and 10GEPON, so this difference, between 7.5 and 7.73, is not practical.

Suggested Remedy
Change 7.73 to 7.5.

Response
ACCEPT.

Elsewhere in 802.3 where a Bessel-Thomson response for measurement (scope or reference receiver) is specified, it isn’t called “3 dB upper electrical cutoff frequency” but “bandwidth” or “reference frequency fr” or simply “7.5 GHz Bessel-Thomson”.

Suggested Remedy
Please change “3 dB upper electrical cutoff frequency” to “reference frequency fr”, or change “ideal fourth-order Bessel-Thomson response with a 3 dB upper electrical cutoff frequency of * GHz” to “ideal * GHz fourth-order Bessel-Thomson response”, or “ideal fourth-order Bessel-Thomson response with a bandwidth of * GHz”. But please don’t try to change “response” to “loss”!

Response
ACCEPT IN PRINCIPLE.

IEEE is not the same as ISO/IEC

Suggested Remedy
Delete ’(IEEE)’

Response
ACCEPT IN PRINCIPLE.

L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2. See also comment #125

Proposed Response
Response Status
REJECT.

This comment was WITHDRAWN by the commenter.

CAUI is an optional interface and therefore may not be present. The gearbox function is within the PMA function and a possible future 25G electrical interface would not need it. See also comment #124

Proposed Response
Response Status
REJECT.

This comment was WITHDRAWN by the commenter.

L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2. See also comment #125

Proposed Response
Response Status
REJECT.

This comment was WITHDRAWN by the commenter.

L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2. See also comment #125

Proposed Response
Response Status
REJECT.

This comment was WITHDRAWN by the commenter.

L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2. See also comment #125

Proposed Response
Response Status
REJECT.

This comment was WITHDRAWN by the commenter.

L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2. See also comment #125
Stress receiver sensitivity has corner frequency of 10 MHz also see comment 224 and 225. D2.1 can limit the receiver to analog type instead of more efficient lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remain even in the case of future generations where ASIC/SerDes operate at 25 G!

Propose to consider corner frequency of 7 MHz instead of current 10 MHz and change 100 KHz to 70 KHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

Propose to consider CRU BW 7.5 MHz instead of current 10 MHz, see ghiasi_02_0909

Propose to consider CRU BW 7 MHz instead of current 10 MHz, see ghiasi_02_0909

Propose to consider CRU BW 7 MHz instead of current 10 MHz. Higher CRU BW has very little benefit on the VCO noise and power supply noise but significant penalty on the receiver, see ghiasi_02_0909

ACCEPT IN PRINCIPLE.

In Table 88-13 correct the formula: change $2 \times 10^5/f$ to $5 \times 10^5/f$

The Task Force voted on whether to:
A - Leave the CRU corner frequency at 10 MHz and correct the formula in Table 88-13
B - Change the CRU corner frequency to 7 MHz in a consistent manner in clause 88

A 9
B 1
There is a wrap around error in the listing for Clause 52.

Suggested Remedy
- fix wrap-around error for Clause 52 entry.

Response
- ACCEPT IN PRINCIPLE.
  Fix ToC formatting as appropriate